Jameco Part Number 41398ATT

AT&T

DATA SHEET

M41256xx-10B, -12B, & -15B Dynamic RAM

FEATURES

- 262,144 words × 1-bit organization
- 100/120/150 ns access time from $\overline{RE}$
- 50/60/75 ns access time from $\overline{CE}$
- 385/360/330 mW active power, Page Mode, 413/385/360 mW active power, Nibble Mode, at minimum cycle time
- 25 mW standby power
- Multiplexed address inputs
- ±10% power supply tolerance
- Read-Modify-Write capabilities
- $\overline{RE}$ Only Refresh/Hidden Refresh
- Latched or high impedance output during refresh
- 256 refresh cycles
- Nibble Mode/Page Mode options
- $\overline{CE}$ before $\overline{RE}$ refresh with Nibble Mode Option
- Available in 2 plastic or hermetic ceramic DIP, plastic leaded chip carrier (PLCC), and hermetic ceramic leadless chip carrier (LCC)

DESCRIPTION

The M41256xx-10B, -12B, & -15B integrated circuits are high-speed, low-power 262,144 words by 1-bit dynamic random access memory (DRAM) devices. These devices are available with various mode, speed, and package options.

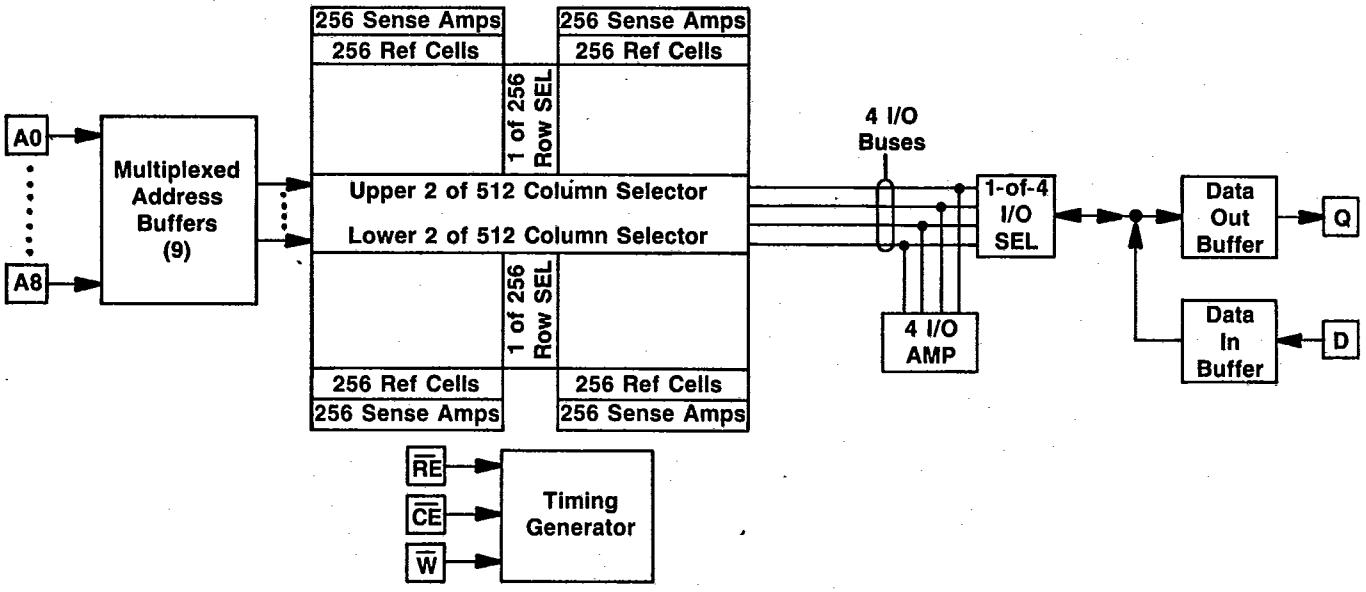


Figure 1. Page Mode Block Diagram

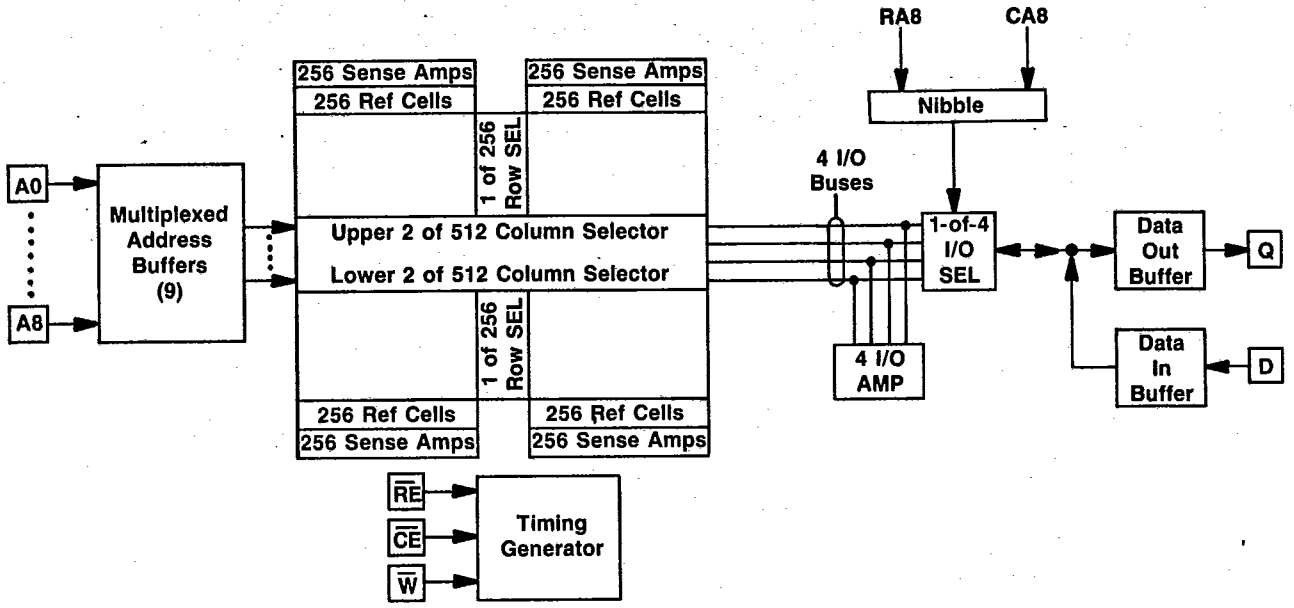
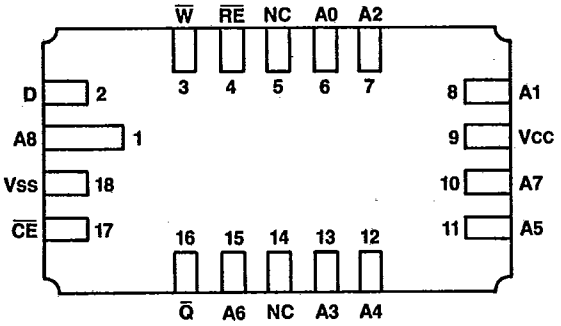


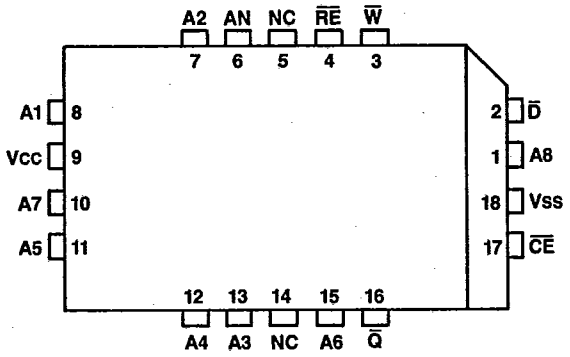
Figure 2. Nibble Mode Block Diagram

USER INFORMATION

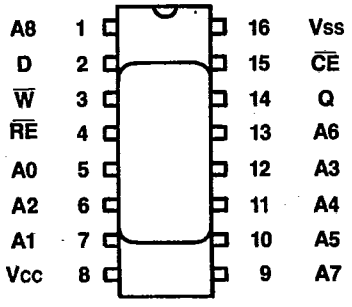
Pin Descriptions



18 I/O Ceramic LCC



18 I/O PLCC



16-Pin DIP

Pin Description Key	
Symbol	**Name**
Vcc	+5 V Supply
D	Data In
Q	Data Out
A(0–8)	Address Input (0–8)
$\overline{W}$	Write Enable
$\overline{RE}$	Row Enable
$\overline{CE}$	Column Enable
Vss	Ground
NC	No Connect

Figure 3. Pin Function Diagram

CHARACTERISTICS

Operating Conditions (T_A = 0 to 70°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltages	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V
Input Voltages* High Level — All Inputs (Logic 1) Low Level — All Inputs (Logic 0)	 V_{IH} V_{IL}	 2.4 −1.0	 — —	 6.5 0.8	 V V
Refresh Cycle Time**	tREF	—	—	4.0	ms

* Application of invalid levels may destroy stored information during that cycle as well as the first cycle using valid levels. Data out is indeterminate.

** Addresses A0—A7 are used for refresh. A8 must be a valid one or zero.

Electrical Characteristics

(V_{CC} = 5 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C)

		M41256xx-10B		M41256xx-12B		M41256xx-15B		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Output Voltages Low Level (I_{OL} = 4.2 mA) High Level (I_{OH} = −5.0 mA)	 V_{OL} V_{OH}	 — 2.4	 0.4 —	 — 2.4	 0.4 —	 — 2.4	 0.4 —	 V V
Power Supply Currents Operating Current (Average Operating Current $\overline{RE}$ & $\overline{CE}$ Cycling, tRELREL = minimum) Page Mode Option Nibble Mode Option	 I_{CC1} I_{CC1}	 — —	 70† 75†	 — —	 65† 70†	 — —	 60† 65†	 mA mA
Standby Current ($\overline{RE}$ = V_{IH}, Q = High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA
Refresh Current (Average Operating Current, Refresh Mode Operation) $\overline{RE}$ Cycling, $\overline{CE}$ = V_{IH}, tRELREL = min. Page Mode Option Nibble Mode Option $\overline{CE}$ before $\overline{RE}$ Nibble Mode Option	 I_{CC3} I_{CC3} I_{CC3}	 — — —	 55† 60† 95†	 — — —	 50† 55† 90†	 — — —	 45† 50† 85†	 mA mA mA
Page Mode Current (Average Operating Current, Page Mode Operation, $\overline{RE}$ = V_{IL}, $\overline{CE}$ Cycling, tCELCEL = minimum)	I_{CC4}	—	50†	—	45†	—	40†	mA
Nibble Mode Current (Average Operating Current, Nibble Mode Operation, $\overline{RE}$ = V_{IL}, $\overline{CE}$ Cycling, tNCELCEL = minimum)	I_{CC5}	—	55†	—	50†	—	45†	mA

† Maximum occurs at T_A = 0°C. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} are specified with output open-circuited.

Parameter	Symbol	M41256xx-10B		M41256xx-12B		M41256xx-15B		Unit
		Min	Max	Min	Max	Min	Max	
Input Leakage Current (V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other leads at 0 V)	I_I	−10	10	−10	10	−10	10	μA
Output Leakage Current (Q = High Impedance, V_Q = 0 to V_{CC})	I_O	−10	10	−10	10	−10	10	μA
Input Capacitance (A0—A8)††	C_{I1}	—	5	—	5	—	5	pF
Input Capacitance (D, $\overline{W}$ Leads)††	C_{I2}	—	5	—	5	—	5	pF
Input Capacitance ($\overline{RE}$, $\overline{CE}$ Leads)††	C_{I3}	—	10	—	10	—	10	pF
Output Capacitance (Q Lead)††	C_O	—	7	—	7	—	7	pF

†† Parameter periodically sampled and not 100% tested.

Maximum Ratings*

Rating	Symbol	Value	Unit
Voltage Range on V_{CC} Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Power Dissipation	PD	1.0	W
Case Operating Temperature Range	T_C	0 to 85	°C
Ambient Operating Temperature Range	T_A	0 to 70	°C
Ambient Storage Temperature Range**	T_{stg}		
Ceramic Package		−65 to +160	°C
Plastic Package		−55 to +120	°C
Short Circuit Output Current	I_{OS}	50	mA

* Maximum Ratings are defined as the limiting conditions that the user can apply to the device under all variations of circuit and environmental conditions. If any rating is exceeded, permanent damage to the device may result. Extended operation at any of these conditions may result in reduced reliability.

** Bonding or soldering of the external pins of these devices can be performed safely at temperatures up to 300°C.

Timing Characteristics

(V_{CC} = 5 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C) (Notes 1, 2, and 3)

Description	Symbol	JEDEC Symbol	M41256xx-10B		M41256xx-12B		M41256xx-15B		Unit
			Min	Max	Min	Max	Min	Max	
Random Read/Write Cycle Time	tRC	tRELREL	200	–	220	–	260	–	ns
Access Time from $\overline{RE}$ (Notes 4 & 5)	tRAC	tRELQV	–	100	–	120	–	150	ns
Access Time from $\overline{CE}$ (Notes 5 & 6)	tCAC	tCELQV	–	50	–	60	–	75	ns
Output Buffer Turn Off Delay (Note 7)	tOFF	tCEHQZ	0	20	0	30	0	30	ns
Transition Time	tT	tT	2	50	2	50	2	50	ns
$\overline{RE}$ Precharge Time	tRP	tREHREL	90	–	90	–	100	–	ns
$\overline{RE}$ Pulse Width	tRAS	tRELREH	100	10000	120	10000	150	10000	ns
$\overline{RE}$ Hold Time	tRSH	tCELREH	50	–	60	–	75	–	ns
$\overline{CE}$ Pulse Width (Note 8)	tCAS	tCELCEH	50	10000	60	10000	75	10000	ns
$\overline{CE}$ Hold Time	tCSH	tRELCEH	100	–	120	–	150	–	ns
$\overline{RE}$ to $\overline{CE}$ Delay (Note 4)	tRCD	tRELCEL	25	50	25	60	25	75	ns
$\overline{CE}$ to $\overline{RE}$ Precharge Time	tCRP	tCEHREL	0	–	0	–	0	–	ns
Row Address Setup Time	tASR	tRAVREL	0	–	0	–	0	–	ns
Row Address Hold Time	tRAH	tRELRAX	15	–	15	–	15	–	ns
Column Address Setup Time	tASC	tCAVCEL	0	–	0	–	0	–	ns
Column Address Hold Time	tCAH	tCELCAX	15	–	20	–	25	–	ns
Column Address Hold Time Ref. to $\overline{RE}$	tAR	tRELCAX	75	–	90	–	105	–	ns
Read Command Hold Time Ref. to $\overline{RE}$	tRRH	tREHWX	10	–	10	–	10	–	ns
Read Command Setup Time	tRCS	tWHCEL	0	–	0	–	0	–	ns
Read Command Hold Time Ref. to $\overline{CE}$	tRCH	tCEHWX	0	–	0	–	0	–	ns
Write Command Hold Time	tWCH	tCELWX	15	–	20	–	25	–	ns
Write Command Hold Time Ref. to $\overline{RE}$	tWCR	tRELWX	85	–	100	–	120	–	ns
Write Command Pulse Width	tWP	tWLWH	15	–	20	–	25	–	ns
Write Command to $\overline{RE}$ Lead Time	tRWL	tWLREH	30	–	35	–	45	–	ns
Write Command to $\overline{CE}$ Lead Time	tCWL	tWLCEH	20	–	30	–	40	–	ns
Data In Setup Time	tDS	tDVCEL	0	–	0	–	0	–	ns
Data In Hold Time	tDH	tCELDX	15	–	20	–	25	–	ns
Data In Hold Time Ref. to $\overline{RE}$	tDHR	tRELDX	85	–	100	–	120	–	ns
Write Command Setup Time (Note 9)	tWCS	tWLCEL	0	–	0	–	0	–	ns
$\overline{CE}$ to $\overline{W}$ Delay (Read-Modify-Write)	tCWD	tCELWL	25	–	30	–	35	–	ns
$\overline{RE}$ to $\overline{W}$ Delay (Read-Modify-Write) (Note 6)	tRWD	tRELWL	75	–	100	–	125	–	ns
Data In Hold Time (Read-Modify-Write) (Note 6)	tDH	tWLDX	20	–	20	–	20	–	ns
Data In Setup Time (Read-Modify-Write)	tDS	tDVWL	0	–	0	–	0	–	ns
Refresh Period	tREF	tR	–	4.0	–	4.0	–	4.0	ms
Cycle Time (Read-Modify-Write)	tRMW	tWRELREL	245	–	260	–	310	–	ns

M41256xx-10B, -12B, & -15B Dynamic RAM

Description	Symbol	JEDEC Symbol	M41256xx-10B		M41256xx-12B		M41256xx-15B		Unit
			Min	Max	Min	Max	Min	Max	
PAGE MODE OPTION									
Page Mode Cycle Time	tPC	tCELCEL	120	–	130	–	145	–	ns
$\overline{CE}$ Precharge Time	tCP	tCEHCEL	45	–	50	–	60	–	ns
NIBBLE MODE OPTION									
$\overline{CE}$ Cycle Time	tNC	tNCELCEL	50	–	60	–	70	10000	ns
Access Time from $\overline{CE}$ (Notes 5 & 6)	tNCAC	tNCELQV	–	20	–	25	–	30	ns
$\overline{RE}$ Hold Time	tNRRSH	tNCELREH	20	10000	25	10000	30	10000	ns
$\overline{CE}$ Pulse Width	tCAS	tNCELCEH	20	10000	25	10000	30	10000	ns
Write Command Hold Time	tWCH	tNCELWX	10	–	10	–	10	–	ns
Write Command to $\overline{RE}$ Lead Time	tNRWL	tNWLREH	20	–	25	–	30	–	ns
Write Command to $\overline{CE}$ Lead Time	tNCWL	tNWLCEH	20	–	25	–	30	–	ns
Write Command Pulse Width	tNWP	tNWLWH	10	–	10	–	10	–	ns
Data In Hold Time	tDH	tNCELDX	10	–	10	–	10	–	ns
$\overline{CE}$ Precharge Time	tNCP	tNCEHCEL	20	–	25	–	30	–	ns
$\overline{CE}$ to $\overline{W}$ Delay (Read-Modify-Write)	tNCWD	tNCELWL	10	–	15	–	15	–	ns
Data In Hold Time (Read-Modify-Write) (Note 6)	tDH	tNWLDX	10	–	10	–	10	–	ns
$\overline{CE}$ Before $\overline{RE}$ Refresh									
$\overline{CE}$ to $\overline{RE}$ Delay	tFCS	tCELREL	10	–	10	–	10	–	ns
$\overline{CE}$ Hold Time	tFCH	tRELCEX	20	–	25	–	30	–	ns
$\overline{RE}$ Precharge to $\overline{CE}$ Active	tRPC	tREHCEL	0	–	0	–	0	–	ns

Notes:

1. Timing specifications given assume tT = 5 ns.
2. VIH (min.), VIL (max.) are reference levels for timing specifications or input signals. Transition times are to be measured between these reference levels.
3. An initial pause of 100 μs followed by a minimum of 8 refresh cycles is necessary after VCC is applied, to achieve proper device operation. Addresses A0–A7 are used for refresh. A8 must be a valid one or zero.
4. For tRELCEL > tRELCEL (max.), tRELQV will increase by the amount that tRELCEL (max.) is exceeded.
5. Q load assumed to be equivalent to 2 TTL loads and 100 pF.
6. Assumes tRELCEL ≥ tRELCEL (max.).
7. tCEHQZ (max.) defines the time at which Q achieves the open circuit condition.
8. $\overline{CE}$ can be held at Logic 0 for an indefinite time for latched output during refresh. However, tRELRAX must be increased to 100 ns.
9. Non-restrictive operating parameter. If tWLCEL ≥ tWLCEL (min.), the cycle is an early write cycle and the data out (Q) will remain an open circuit (high impedance) for the entire cycle. If tCELWL ≥ tCELWL (min.) and tRELWL ≥ tRELWL (min.), the cycle is a read-write cycle and the data out (Q) will validly reproduce the data contained in the selected cell. If neither of the above sets or conditions is satisfied, data out will be indeterminate.

Timing Diagrams

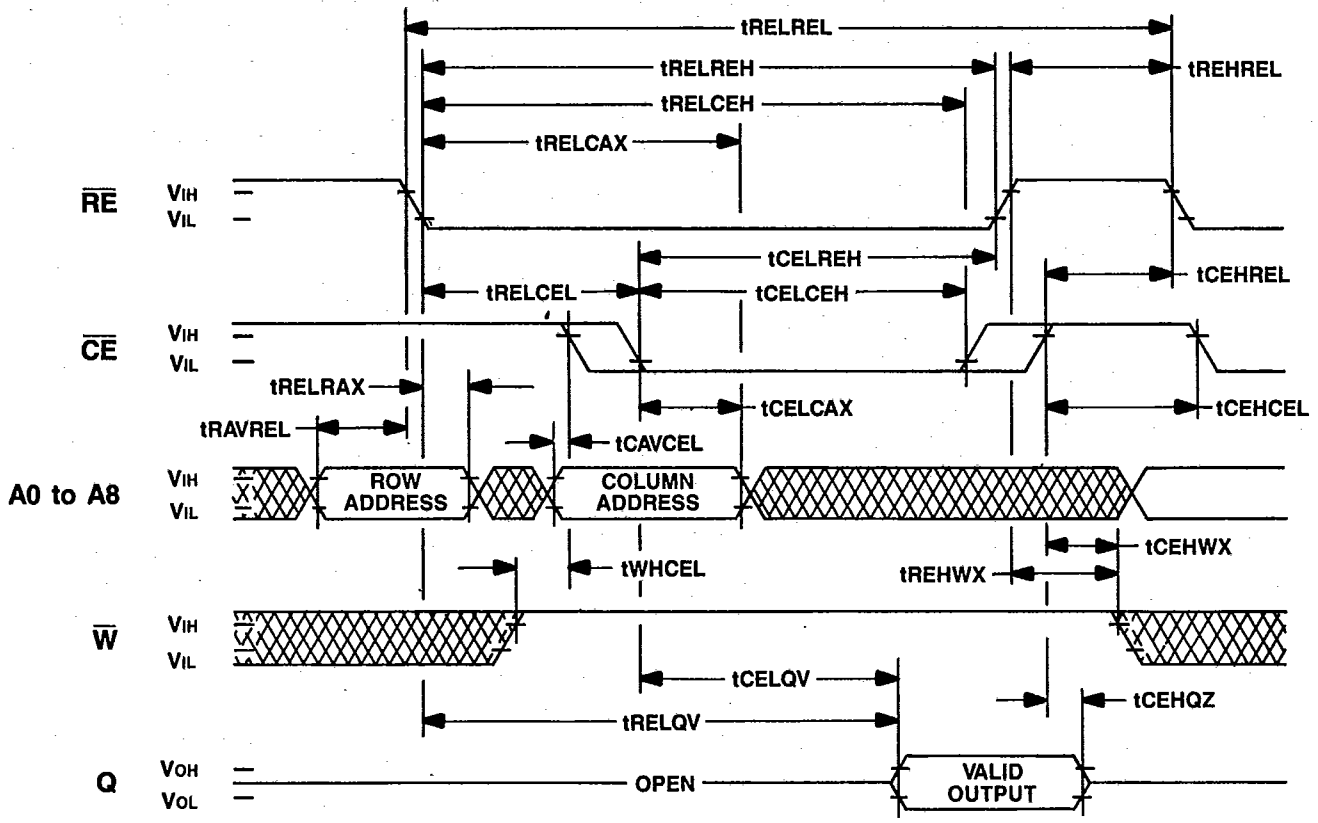


Figure 4. Read Cycle

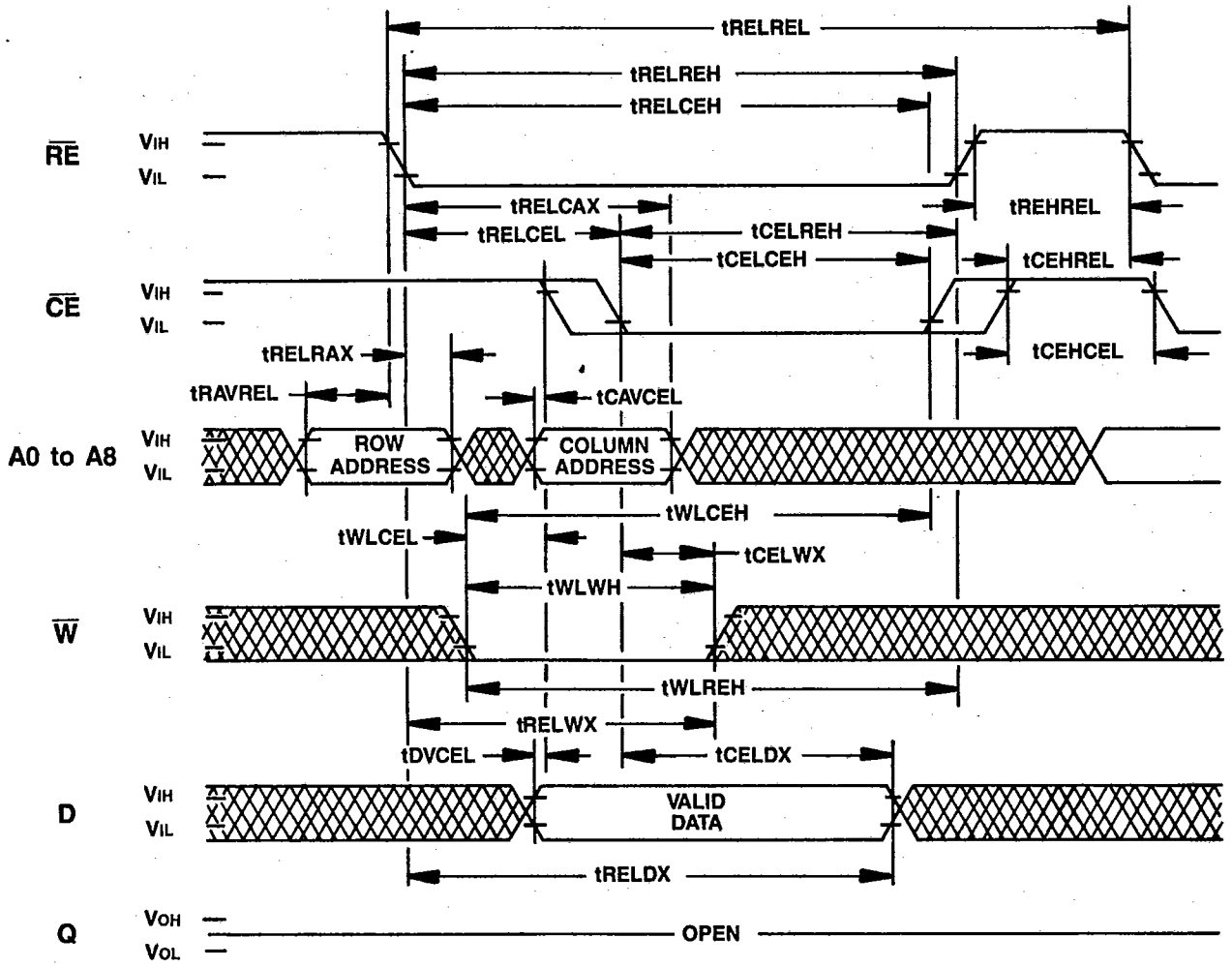


Figure 5. Write Cycle (Early Write)

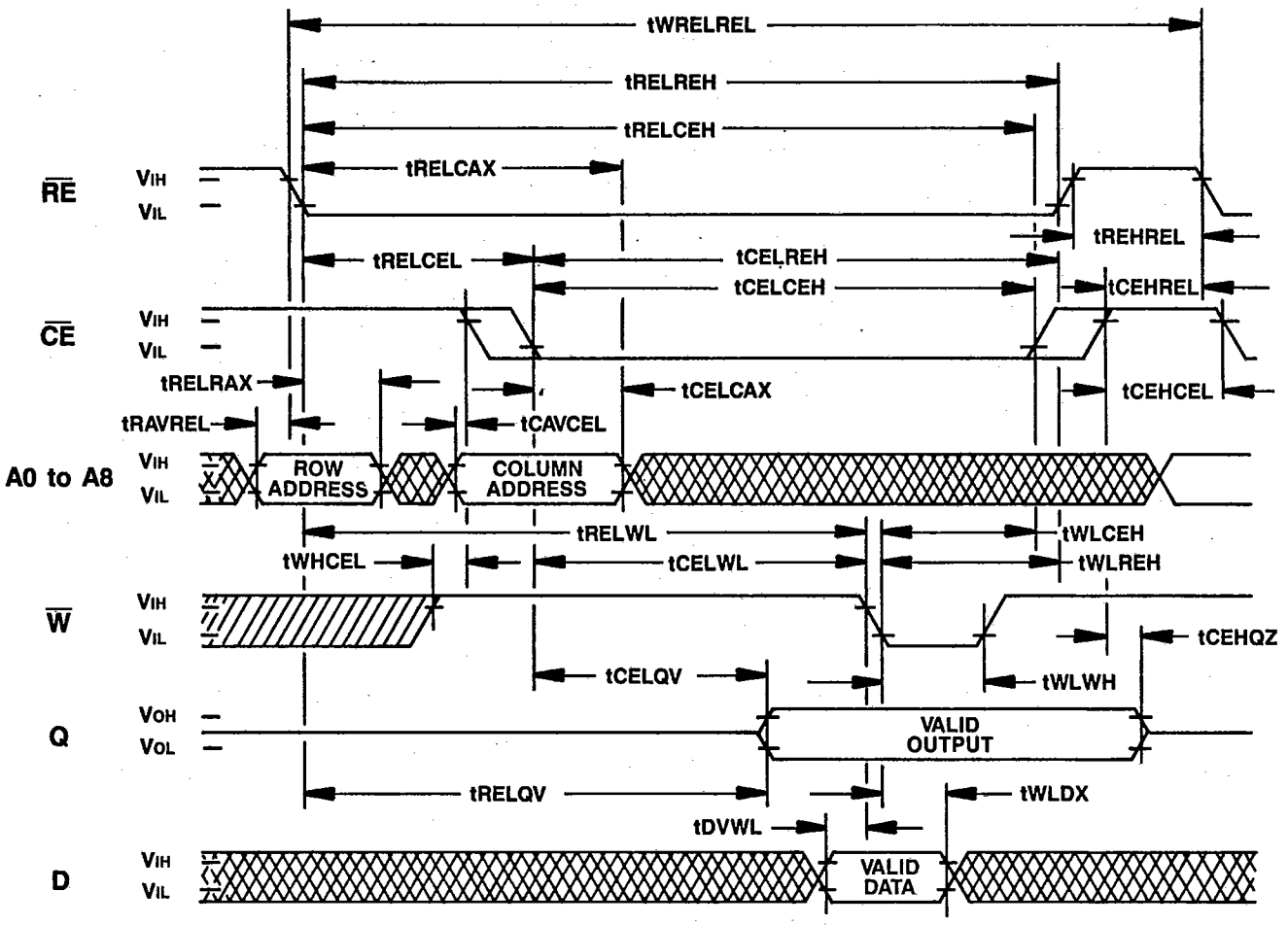
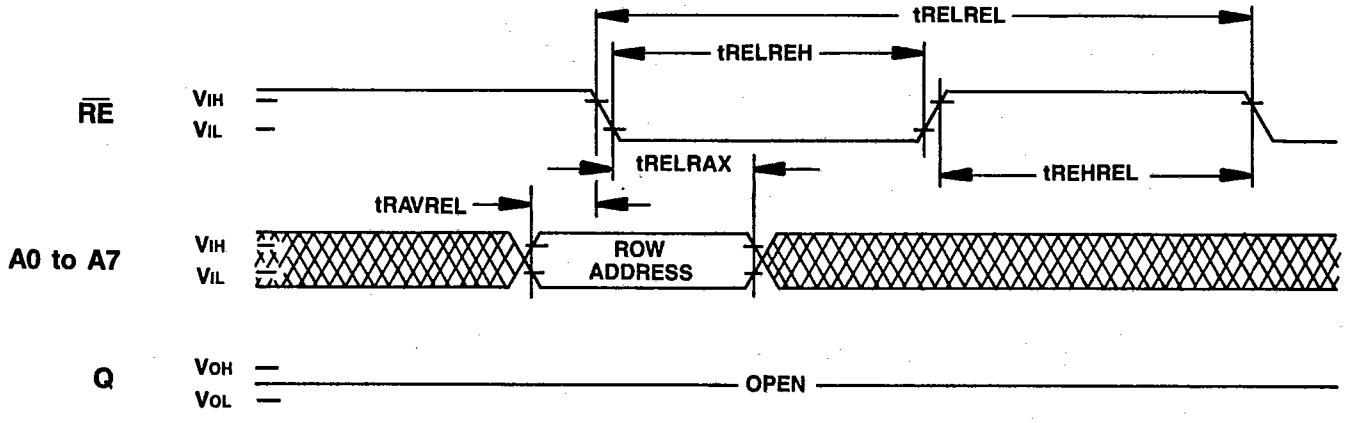
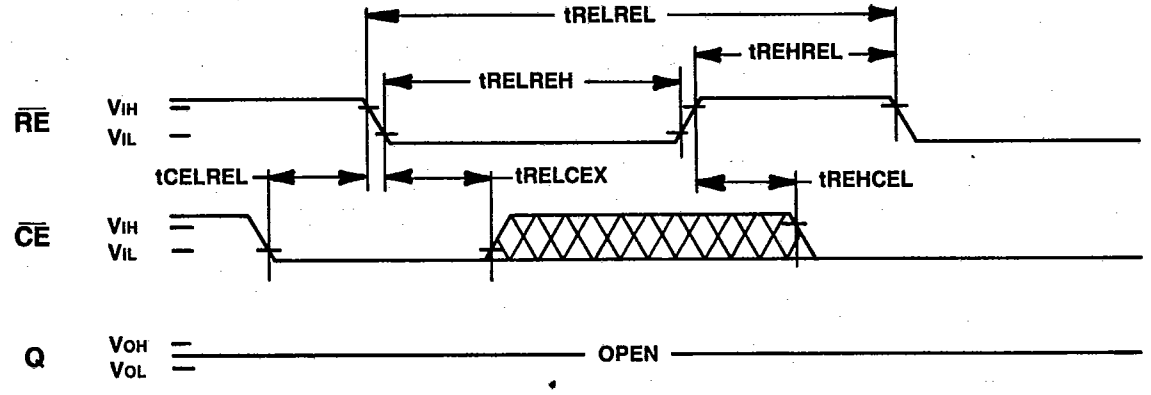


Figure 6. Read-Modify-Write Cycle



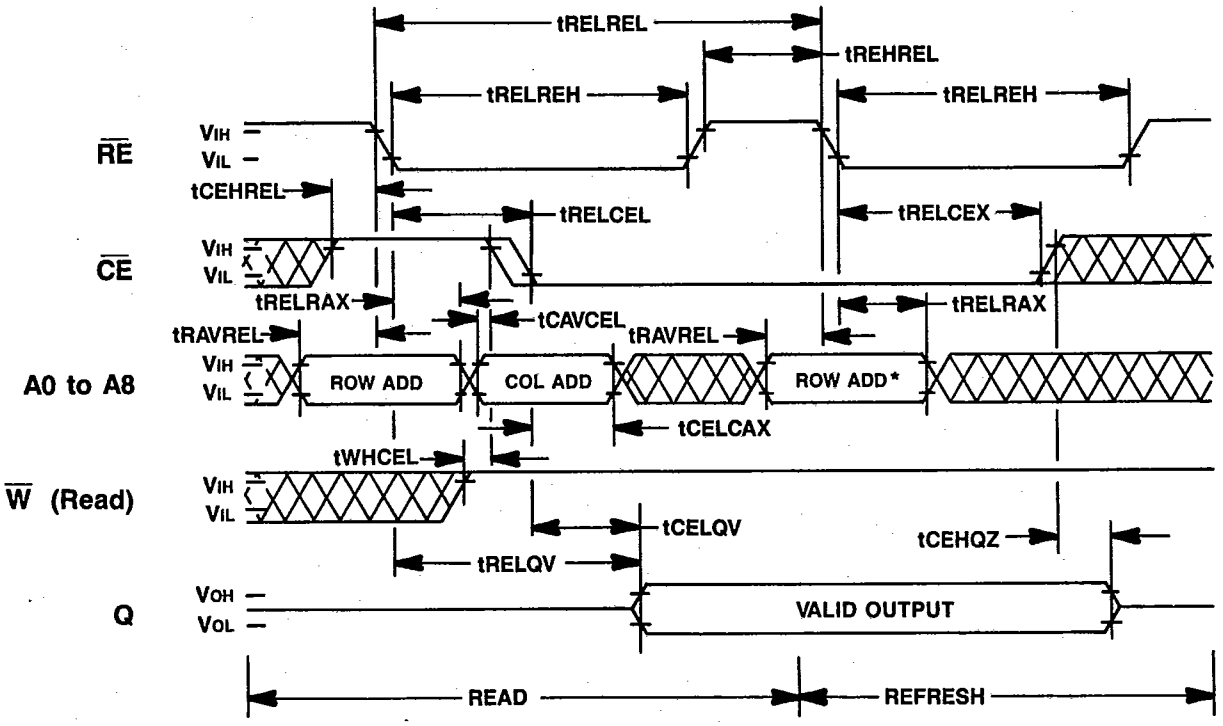
NOTE: Input $\overline{CE}$ ≥ VIH, Input $\overline{W}$ = Don't Care

Figure 7. $\overline{RE}$ Only Refresh Cycle (Note 3)



NOTE: Inputs A0—A8, $\overline{W}$, D = Don't Care

Figure 8. $\overline{CE}$ Before $\overline{RE}$ Refresh Cycle (Available with Nibble Mode Option Only)



* This row address not necessary when using a device with $\overline{CE}$ before $\overline{RE}$ refresh (as available with the nibble mode part).

Figure 9. Hidden Refresh Cycle (Notes 3 & 8)

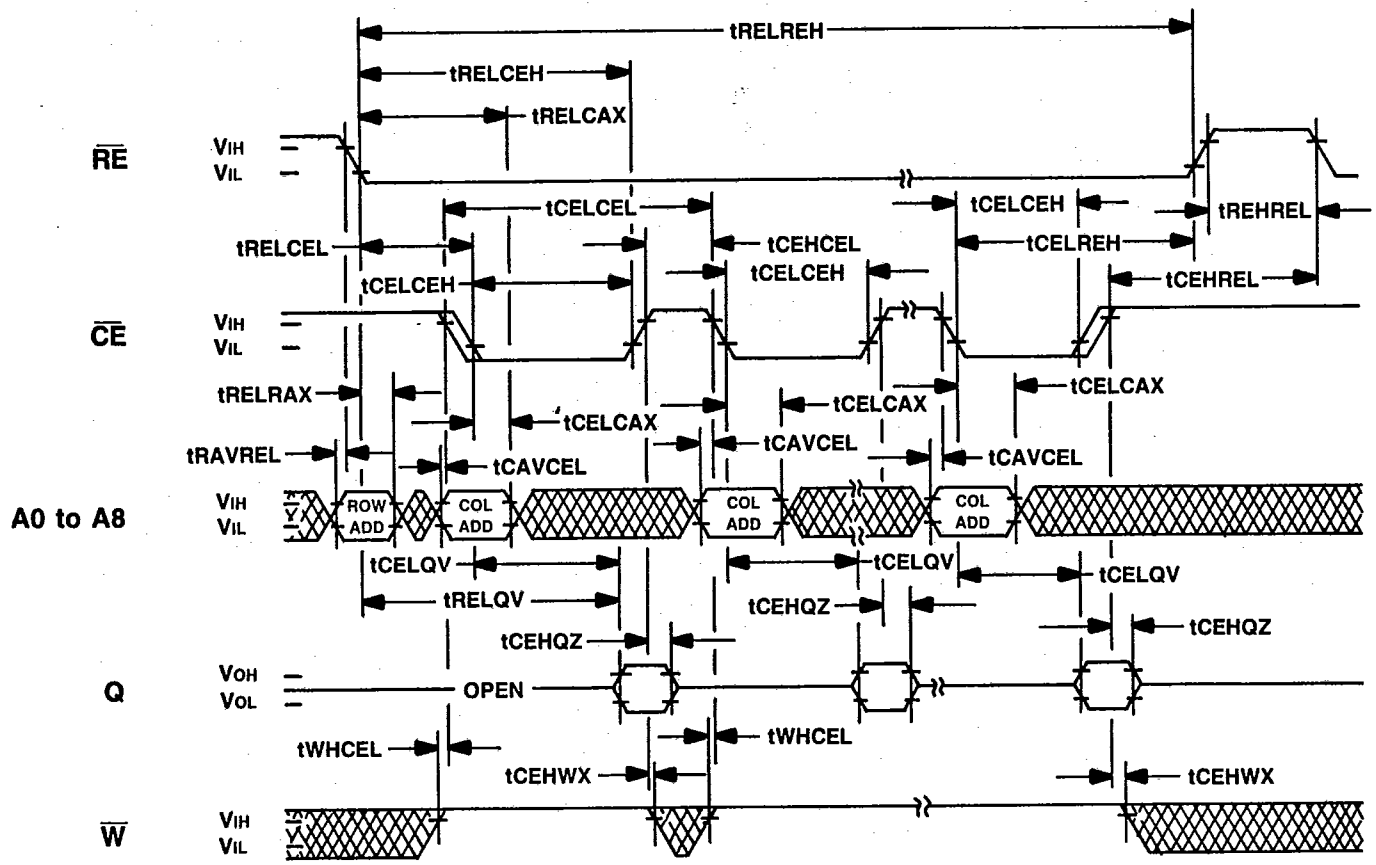


Figure 10. Page Mode Read Cycle

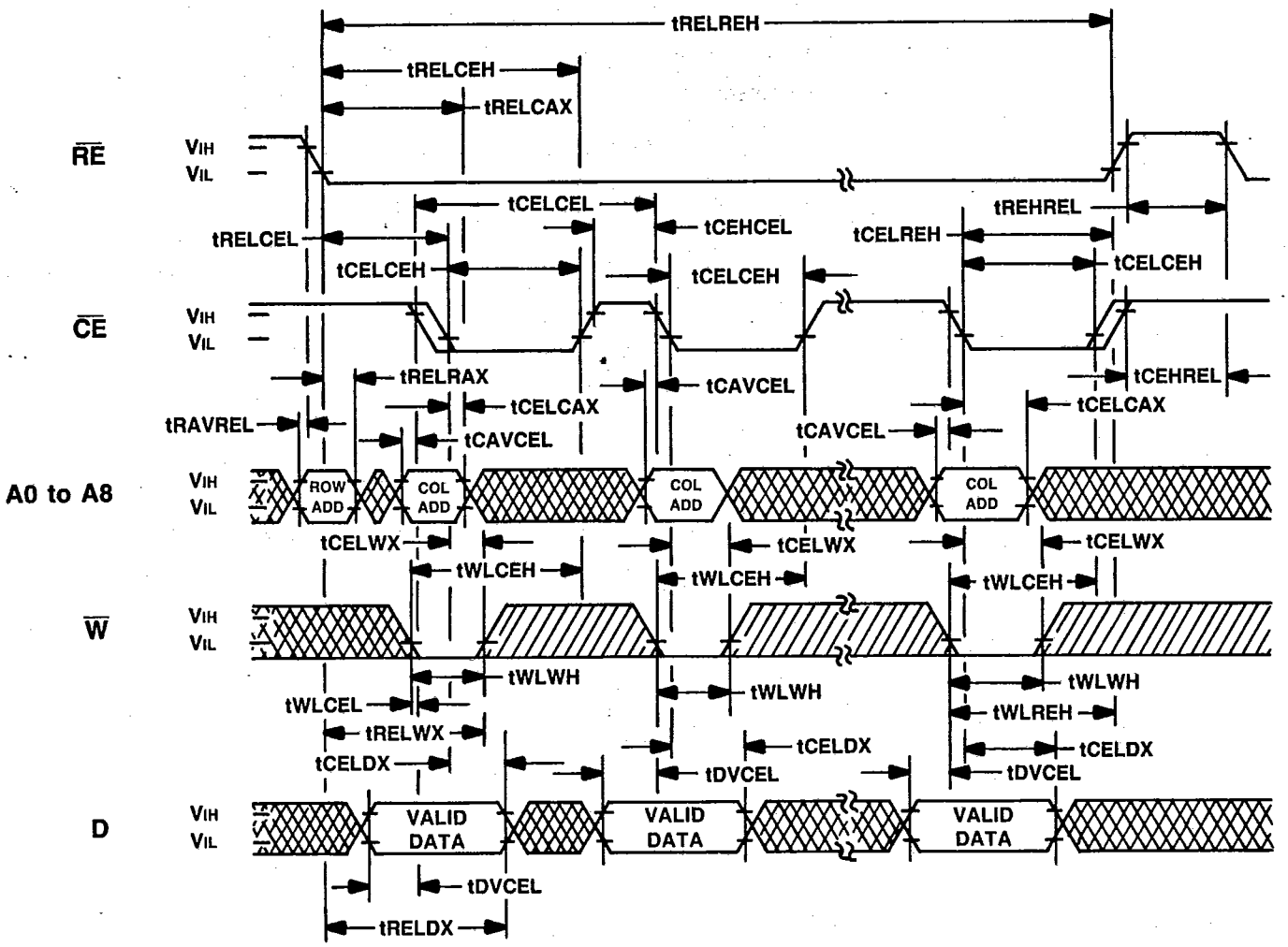


Figure 11. Page Mode Write Cycle

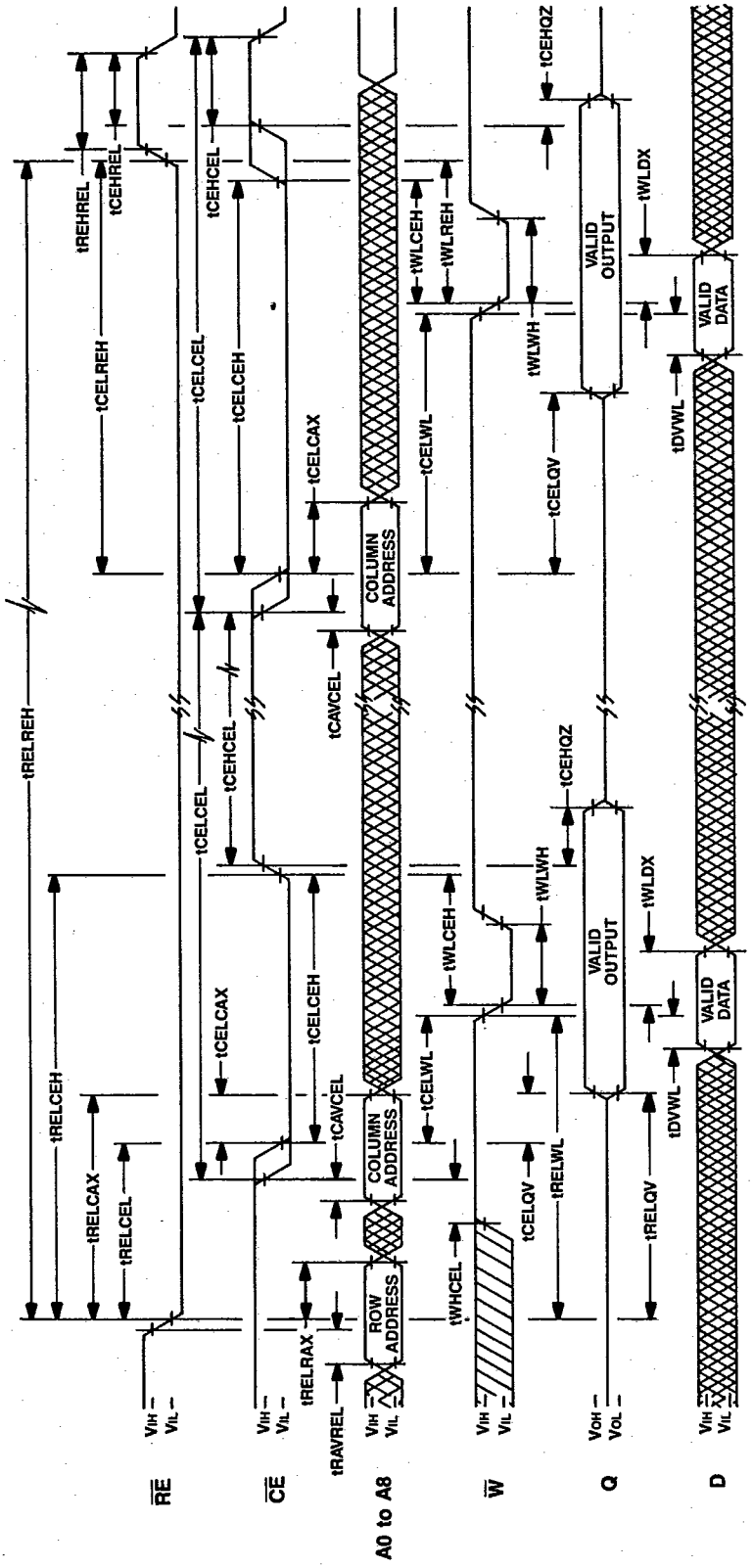


Figure 12. Page Mode Read-Modify-Write Cycle

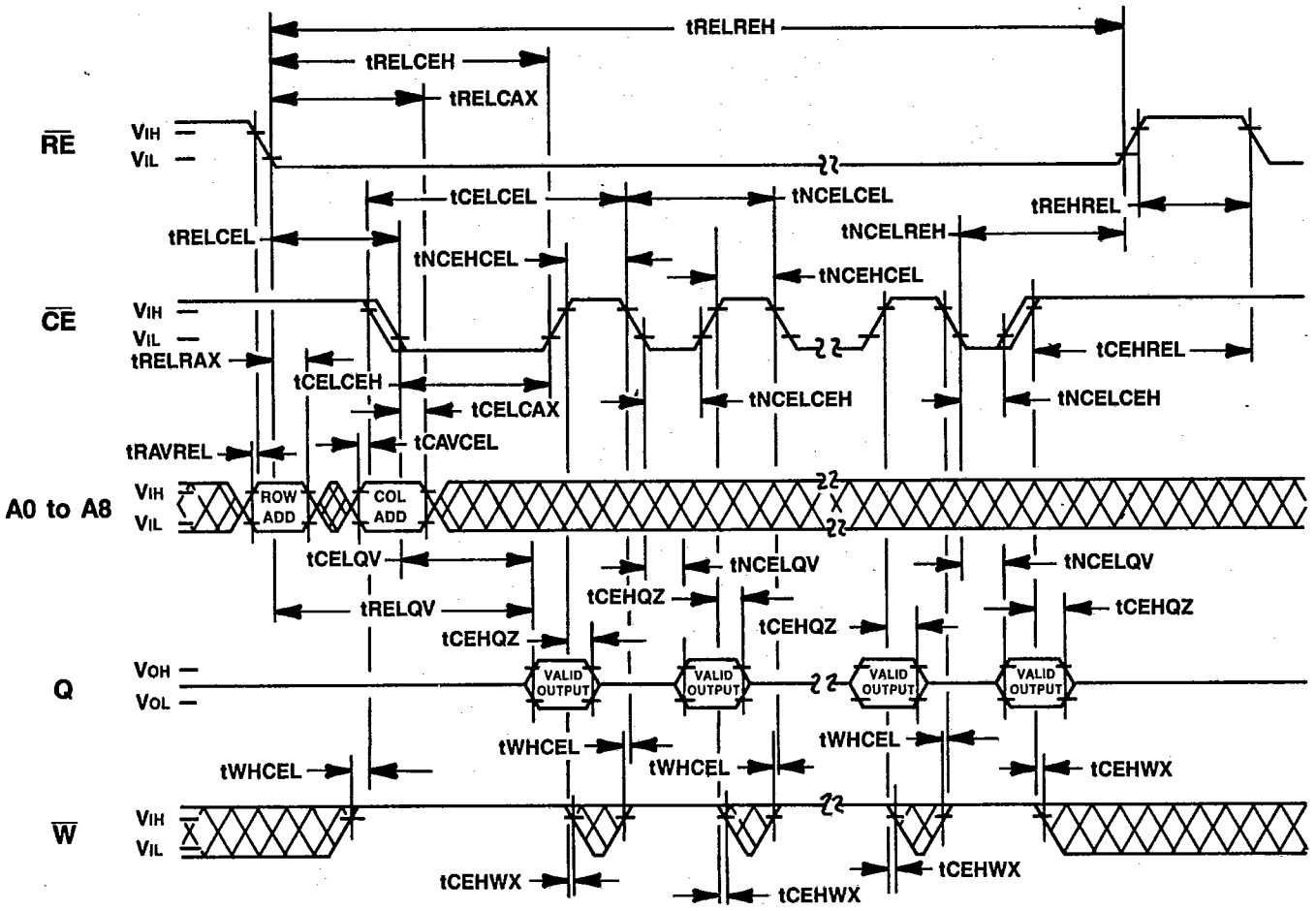


Figure 13. Nibble Mode Read Cycle

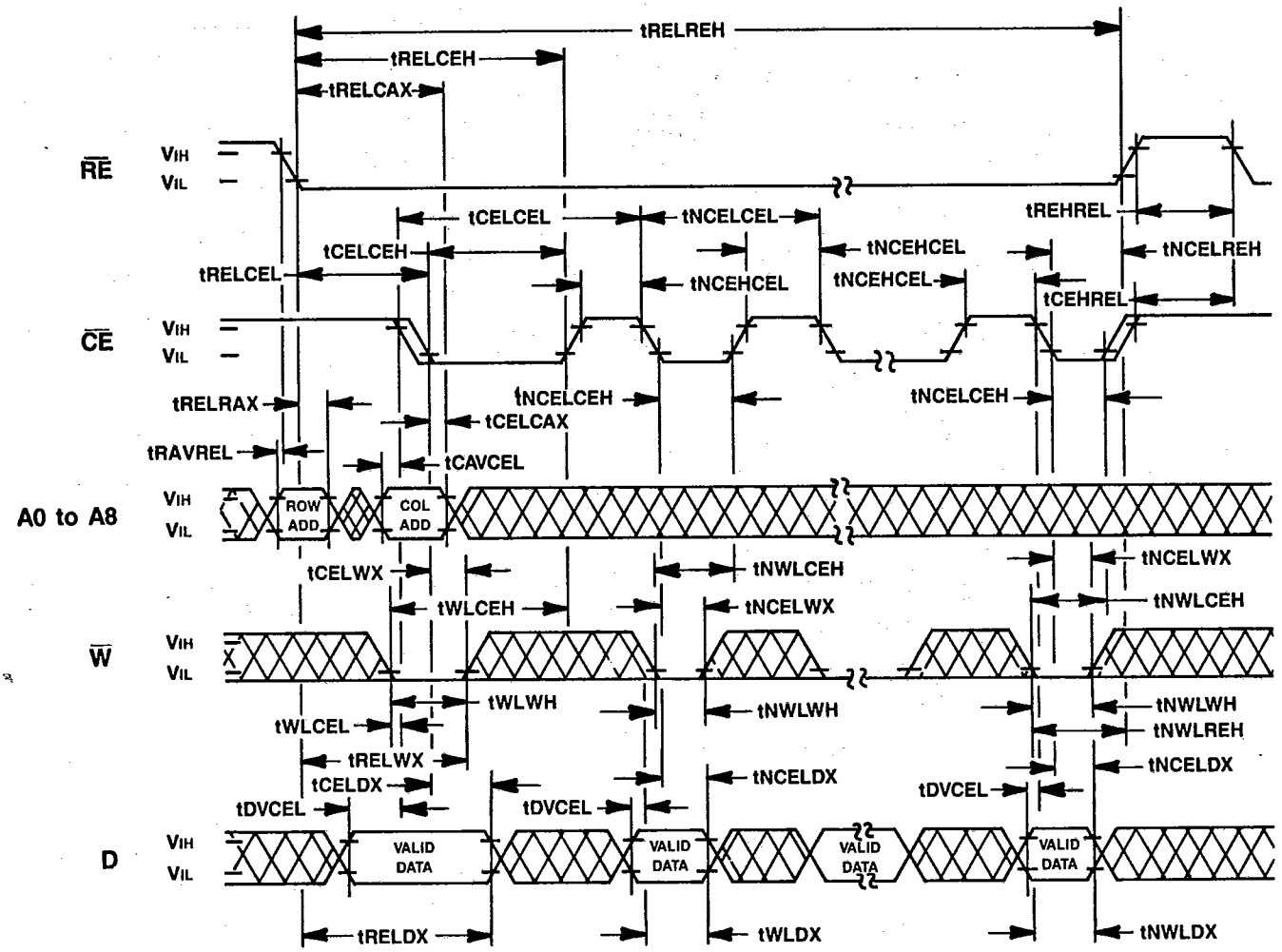


Figure 14. Nibble Mode Write Cycle

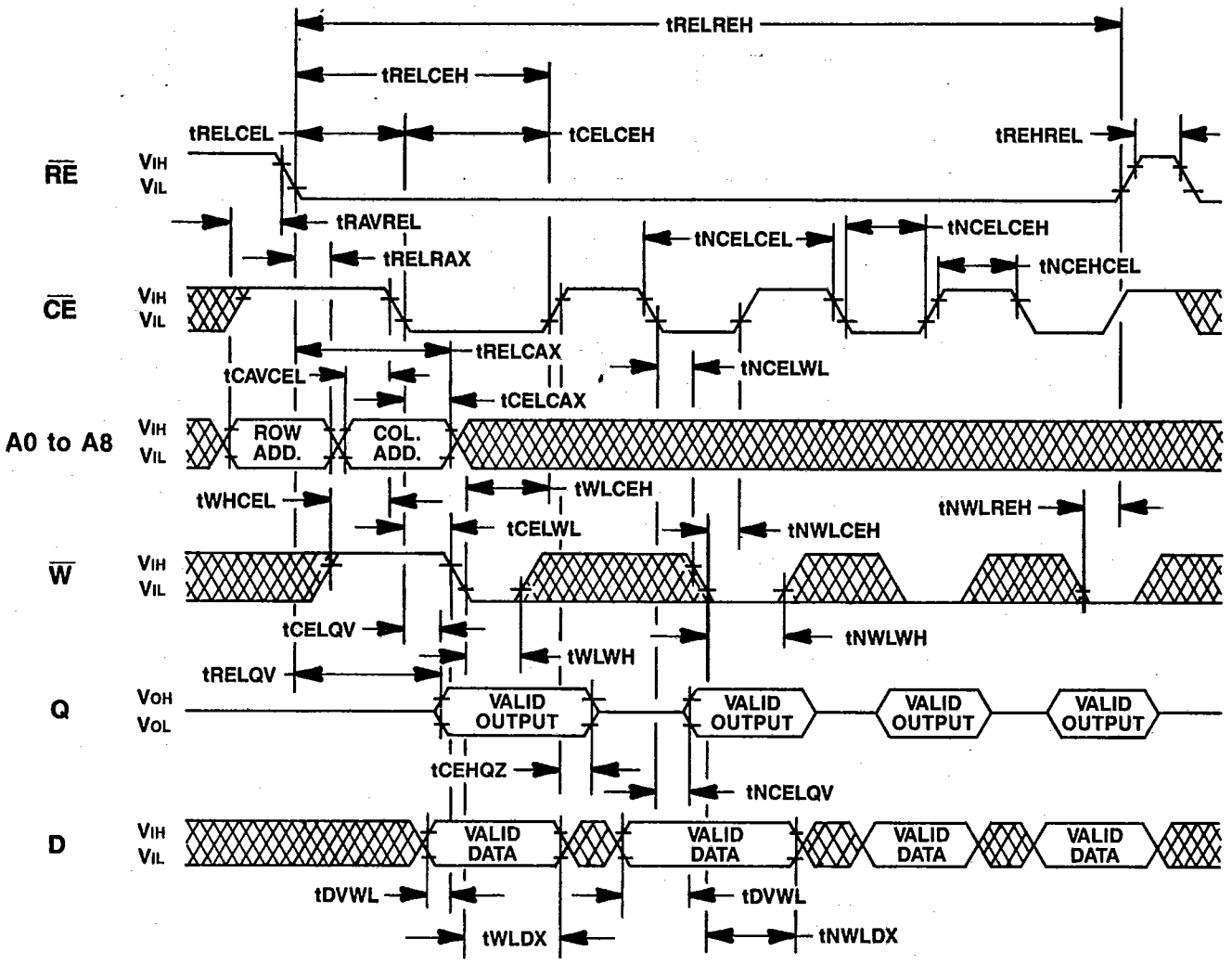
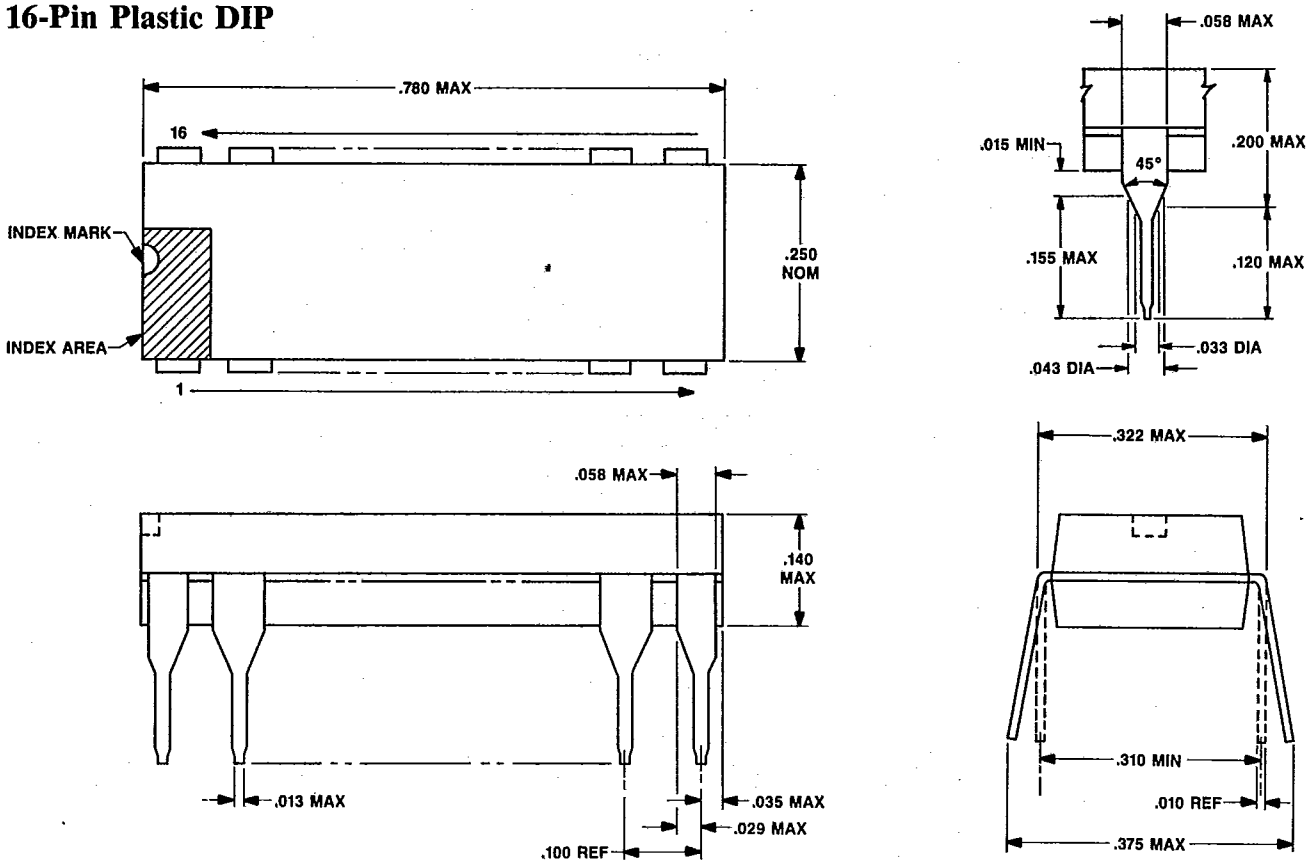


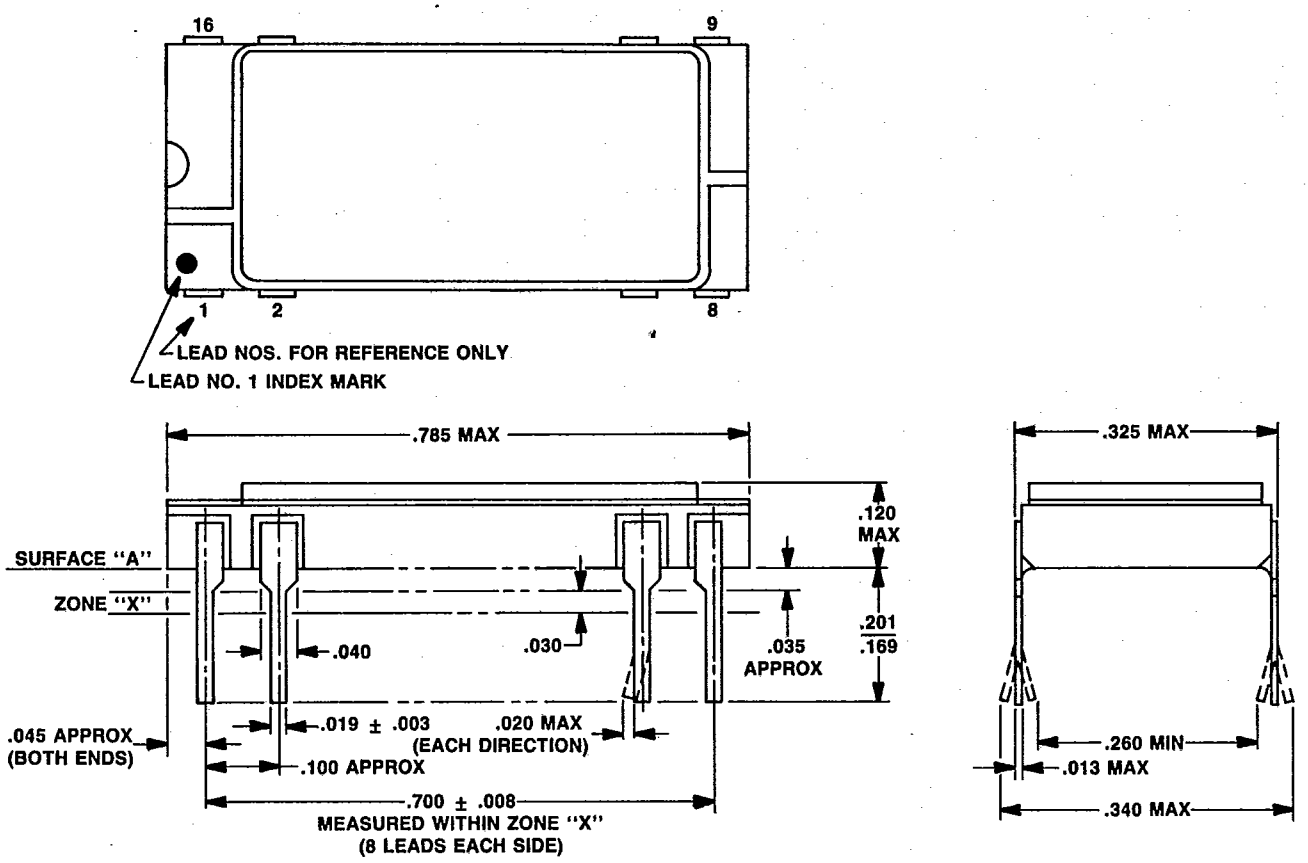
Figure 15. Nibble Mode Read-Modify-Write Cycle

OUTLINE DRAWINGS *(Dimensions in Inches)*

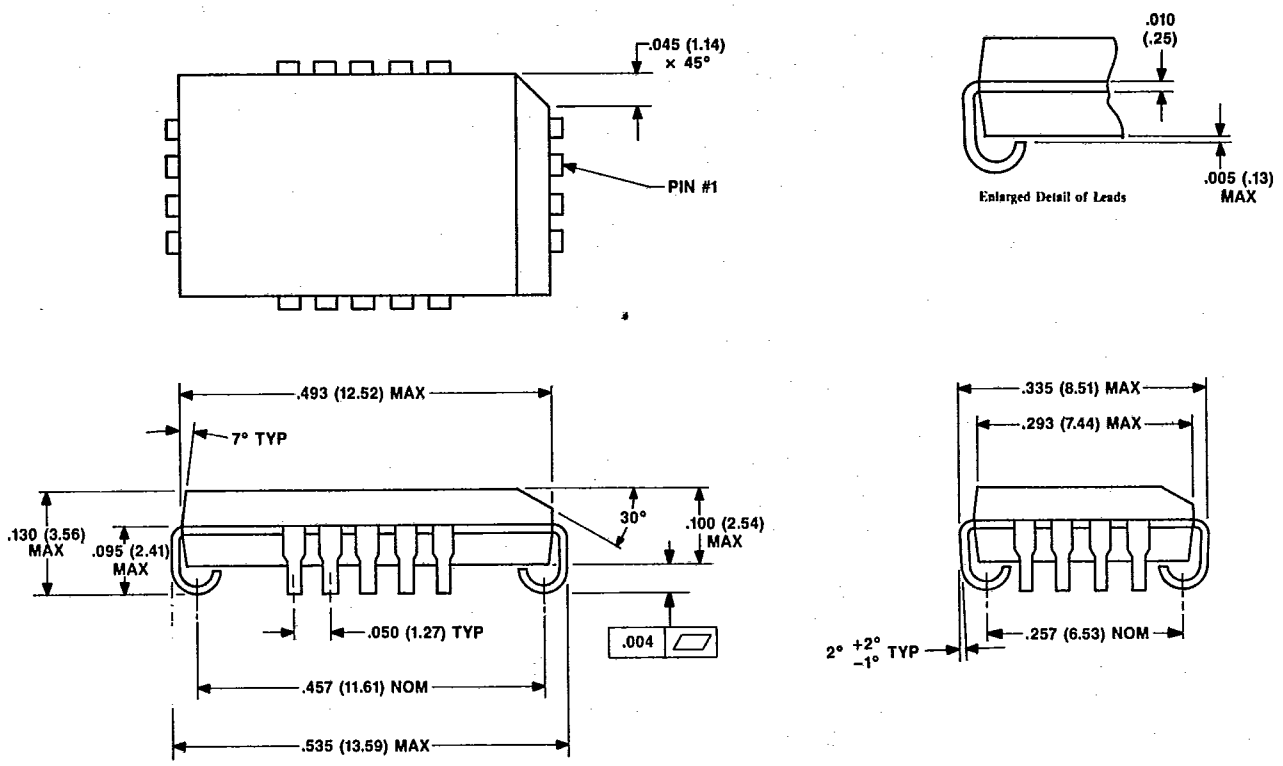
16-Pin Plastic DIP



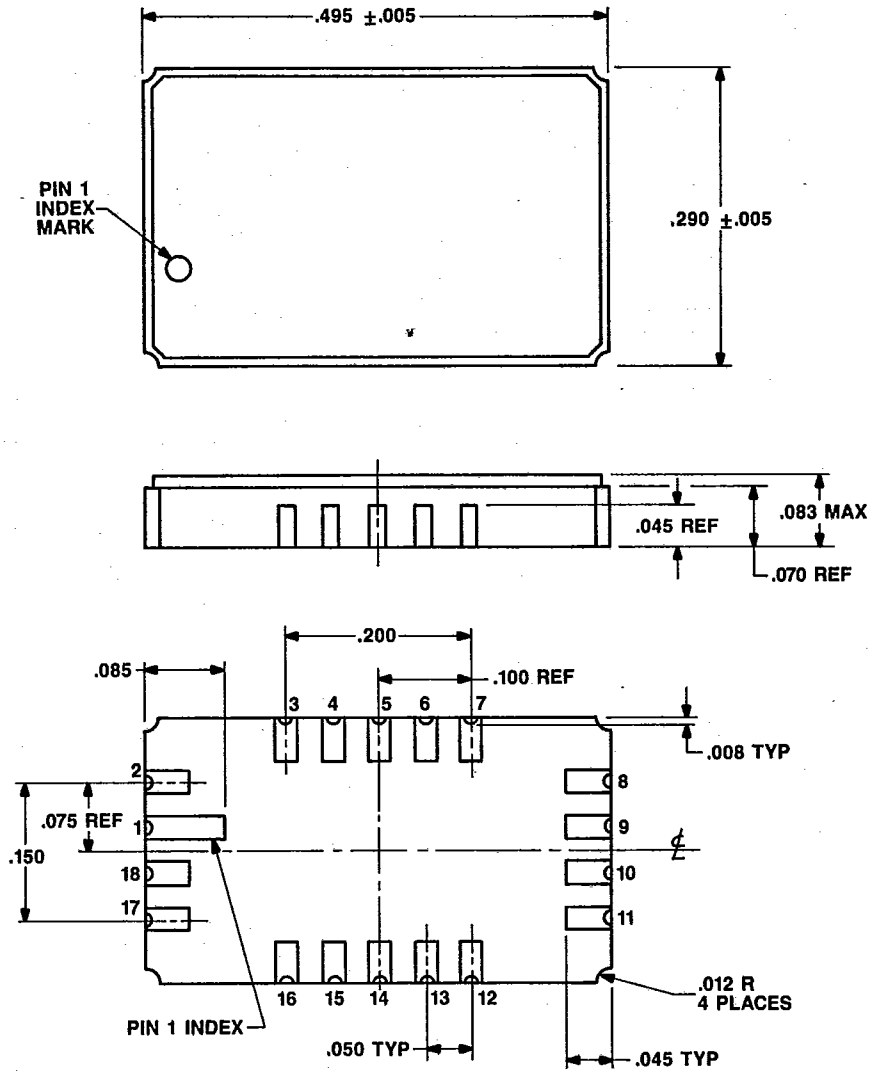
16-Pin Hermetic Ceramic DIP



18 I/O Plastic Leaded Chip Carrier



18 I/O Ceramic Leadless Chip Carrier (Hermetic)



ORDERING INFORMATION

Package	Mode	Part Number	COMCODE
PLCC	Page	M41256DP-10B* M41256DP-12B M41256DP-15B	104382395 104370358 104370366
Plastic DIP	Page	M41256PP-10B* M41256PP-12B M41256PP-15B	104375159 104375167 104375175
Ceramic LCC	Page	M41256CP-10B* M41256CP-12B M41256CP-15B	104382239 104382247 104382254
Ceramic DIP	Page	M41256HP-10B* M41256HP-12B M41256HP-15B	104382320 104375092 104375100
Ceramic LCC	Nibble	M41256CN-10B* M41256CN-12B M41256CN-15B	104382213 104387618 104382221
Ceramic DIP	Nibble	M41256HN-10B* M41256HN-12B M41256HN-15B	104382312 104375076 104375084

* Limited Quantities

T-46-23-15

For additional information, contact your AT&T Account Manager, or call:

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