M100/T102 Test Harness Reference Manual

V3.2

18 Dec 2020

Contents

Document Changes

Date	Version	Changes
11 May 2020	1.0	Original
18 May 2020	1.1	- Added test table - Updated text in Test Coverage section
22 Dec 2020	3.2	- Updated test table to include LCD and keyboard loopback tests. - Amended memory tests to improve failure identification. - Updated board images to the latest versions and added in LCD loopback board.

Welcome to the M100/T102 Test Harness Reference Manual!

Introduction

This document outlines the use of the M100/T102 test harness including how to construct the harness, use the harness to test the Model M100/T102 and items to look for when running tests. The Test Harness runs its own firmware independently of the Model T ROM, therefore it is easily modified to suit your own needs and methods of debugging hardware, everyone works out problems differently so there is some flexibility. The firmware is written using the 8085 Assembly Language and will assemble using the TASM assembler, however it should be straightforward to modify it to run under any assembler. The firmware is not designed to run on the M200.

There are 3 boards in the baseline test harness set: Format 1 ROM board (Rectangular Shape), Format 2 ROM board (T-shape) and Connection test board. The two ROM boards are electrically identical only the format is changed to allow more access to the board motherboard chip set, especially on the M100. NOTE: Only one of the ROM boards is required.

One further loopback board exists to assist in testing the LCD connector on the M100. This board will not work with the T102 as it uses a regular ribbon cable connector.

A loopback cable set can also be constructed to allow the testing of the keyboard connectors on the M100. The loopback cable will not work with the T102.

The test harness firmware provides the ability to test all parts of the model T with the following exceptions:

- Power supply. The power supply section should be operational before testing and producing a good +5V and -5V.
- Modem port. The modem port is not tested however the serial port is tested which is shared with the modem. Tests could be added to test the modem if desired.
- LCD contrast. The contrast control for the LCD is not tested this can only be checked by viewing the screen or checking with a voltmeter. The LCD contrast on the M100 can be tested with the LCD loopback board.
- Low power warning. The low power warning to the 8085 is not tested however the TRAP function is used to turn off the model T if power is removed. If the TRAP is not working then the battery backup feature might fail. This would be shown by the RAM backup test. It is therefore indirectly tested.

References

1. TRS-80 Model 100 Reference Manual, Catalog No. 26-3810
2. TRS-80 Model 102 Reference Manual, Catalog No. 26-3803
3. TASM Documentation.

Test Equipment

The following test/repair equipment is recommended to supplement the test harness.

1. Voltmeter. Used to verify the power supply voltages and battery charge state.
2. Logic Probe. This can be used to check that pins are connected electrically or are changing when a particular test is run. It is also helps if the NOP function is set. Many of the faults on the model T involve corrosion of PCB tracks leading to floating pins on the affected IC.
3. EEPROM Programmer. The programmer is required to load or change the firmware in the onboard EEPROM. The XGecu Programmer TL866II PLUS works well with the test harness.
4. Magnifying glass or loupe. This is useful when inspecting the board for corrosion, broken tracks or poor solder joints.
5. Soldering iron and solder. This can be used to replace or repair parts.
6. Solder sucker. A good quality solder sucker can be useful when removing through hole parts. Extreme care should be taken when de-soldering through hole parts as the holes are plated through and removing the hole plating may disconnect the bottom and top traces causing even more failures.
7. Cassette cable. This is used to test the cassette port on the model T.

Useful additional equipment:

8. Oscilloscope. Although not essential to debug a board it might help with the tracking down failing components and looking at signal failures. A desktop model or unit that attaches to a computer can be used.
9. Logic Analyzer. This might come in useful when verifying some operations but generally should not be needed. Modifying tests on the ROM or other means could be used to track down faults.

Construction

The construction of the boards should be straightforward some of the parts might not be required depending on how the boards will be used. Only one ROM board is required, the choice of the ROM board format is a personal preference.

Consideration should be given to the type of pins etc used to insert into the ROM socket of the M100. They should be considered a consumable item, as they are very likely to break with constant insertion-removal from an IC socket. For this reason the BOM for the ROM boards uses headers to accommodate pins for insertion into the sockets. Female pin headers are then used to insert into the ROM sockets and onto the ROM board. The parts are identified in the Annex C parts list.

The connection test board is powered by the system bus +5V line this should illuminate the power LED when connected correctly. The use of the connection test board is optional however all tests dependent on that board will fail. The serial test port has jumpers for the CTS, DSR, RTS and DTR lines which can be removed during the test to confirm their operation as well as to connect test equipment. Similarly the RX-TX lines are looped back via a header that allows connection to external test equipment.

The remote lead for the cassette cable is plugged into the 2.5mm socket on the test board. It is also connected to one of the onboard LEDs. The LED should blink during the testing as the remote feature is turned on and off.

Loading the firmware onto the ROM board

For any home built test boards the blank EEPROM on the ROM board needs to be programmed with the required test firmware before use. The supplied .ASM file is TASM compatible and uses the 8085 CPU option. It should be possible to use other assemblers with some modification of the directives or label syntax. The assembler should be configured to produce Intel HEX format for loading into the EEPROM programmer. Annex B contains the .bat file used to assemble the test program.

Both formats of the ROM board were designed to minimize their size and allow greater access to the motherboard chipset consequently it is difficult to use the ZIF socket directly on an EEPROM programmer – the PCB blocks the lever on the ZIF socket. If the board will only be programmed once or very infrequently then it is possible to raise the ROM board higher using another socket, the STANDARD ROM option can then be used to program the board. The slide switches should be set to PROG and RUN/PROG.

An alternative approach is to use a ribbon cable fitted with a 28pin IDC DIP header on one end and a 28pin IDC female header on the other. The DIP header is easily fitted into the programmer ZIF socket and the 28pin header can then be plugged onto the male header on the ROM board. This arrangement is very convenient if the board will be reprogrammed frequently during a debug session. The slide switches should still be set to PROG and RUN/PROG.

Configuration

The configuration of the Test Harness only varies slightly for the two supported Model Ts.

M100

The model 100 fortunately has a ROM socket which makes it very easy to insert the ROM test board. However the model 100 has two different ROM socket styles: Original and Standard. The Original format is primarily found on early versions of the M100 they are identified by PLX110CH1X printed on the PCB. This requires the use of the ORIGINAL headers on the ROM board. The Standard format is identified by PLX110EH1X printed on the PCB. This requires the use of the STANDARD headers on the ROM board.

The system bus connection on the model 100 uses a 40pin DIP IC socket. This connection will require the use of a 40pin DIP IC header to 40pin header. The ribbon cable can be a simple straight through connection without any need to twist the cable as is normally required for connection to a DVI unit.

The remaining connectors are straightforward connections to their respective ports.

The WR- line on the ROM board has to be connected to M20/Pin 7, this is the buffered WR- line from the 80C85.

Two optional test units are available for the M100: LCD Loopback PCB and Keyboard cable loopback. The LCD loopback PCB plugs into the LCD cable header and provides easy access to the header pins for signal probing. The PCB also contains three LEDs that indicate the status of the +5V, -5V and LCD contrast (V2) lines. The +5V and -5V lines should illuminate brightly, if they are dim then these power lines need to be checked for the correct voltages. The brightness of the LCD contrast LED is determined by the LCD contrast control. The brightness should vary from off to nearly as bright as the -5V light when the contrast is adjusted. If the LED fails to change brightness as the LCD contrast if varied then the V2 line needs to be checked. Often the line has been corroded by the leakage of C82. The LCD loopback board can only be used on the M100.

The keyboard loopback cable is designed to plug into CN1 allowing the testing of the keyboard section without a working keyboard. Take care inserting the loopback cable, as the connectors are not symmetrical. The connector connects PIO pins PA0-PA7 to KR0-KR7 so the whole motherboard path can be tested. It does not test PIO pin PB0 to the connector, although this pin is tested in the LCD test, if there is corrosion or cable breakage on the keyboard module then the SHIFT, CTRL, BREAK, CAPS, NUM, CODE or GRPH keys might not work when the keyboard is reconnected – these keys are driven by PB0. If this situation occurs then inspecting the traces is warranted. The keyboard diagram in the reference manual can help in tracking down broken connections. The cable can only be used on the M100.

T102

The model 102 is slightly more difficult to work on as it must be removed from the case and spread out in order to access the ICs which are on both sides of the motherboard. This can make it awkward to connect the ROM board and the

required jumpers to make the ROM board operational. Take great care not to damage either the LCD screen or keyboard flat flex cables it is very easy to crack the copper traces inside the cables or rip off the edge fingers when inserting the cables into their sockets. New flat flex cables are not readily available for these two units breaking the trace in a cable may therefore require other means to connect the screen or keyboard. The LCD screen and keyboard do not need to be attached when testing, their tests will show as fail but the rest of the tests will run.

The model 102 unfortunately does not use a ROM socket (unless it has been modified) this means that IC test clips are needed to clip onto the T102 ROM. The header on the ROM test board can be used to connect to the IC test clip via Dupont cables. In addition the CS- line (pin 20) to the ROM needs to be cut in order to disable the onboard ROM and allow the ROM board to take over the motherboard. The track near the pin can be cut and repaired very easily. The T102 ROM is a standard ROM so that is the only option available for this machine. The T102 PCB is stamped with PLX120CH1X just for confirmation. NOTE: The IC test clip can be any size greater than 28pins, there is plenty of room for the clip to overhang the board.

The system bus connection on the model 102 is found on the rear of the unit and the connection test board can be plugged directly into this port. There is no need to make a cable. However because of how the model 102 is configured the board might have to be inserted “upside down”. It also depends on how you wish to work on the 102 having the board over and open box with the IC test clip downwards helps access to the other side of the board.

The remaining connectors are straightforward connections to their respective ports from the connection test board.

The WR- line on the ROM test board has to be connected to M20/Pin 3, this is the buffered WR- line from the 80C85. The CS- line on the ROM test board has to be connected to M5/Pin 4 in order to allow access to the ROM on the test board.

Prerequisite

The following items need to be considered before using the ROM test board.

- Power supply operational. Before running the test harness it is important that the power supply is working correctly.

- Recap. As the boards to be tested are over 35 years old it is very likely that some or all of the electrolytic capacitors are bad. It is recommended that at least the caps listed in Annex A are replaced before testing further. This might actually resolve many issues on the board.

- Replace NiCd battery. If the backup NiCd battery has not been replaced it is very likely bad and should be replaced as a matter of course. It can be replaced with a NiMH battery of the same style. Or in some cases it could be replaced with a Supercap. The Supercap will not last as long as a NiMH battery but should give

sufficient time to change the AA batteries. The boards can run without the backup battery so it could be disconnected and left out during testing. NOTE: Without the backup battery it will not be possible to test SRAM data retention.

Hints and tips for debugging M100 and T102 motherboards

The following section gives some insight into things to look for when debugging M100 and T102 motherboards.

- The M100/T102 boards were occasionally not washed properly after manufacture leaving solder flux on the board. Over the years the solder flux will sometimes corrode copper tracks causing breaks in the connections. When inspecting a board look for flux that has not been removed and check for continuity of the traces. This effect seems to occur most around connectors or sockets where solvent and flux can become entrapped. The trace might look OK however the copper has usually been transformed into an open trace.

- On the M100 motherboards there can be dry solder joints that may fail over time. The bad joints usually have a silver crystalline appearance or may show as ring breaks. Reheating the bad joint with fresh solder will usually fix this problem.

- On the M100/T102 boards some of the traces are very fine and can be over etched cause the traces to break particularly around through-hole components. Take care when handling boards so as not to flex them too much.

- The Electrolytic caps will fail over time and can either leak or outgas onto the board. If the caps leak their chemicals can easily destroy nearby copper traces causing them to become open circuit (e.g. C82 on the M100 can corrode the V2 line to the LCD causing the LCD to fail). Again the trace could appear as a copper trace but it might have become a non-conductive trace. This is a particular problem in the power supply area where important traces run under or near the caps. Therefore it is imperative to clean the area under the cap and inspect for damage. Outgassing can cause corrosion of nearby parts but generally this does not have much of a severe impact on the board however it could damage the LCD screen or keyboard near those parts.

- Battery acid leakage on the motherboards is a big problem in some cases. Generally this can be more severe on the T102 motherboards as the battery box is attached directly to the board. The acid damage is very difficult to deal with and cleaning the board can simply reactivate the acid causing more damage. Any gas from the acid can also damage nearby components such as the LCD display edge connector or the LCD panel itself. Various options can be used to clean the board if the leak is alkaline then vinegar could be used to neutralize the residue and clean the board. Test on a small portion of the board first to check it does not further damage. Make sure to take care when handling contaminated boards.

Test Coverage

The following table lists the tests in order of application. It also highlights the area or chips being tested.

If a test fails the remaining tests should be allowed to execute as this may shed more light on the location of the fault condition. Observing which tests fail can help to isolate the problem area or part. For example if the OPTROM, LPT, CLK IC and REMOTE test fail this could indicate problems with the M14 'h175 latch. This could be the CS- line, RESET- line or M14 itself.

If the CLK IC (M18 uPD1990AC) has failed either it is not running or not generating the TP signal then the Keyboard test and Cassette tests might not work correctly.

If there is no good SRAM then the tests terminate as RAM is required to run the remainder of the tests.

Test Name	Example Screen Display	Description	M100 Coverage	T102 Coverage
CPU	CPU	The first test simply confirms the CPU and the identified ICs are functional by writing to the diagnostic screen (DS). If the 'CPU' text does not appear then the first area to check is the CPU area.	RESET circuit M19 – 80C85 M21 – 'H244 M20 – 'H244 M2 – 'H245 M1 – 'H373 M5 – H139 (1,2,3,4) M12 – ROM X2 - XTAL	RESET circuit M19 – 80C85 M21 – 'H244 M20 – 'H244 M2 – 'H245 M1 – 'H373 M5 – H139 (1,2,3,4) M12 – ROM X2 - XTAL
RAM 1st line	CPU RAM? .mggBmggBFggBmgg	The RAM tests are broken into several parts to focus on different parts of the RAM modules. For the M100 each RAM module is made up of 4 x 2K blocks so there could be individual failures that might go undetected with tests for an 8K block. The first line of the screen provides information on the four RAM modules. Each module accounts for 4 characters they are sequenced: 3, 2, 1 and 0. There are four tests in part 1 as follows: 1. Battery backup. This is only valid if the test has been run once and the unit power cycled. The test looks for a specific pattern at a certain address to see if the memory has been retained. If successful the DS will show 'B' for that module, or a '.' if the test fails. 2. Complete RAM write-read test. Each location is written to and read back with a sequence of pre-stored patterns. Any location that fails to read back correctly stops the test and will cause an 'F' to printed on screen. If the RAM passes then 'm' will be printed. This test may take a while to run if the RAM is good.	M6 – RAM M7 – RAM M8 – RAM M9 – RAM M3 – 'H138 M4 – 'H138 D22 – Diode, as part of the VB battery backup operations	M6 – RAM M7 – RAM M8 – RAM M9 – RAM M5 – 'H138 M37 – 'H00 (8,9,10,11,12,13) M27 – 'H11 (4,5,6) D22 – Diode, as part of the VB battery backup operations

Test Name	Example Screen Display	Description	M100 Coverage	T102 Coverage
		3. First page RAM test. This test writes 1..255 into the first 255 locations in order to test the address selection for the RAM module and that each location is uniquely addressed. If the test passes it will print 'g', a failure will print an 'H'. The test is checks the first 2K byte SRAM is correctly receiving data. It is primarily to exercise the data lines. It is possible for the first 2K module to be good and the remainder to be bad so this test alone should not be used to determine if the SRAM module is good. 4. Address line test. This test checks each of the A0..A8 address lines to make sure they are operational. If the test passes it will print 'g' otherwise it will print a number to indicate which address line has failed (e.g. 1 = A0). It should be noted that failed lines may mask other failures.		
RAM 2nd Line	.mggBmgg.FH0Bmgg mmmmmmmm9ABCmmmm	Part 2 of the RAM tests exercises address lines A8-A14 of the SRAM array. The M100 and T102 differ in the organization of their respective SRAM. The M100 uses16x2Kbyte RAM modules if all the SRAM is present. The T102 uses 4x8Kbyte RAM modules if all the SRAM is present. Therefore the results from the test require a slightly different interpretation when failures are reported. **M100**: The M100 uses 16 chip enable lines (CE1-CE16) to control each 2Kbyte SRAM. Each CEx is driven from either M3 (CE1-CE8) or M4 (CE9-C16) they are in turn controlled from M5. M3 and M4 are under the control of A11-A13 and M5 is under the control of A14-A15. This test exercises each of the address lines A8-A14. If testing address lines A12-A14 highlight faults these will show as CEx failures and the 2nd line of the DS will display the failing CEx line numerically from 1 – G => CE1 – CE16. This may indicate a fault in the respective decoder or SRAM chip. If address lines A8-A10 highlight a fault then they will show as J,K or L respectively. If the module is good then 'm' is displayed. In the example left RAM module 2s (if present) CE9, C10, CE11 and CE12 have failed. **T102**: The T102 uses 4 chip enable lines (CE1-CE4) to control each 8Kbyte SRAM chip. The CEx lines are driven by M5 controlled from A13-A14. As the firmware cannot detect the type of motherboard being tested the results assume it is an M100 therefore the test results will not directly map to the T102 hardware. If A8-A10 have failed then they will still show J, K or L to indicate the problem. The address lines A11-A14 can be mapped as follows: A11 -> 2, 4, 6, 8, A, C, E or G. A12 -> 3, 7, B or F. A13 -> 5 or D. A14 -> 9. An indication of 1, 5, 9 or D would more likely indicate a CEx failure.	M6 – RAM M7 – RAM M8 – RAM M9 – RAM M3 – 'H138 (Y0-Y7) M4 – 'H138 (Y0-Y7)	M6 – RAM M7 – RAM M8 – RAM M9 – RAM M5 – 'H138 M37 – 'H00 (8,9,10,11,12,13)

Test Name	Example Screen Display	Description	M100 Coverage	T102 Coverage
PIO	PIO ABC PASS	The PIO test checks that the Port A and Port B registers can be written to and read from using the same test pattern as that used for the RAM tests. In the case of Port B the power off bit is masked so it does not turn off the machine! If either Port A or Port B fails then further testing is aborted as all other parts of the M100/T102 rely on the PIO to operate. In this case the test program will display four options a Port A write of 00H and FFH and the read back and the same for Port B. The test will then halt the CPU. If Port A and Port B test out successfully then Port C is read and the status of the LPT busy lines checked. If this fails then the PIO test fails. The other lines associated with Port C are tested in their relevant sections. The timer portion of the PIO is tested when the serial port is tested. The control register can only be indirectly tested however if subsequent tests fail then it can be assumed that the PIO has a problem. The problem could be a failed IC or failed traces on the board due to corrosion.	M25 – 81C55 M16 – ‘H138 (Y3) Registers tested and lines into 81C55. The Port A, B and C output lines are not tested by this test except indirectly via the data written to the ports.	M25 – 81C55 M16 – ‘H138 (Y3) M17 – ‘H00 (1,2,3) Registers tested and lines into 81C55. The Port A, B and C output lines are not tested by this test except indirectly via the data written to the ports.
LCD Tests		There are two options for testing the LCD on an M100: Use of the LCD panel or Loopback PCB. The firmware automatically detects whether or not the LCD is looped back.		
LCD Present	PIO ABC PASS LCD IU LCD OK?	The screen should be observed during this test run. The LCD is first checked by initializing the column drivers, this involves resetting them via software, setting the counters for up mode, turning on the screen and checking the busy bit clears. If the initialization is successful then ‘I’ is printed on the DS. If the column drivers are set to up mode then ‘U’ is printed on the DS. If one or both of these operations fail then ‘FAIL’ is printed on the DS. The failure could occur if the screen is disconnected or faulty. If the screen passes initialization then it is cleared by printing ‘X’ to all locations. After which each of the 8 lines is printed with text. The screen should show no missing pixels, blank lines or rows. This is a visual check, as the hardware cannot directly test the LCD panel is working.	M25 – 81C55 (Port A, Port B [PB0, PB1]) M17 – ‘H00 (1,2,3,8,9,10,11,12,13) M16 – ‘H138 (Y7)	M25 – 81C55 (Port A, Port B [PB0, PB1]) M17 – ‘H00 (4,5,6,11,12,13) M16 – ‘H138 (Y7)
LCD Loopback 1 (M100 Only)	DNGL-AD7-0 PASS	M100 ONLY The first screen of the LCD loopback test is for the data lines. All the data lines are tested. If all tests pass then ‘PASS’ will be displayed. If a test fails then the 2nd line of the DS will display the data written and the data read back for the failed test. From this data it should be possible to determine which data line is not being correctly driven to the LCD.	M25 – 81C55 (Port A, Port B [PB0, PB1]) M17 – ‘H00 (1,2,3,8,9,10,11,12,13) M16 – ‘H138 (Y7)	N/A

Test Name	Example Screen Display	Description	M100 Coverage	T102 Coverage
LCD Loopback 2 (M100 Only)	DNGL-C20-27 PASS	M100 ONLY The next screen of the LCD loopback test is for CS20-27. All the CS lines are tested. If all tests pass then 'PASS' will be displayed. If a test fails then the 2nd line of the DS will display the data written and the data read back for the failed test. From this data it should be possible to determine which CS line is not being correctly driven to the LCD.	M25 – 81C55 (Port A, Port B [PB0, PB1]) M17 – 'H00 (1,2,3,8,9,10,11,12,13) M16 – 'H138 (Y7)	N/A
LCD Loopback 3 (M100 Only)	DNGL-C28-29 PASS RST 1 CS28-29 3	M100 ONLY The next screen of the LCD loopback test is for CS28-29. Both CS lines are tested. If all tests pass then 'PASS' will be displayed and the 2nd line will display the status of the RESET line, which should always be 1 and the state of CS28-C29 which should be 3 at the end of the test. Alternatively if a test fails then the 2nd line of the DS will display the data written to CS28-29 and the data read back. From this data it should be possible to determine which CS line is not being correctly driven to the LCD.	M25 – 81C55 (Port A, Port B [PB0, PB1]) M17 – 'H00 (1,2,3,8,9,10,11,12,13) M16 – 'H138 (Y7)	N/A
CLK	01001115350 PASS 01001115356	The clock IC is tested by initializing it with a pre-stored date and time. The IC is then allowed to run for ~6 secs and read back. The new time is compared to the old time and if the new time is more than 6s from the start time the test is successful and 'PASS' is printed on the screen. Otherwise 'FAIL' is printed.	M25 – 81C55 (37, PA0-PA4) M18 – uPD1990AC M14 – 'H175 (10) M13 – 'H32 (4,5,6) M16 – 'H138 (Y6) X1 – XTAL	M25 – 81C55 (37, PA0-PA4) M18 – uPD1990AC M14 – 'H175 (10) M26 – 'H32 (8,9,10) M16 – 'H138 (Y6) X1 – XTAL
RST 7.5	01001115356 05 01001115401 PASS	The RST7.5 interrupt is driven by the TP output from the clock IC to provide the regular 'tick' for the model T. Once the clock IC has been configured in the previous test the RST7.5 interrupt is enabled and the number of 'ticks' is counted over a set period. The period is determined by software delay loops. In this case it is set to 6s. If the required number of 'ticks' occur in 6s then the test is considered to have succeeded and 'PASS' is printed on the DS, if not then 'FAIL' is printed.	M18 – uPD1990AC (TP) M19 – 80C85 (7)	M18 – uPD1990AC (TP) M19 – 80C85 (7)
Serial Port Pt 1	CTRL BITS PASS RT/CT 1 DS/DT 1	The serial port is tested in two parts using the connection test board. The first part of the test confirms that the RTS, DTS, DTR and DSR lines toggle. The RTS and CTS lines are looped back as are the DSR and DTR lines. First the lines are set to 1 and then 0, each time the looped back line is checked to confirm the value. If the values are good then the test is successful otherwise the test fails and the DS will show which line(s) have failed in the loopback. Subsequent testing could be done to cross link to the other lines and see where the fault goes to isolate the problem. For example link RTS-DSR and CTS-DTR and see which line is faulty. Further testing might be required to determine which part is faulty.	M35 – 4904 (3,4,5,6,8,9,10,11) M25 – 81C55 (2,5,32,35,36) M33 – 'H157 (5,11,7,9) M24 – 'H32 (8,9,10) M34 – 4904 (1,2)	M25 – 81C55 (2,5,32,35,36) M33 – 'H157 (5,11,7,9) M24 – 14584 (8,9,12,13) M35 – 14584 (3,4,5,6,8,9,10,11) M38 – 'H02

Test Name	Example Screen Display	Description	M100 Coverage	T102 Coverage
		The test also tests the PIO Port C pins related to CTS (PC4) and DSR (PC5), plus the PIO Port B pins RTS (PB7) and DTR (PB6)		(8,9,10,11,12,13) M34 - 14584 (10,11)
Serial Port Pt 2	LOOPBACK PASS C 04 TX 00 RX 00	The second part of the serial test involves a loop back of the TX and RX lines. In this test 256 bytes from 0 to 255 are transmitted and received. If any byte does not check then the test fails. This test uses the RST6.5 interrupt to run the test. In addition the PIO timer register is configured for 19,200bps as well as configuring the IM6402 for 8bits + No Parity + 1 stop. The TX pin could be monitored externally to verify the functionality. PIO pin PB3 is used to control the switch to the RS232 port from the modem. The bottom line of the DS shows the TX and RX byte being sent/received. The C value is that read from the serial comms register M23 (M100/T102).	M35 – 4904 (1,2,12,13) M25 – 81C55 (32) M33 – ‘H157 (2,4) M24 – ‘H32 (11,12,13) M34 – 4904 (1,2) M23 – ‘H244 (4,6,11,13) M22 – IMS6402 M26 – ‘H02 (11,12,13) M16 – ‘H138 (Y5,Y7)	M35 – 14584 (1,2,12,13) M24 – 14584 (10,11) M25 – 81C55 (32) M33 – ‘H157 (2,4) M23 – ‘H244 M4 – ‘H244 M22 – IMS6402 M38 – ‘H02 (4,5,6) M16 – ‘H138 (Y5,Y7) M34 – 14584 (10,11)
System Bus	SYS BUS PASS WR 00 RD 00 S 7F	The System Bus test simply writes/reads a sequence of patterns to one address on the system bus. It is a basic loopback test. If all the bytes are successfully written/read the test is successful otherwise it fails. The lower line of the DS indicates the progress of the test by showing the byte being written/read. The S portion of the lower line shows the state of the 4 DIP switches on the header board. This is another address on the header board that effectively tests the A0 and A1 lines. The DIP switches could also be used to change the tests etc during a run if required. Currently they are ignored by V2.5, although changing their value during the test will be reflected on the DS.	M10 – Sys bus SKT M16 – ‘H138 (Y0) INTR & INTA not tested	M10 – Sys bus plug M16 – ‘H138 (Y0) M17 – ‘H00 (8,9,10) M40 – ‘H244 M41 – ‘H367 M42 – ‘H367 M43 – ‘H11 M35 – ‘H245 INTR & INTA not tested
LPT Port Pt 2	LPT I/F PASS WR 00 RD 00	The printer port tests are split into two parts. The first part of the test writes a sequence of bytes onto the printer port that are latched on the connection test board. The system bus is then used to read the latch and compare the read value with that written on the port. If all the test patterns match then the test was successful otherwise it fails. The lower line of the DS shows the progress of the write/read test.	M19 – 80C85 (RST 6.5) M25 – 81C55 (Port A) M16 – ‘H138 (Y6,Y7) M13 – ‘H32 (4,5,6) M14 – ‘H175 (7) M32 – ‘H244 T8 – Trans The system bus is used to confirm the LPT output.	M19 – 80C85 (RST 6.5) M25 – 81C55 (Port A) M16 – ‘H138 (Y6,Y7) M13 – ‘H32 (4,5,6) M14 – ‘H175 (7) M32 – ‘H367 M10 – ‘H367 The system bus is used to confirm the

Test Name	Example Screen Display	Description	M100 Coverage	T102 Coverage
				LPT output.
LPT Port Pt 1	Busy- 01 Busy 01	The second part of the printer test exercises the BUSY and BUSY- lines on the port. This is achieved by writing a 0 and 1 into the printer latch (used in the previous test) and checking that the data read back is correct. If the test fails it should be left as '?' on the screen. This also tests the PIO Port C register for PC0 (BUSY) and PC1 (BUSY-).	M25 – 81C55 (38,39) M16 – 'H138 (Y7)	M25 – 81C55 (38,39) M16 – 'H138 (Y7)
BCR Port	BCR I/F LP FA CT 00 PASS	The BCR port test checks the RST 5.5 and PIO Port PC3 (BCR). The printer port latch is used to toggle the BCR input pin a set number of times. This is counted using an RST 5.5 routine. In addition the PIO pin is checked to make sure it is a logic 1, if it is not the count is not incremented. At the end of the test the count should match the number of cycles. If the counts do not match the test fails. The lower line of the DS shows the status of the test.	M19 – 80C85 (RST 5.5) M25 – 81C55 (1) M16 – 'H138 (Y7) M34 – 4904 (8,9)	M19 – 80C85 (RST 5.5) M25 – 81C55 (1) M16 – 'H138 (Y7) M34 – 14584 (8,9)
OPT ROM	OPTROM SWITCHED RAM 0	The OPTROM switch is tested by copying code from the ROM into a good RAM module. This code is then called from the ROM during the test. During execution the code switches to the OPTROM and reads address locations 40H to 48H storing the results in preset RAM locations, the code then switches back to the ROM. The ROM checks the RAM locations do not read 'No Optrom' if this is the case then the switch to the OPTROM was successful otherwise it failed. The lower line of the DS indicates which RAM module was used to run the test. Generally the lowest numbered good RAM module is used to run the test.	M5 – 'H139 (5) M14 – 'H175 (2) M16 – 'H138 (Y6) M13 – 'H32 (4,5,6)	M5 – 'H139 (5) M14 – 'H175 (2) M16 – 'H138 (Y6) M13 – 'H32 (4,5,6)
Keyboard Tests		There are two options for testing the keyboard on an M100: Use of the keyboard panel or Loopback cable. The firmware automatically detects whether or not keyboard is looped back.		
Keyboard	KEYBOARD KEY: 01 X	The keyboard test requires some interaction to press the desired keys. When a key is pressed the key char/function and the keyboard matrix status are displayed on the lower line of the DS. If a key is not working then this could mean the key contact is bad, the keyboard PCB trace is bad (e.g. corroded) or the keyboard buffers on the motherboard are bad. The problem can be further diagnosed by reference to the keyboard matrix in the relevant reference manual. If a key on the same col or row as a failed key works then it would indicate a bad key, for example. It should be noted that the keyboard PCB is not a direct physical analog some of the tracks split in the middle to run back to the relevant pin. This could mean some keys on a row or column will work while others do not. If no key is pressed for 10s the test ends and moves on. This is to prevent the case of a bad keyboard causing the test to stall. Pressing ctrl-break will cause the keyboard test to	M25 – 81C55 (Port A, PB0) M15 – 'H244 M13 – 'H32 (1,2,3) M16 – 'H138 (Y5) Keyboard array is tested by pressing keys.	M25 – 81C55 (Port A, PB0) M3 – 'H367 M15 – 'H367 M13 – 'H32 (1,2,3) M16 – 'H138 (Y5) M26 – 'H32 (4,5,6) Keyboard array is tested by pressing keys.

Test Name	Example Screen Display	Description	M100 Coverage	T102 Coverage
		terminate immediately.		
Keyboard Loopback (M100 Only)	KEY LOOPED PASS	M100 ONLY The keyboard loopback test will test the PIO PA0-PA7 lines to the keyboard by connecting them directly the keyboard KR0-KR7 lines. All the KRx lines are tested. If all tests pass then 'PASS' will be displayed. If a test fails then the 2nd line of the DS will display the data written and the data read back for the failed test. From this data it should be possible to determine which KRx line is not being correctly driven to the keyboard. NOTE: The PB0 line also connects to the keyboard however it is not possible to loop this back so is omitted from the test. If the keys controlled by PB0 fail when the keyboard is connected then this line will need to be checked for continuity as PB0 is also used to drive the LCD. The LCD test does test PB0 and if that passes then either the keyboard or a trace is faulty.	M25 – 81C55 (Port A) M15 – 'H244 M13 – 'H32 (1,2,3) M16 – 'H138 (Y5).	N/A
Cassette Remote	CAS REMOTE PASS	The cassette remote control is tested using the connection test board. In this case the remote is set on and off and this is confirmed via the connection board. When the remote is being tested the clicking of the RY1 relay should be audible. The RM LED on the connection test board should blink during the test.	M14 – 'H175 (15) M16 – 'H138 (Y6) M13 – 'H32 (4,5,6) M34 – 4904 (3,4) T6 – Trans RY1 – Relay	M14 – 'H175 (15) M16 – 'H138 (Y6) M13 – 'H32 (4,5,6) M34 – 4904 (3,4) T6 – Trans RY1 – Relay
Cassette Write	CAS AUDIO TEST REC[GRY]ctl-brk	The cassette tests are best conducted using a PC/MAC running an audio playback/record program. Audacity works very well for this purpose. The first test involves writing a header (AAH and sync sequence) to the cassette output. Before starting the test by pressing ctrl-break the recorder should be started. When the header has been written the recorded output can be examined to determine if the test has passed. If no action is taken for 10s the test ends and moves on. This is to prevent the case of a bad keyboard causing the test to stick. Pressing shift-break will cause the cassette test to terminate immediately.	M34 – 4904 (12,13) M19 – 80C85 (SOD)	M34 – 14584 (1,2) M19 – 80C85 (SOD)
Cassette Read	CAS AUDIO TEST PLAY[BLK]ctl-brk	The play back test is best conducted using a .wav file from a pre-recorded software program, any of the many downloadable examples will work. The header recorded in the previous test could also be used. This test may require some tuning of the volume settings to make the test successful. Once started the test does not time out nor is it possible to break out. The test can be started and then the audio file played into the port. If a header and sync sequence is detected then the test will pass and display 7FH as the received sync sequence.	M30 – TL064 (8,9,10) M34 – 4904 (10,11) M19 – 80C85 (SID)	M30 – TL064 (14,15,20) M34 – 14584 (5,6) M19 – 80C85 (SID)

Test Name	Example Screen Display	Description	M100 Coverage	T102 Coverage
		Otherwise it will remain searching for the header until reset.		
Power Down	WAIT FOR PWR OFF (c) 4/2020 V2.5 Powering off! (c) 4/2020 V2.5	This is the final screen showing the test version and copyright information. The screen will change to a powering off screen after about 10s. The powering off screen will then be displayed for ~2s before the unit powers off. This tests the power off circuits on the board.	M27 – 'H11 (1,2,3,11,12,13) M28 – 'H13	M27 – 'H11 (1,2,3,11,12,13) M28 – 'H13 T20 - Trans

Annex A

Electrolytic Capacitors

The following capacitors should be replaced as part of any refurbishment of the M100 or T102 motherboard. When replacing the capacitors check underneath and around the area to look for corroded tracks. A number of critical tracks run under several of the capacitors and may appear intact when they are in fact corroded.

Reference	Value, Voltage
C49, C50, C54, C55	10µF, 16V
C78	3.3µF, 50V
C82	4.7µF, 25V
C83	470µF, 10V
C84	470µF, 6.3V
C85	33µF, 10V
C86	100µF, 6.3V
C90	1µF, 50V
C92	0.47µF, 50V

Annex B

TASM Batch File

Windows Batch file used to generate the test firmware. The TASM assembler location will vary depend on how it is installed on the machine.

```
C:\tasm32-1\tasm -g0 -85 %1
@echo off
del *.hex
ren *.obj *.hex
```

Annex C

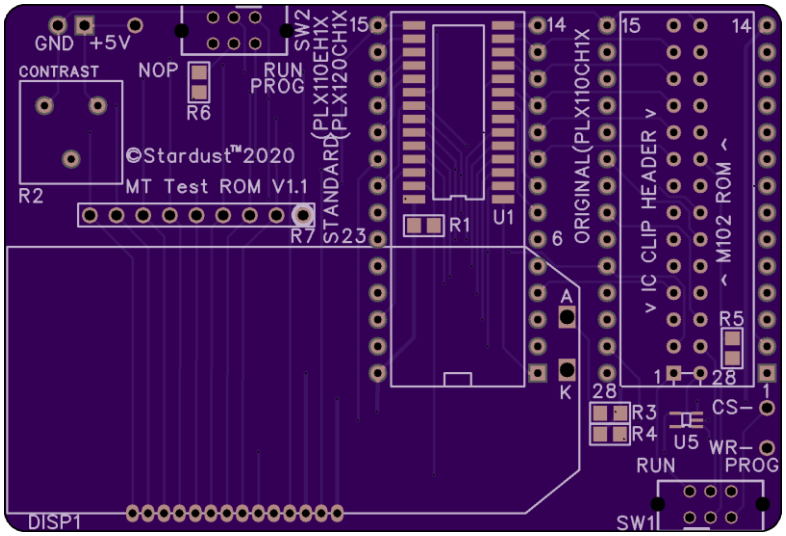
Board layouts and parts list.

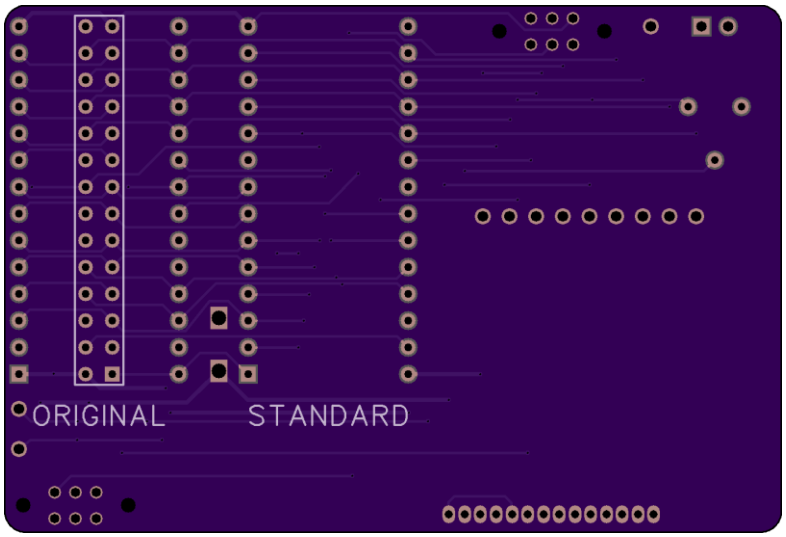
In addition to the following boards these extra parts are also required:

2 x Test clips, XKMGRY, 461-1011-ND, MICRO-HOOK GRAY 0.025" SQ PINS

1 x Flat ribbon cable to program ROM board. Made up of 28pin IDC DIP Header and 28pin IDC Header.

ROM Board Type 1



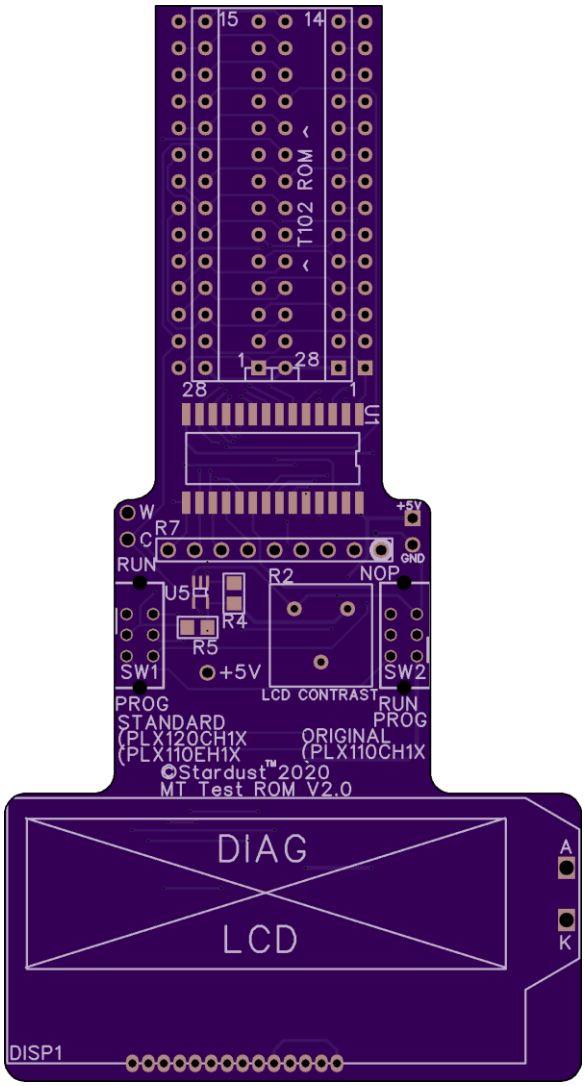


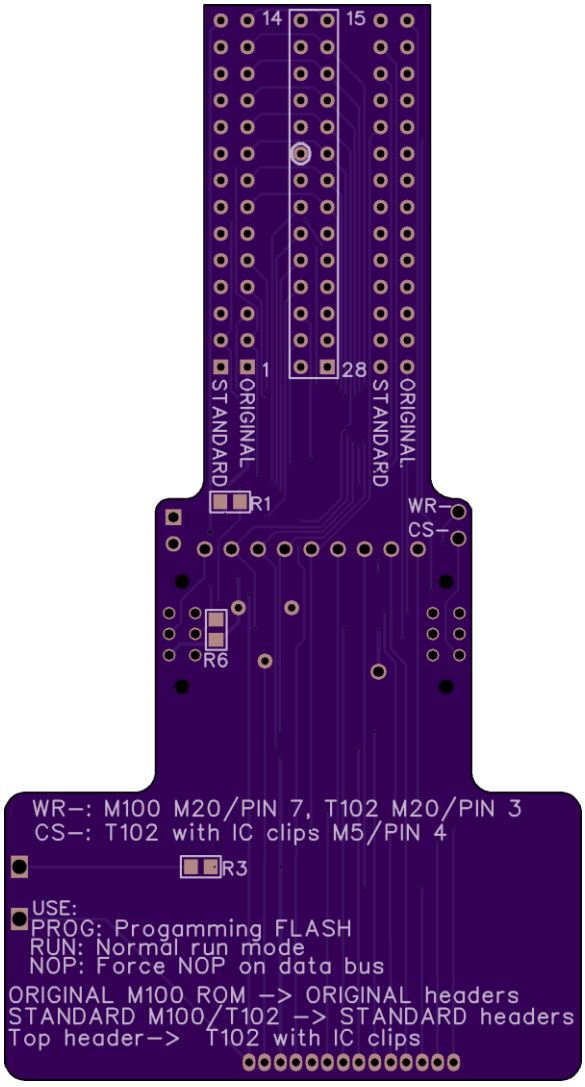
Parts List for Rectangular ROM Board

Reference	Digi-Key Part Number	Qty	Man. Part Number	Description

Used as the consumable pins for the ROM socket	1175-1525-5-ND	1	220-1-28-006	CONN HDR DIP MALE PIN 28POS GOLD
DISP1	NHD-C0216AZ-FSW-GBW-ND	1	NHD-C0216AZ-FSW-GBW	LCD MOD 32DIG 16X2 TRANSFLCT WHT
R1, R4, R5, R6	311-100KCRCT-ND	4	RC0805FR-07100KL	RES SMD 100K OHM 1% 1/8W 0805
R2	3386F-203LF-ND	1	3386F-1-203LF	TRIMMER 20K OHM 0.5W PC PIN TOP
R7	4609X-AP1-103LFCT-ND	1	4609X-AP1-103LF	RES ARRAY 8 RES 10K OHM 9SIP
ROM Headers	952-1938-ND	2	D01-9973242	CONN SOCKET SIP 32POS GOLD
SW1, SW2	EG1941-ND	2	EG2208	SWITCH SLIDE DPDT 200MA 30V
U1	AT28C256-15SU-TCT-ND	1	AT28C256-15SU-T	IC EEPROM 256K PARALLEL 28SOIC
U5	74AHC1G02SE-7DICT-ND	1	74AHC1G02SE-7	IC GATE NOR 1CH 2-INP SOT353

ROM Board Type 2 (T-Board)



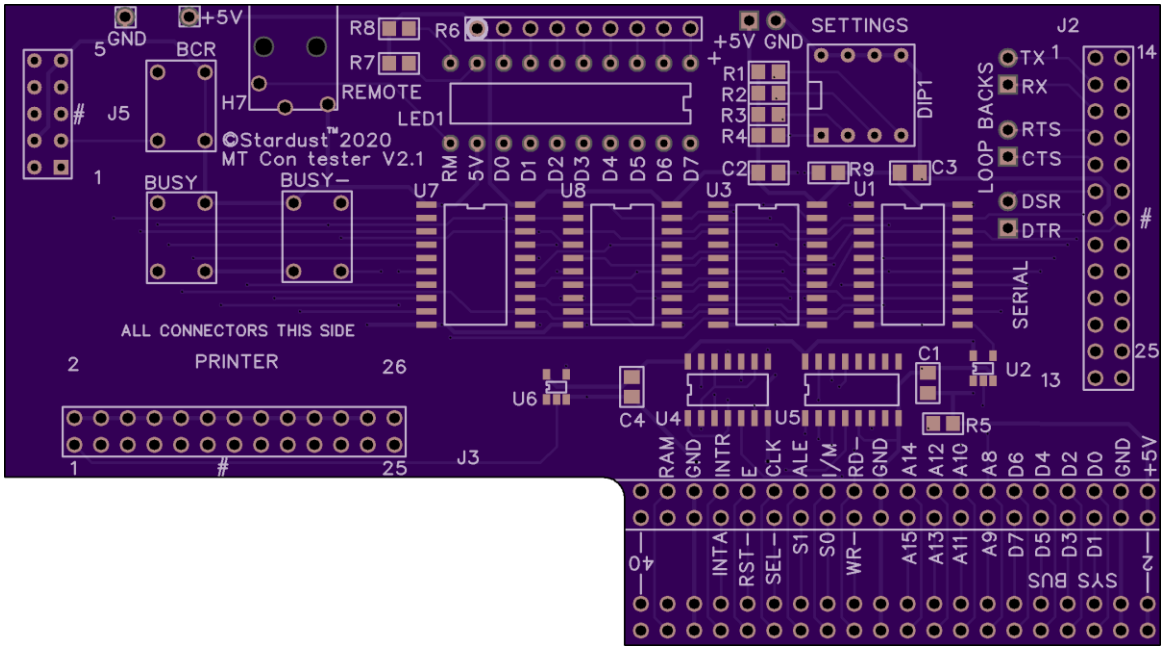


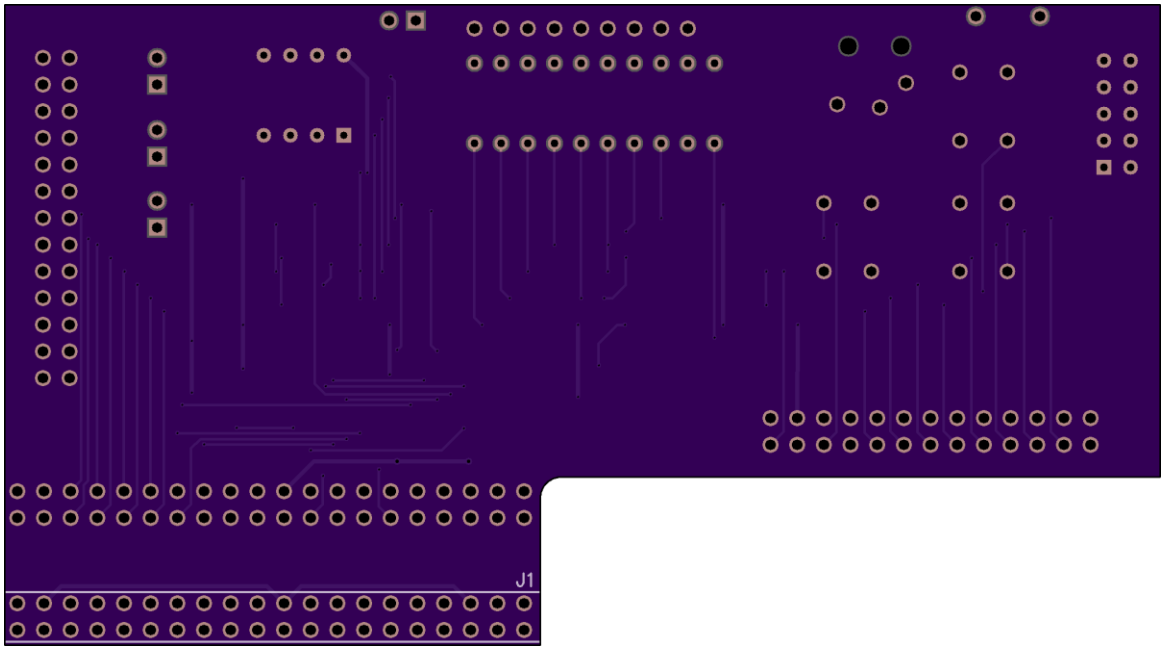
Parts List for T shaped ROM Board

Reference	Digi-Key Part Number	Qty	Man. Part Number	Description
Used as the consumable pins for the ROM socket	1175-1525-5-ND	1	220-1-28-006	CONN HDR DIP MALE PIN 28POS GOLD
ROM Headers	SAM1140-14-ND	2	SDL-114-TT-11	CONN RCPT 28POS 0.1 TIN PCB
DISP1	NHD-C0216AZ-FSW-GBW-ND	1	NHD-C0216AZ-FSW-GBW	LCD MOD 32DIG 16X2 TRANSFLCT WHT
R1, R4, R5, R6	311-100KCRCT-ND	4	RC0805FR-07100KL	RES SMD 100K OHM 1% 1/8W 0805
R7	4609X-AP1-103LFCT-ND	1	4609X-AP1-103LF	RES ARRAY 8 RES 10K OHM 9SIP
SW1, SW2	EG1941-ND	2	EG2208	SWITCH SLIDE DPDT 200MA 30V
U1	AT28C256-15SU-TCT-ND	1	AT28C256-15SU-T	IC EEPROM 256K PARALLEL 28SOIC
U5	74AHC1G02SE-7DICT-ND	1	74AHC1G02SE-7	IC GATE NOR 1CH 2-INP SOT353

Reference	Digi-Key Part Number	Qty	Man. Part Number	Description
R2	3386F-203LF-ND	1	3386F-1-203LF	TRIMMER 20K OHM 0.5W PC PIN TOP

Connection Test board



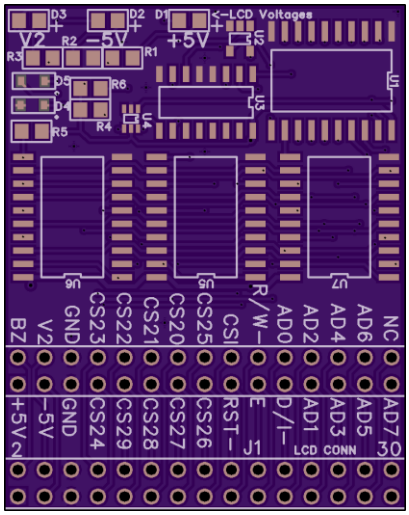


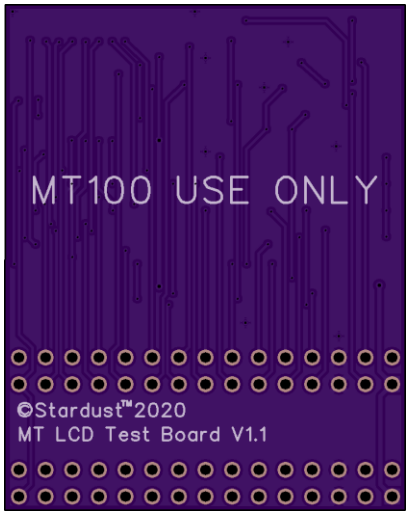
Parts List for Connection Test Board

Reference	Digi-Key Part Number	Qty	Man. Part Number	Description

BCR test plug.	LFL09H-ND	1	410F0-09-1-00	CONN D-SUB RCPT 9POS IDC
Serial test plug.	HMM25H-ND	1	A-DSF 25LPIII/Z	CONN D-SUB PLUG 25POS IDC
BCR test header.	ED10500-ND	1	101-106	CONN SOCKET 10POS IDC GOLD
Serial header Printer header (2)	ED10505-ND	3	101-266	CONN SOCKET 26POS IDC GOLD
BUSY, BUSY-, BCR test switches (optional)	450-1650-ND	3	1825910-6	SWITCH TACTILE SPST-NO 0.05A 24V
Shorting pins for loopbacks	S9001-ND	3	SPC02SYAN	CONN JUMPER SHORTING GOLD FLASH
Shorting headers pins	S1211EC-02-ND	3	PRPC002SFAN-RC	CONN HEADER VERT 2POS 2.54MM
C1, C2, C3, C4	399-1284-1-ND	4	C0805C105K4RACTU	CAP CER 1UF 16V X7R 0805
DIP1	GH7170-ND	1	76SB04T	SWITCH ROCKER DIP SPST 150MA 30V
H7	CP-M2509N-ND	1	MJ-2509N	CONN JACK MONO 2.5MM R/A
J1	3M15457-ND	1	30340-5002HB	CONN HEADER R/A 40POS 2.54MM
J2,J3	377-2269-ND	2	BC-32677	CONN HEADER VERT 26POS 2.54MM
J5	ED1543-ND	1	302-S101	CONN HEADER VERT 10POS 2.54MM
LED1	1080-1183-ND	1	MV54164	LED BARGRAPH 10-SEG HI EFF GREEN
R1, R2, R3, R4, R5, R9	311-100KCRCT-ND	6	RC0805FR-07100KL	RES SMD 100K OHM 1% 1/8W 0805
R6	4609X-101-102LF-ND	1	4609X-101-102LF	RES ARRAY 8 RES 1K OHM 9SIP
R7, R8	311-1.0KARCT-ND	2	RC0805JR-071KL	RES SMD 1K OHM 5% 1/8W 0805
U1,U7	296-1203-1-ND	2	SN74HC573ADWR	IC OCT D-TYPE LATCH 20-SOIC
U2,U6	296-1092-1-ND	2	SN74AHC1G14DBVR	IC INVERTER SCHMITT 1CH SOT23-5
U3,U8	296-1196-1-ND	2	SN74HC244DWR	IC BUFFER NON-INVERT 6V 20SOIC
U4	296-1199-1-ND	1	SN74HC32DR	IC GATE OR 4CH 2-INP 14SOIC
U5	296-4540-1-ND	1	SN74AHC138DR	IC 3-8 LINE DECODR/DEMUX 16-SOIC

LCD loopback board (MT100 use only)





Parts List for LCD loopback Board

Reference	Digi-Key Part Number	Qty	Man. Part Number	Description
D1,D2,D3	160-1428-1-ND	3	LED YELLOW CLEAR CHIP SMD	LTST-C171KSKT
D4,D5	MM3Z2V7T1GOSTR-ND	2	DIODE ZENER 2.7V 300MW SOD323	MM3Z2V7T1G
J1	S5568-ND	1	CONN HDR 30POS 0.1 GOLD PCB R/A	PPPC152LJBN-RC
R1,R2	311-511CRCT-ND	2	RES SMD 511 OHM 1% 1/8W 0805	RC0805FR-07511RL
R3	311-1.0KARCT-ND	1	RES SMD 1K OHM 5% 1/8W 0805	RC0805JR-071KL
R4,R5,R6	311-100KCRCT-ND	3	RES SMD 100K OHM 1% 1/8W 0805	RC0805FR-07100KL
U1	296-1203-1-ND	1	IC OCT D-TYPE LATCH 20-SOIC	SN74HC573ADWR

U2	296-1092-1-ND	1	IC INVERTER SCHMITT 1CH SOT23-5	SN74AHC1G14DBVR
U3	296-4540-1-ND	1	IC 3-8 LINE DECODR/DEMUX 16-SOIC	SN74AHC138DR
U4	296-15569-1-ND	1	IC 1OF2 NON-INV DEMUX SC70-6	SN74LVC1G18DCKR
U5,U6,U7	296-1196-1-ND	3	IC BUFFER NON-INVERT 6V 20SOIC	SN74HC244DWR

Keyboard loopback Test Board (MT100 use only)

No Image.

Parts List for Keyboard loopback Test Board

Reference	Digi-Key Part Number	Qty	Man. Part Number	Description
J1,J2	WM18880-ND	2	CONN HOUSING 10POS 2.5MM SHROUD	50375103
Pins	WM18889CT-ND	16	CONN SOCKET 22-28AWG CRIMP TIN	8701039

Annex D

Test template

Test Name	PASS	FAIL	RESULT
CPU			
RAM Upper Line			
RAM Lower Line			
PIO			
LCD ONLY			
DNGL-AD7-0			
DNGL-C20-27			
DNGL-C28-29			
CLK			
RST 7.5			
Serial Port Pt 1			
Serial Port Pt 2			
System Bus			
LPT Port Pt 2			
LPT Port Pt 1			
BCR Port			
OPT ROM			
Keyboard			
KEY LOOPED			
Cassette Remote			
Cassette Write			
Cassette Read			
Power Down			