

M100/T102 Test Harness Reference Manual

V1.0

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Welcome to the M100/T102 Test Harness Reference Manual!

Introduction

This document outlines the use of the M100/T102 test harness including how to construct the harness, use the harness to test the Model T and items to look for when running tests. The Test Harness runs its own firmware independently of the Model T ROM, therefore it is easily modified to suit your own needs and methods of debugging hardware, everyone works out problems differently so there is some flexibility. The firmware is written using the 8085 Assembly Language and will assemble using the TASM assembler, however it should be straightforward to modify it to run under any assembler. The firmware is not designed to run on the M200.

There are 3 boards in the test harness set: Format 1 ROM board (Rectangular Shape), Format 2 ROM board (T-shape) and Connection test board. The two ROM boards are electrically identical only the format is changed to allow more access to the board motherboard chip set, especially on the M100.

The test harness firmware provides the ability to test all parts of the model T with the following exceptions:

- Power supply. The power supply section should be operational before testing and producing a good +5 and -5V.
- Modem port. The modem port is not tested however the serial port is tested which is shared with the modem. Tests could be added to test the modem if desired.
- LCD contrast. The contrast control for the LCD is not tested this can only be checked by viewing the screen or checking with a voltmeter.
- Low power warning. The low power warning to the 8085 is not tested however the TRAP function is used to turn off the model T if power is removed. If the TRAP is not working then the battery backup feature might fail. This would be shown by the RAM backup test. It is therefore indirectly tested.

References

1. TRS-80 Model 100 Reference Manual, Catalog No. 26-3810
2. TRS-80 Model 102 Reference Manual, Catalog No. 26-3803
3. TASM Documentation

Test Equipment

The following test/repair equipment is recommended to supplement the test harness.

1. Voltmeter. Used to verify the power supply voltages and battery charge state.
2. Logic Probe. This can be used to check that pins are connected electrically or are changing when a particular test is run. It also helps if the NOP function is set. Many of the faults on the model T involve corrosion of PCB tracks leading to floating pins on the affected IC.
3. EEPROM Programmer. The programmer is required to load or change the firmware in the onboard EEPROM. The XGecu Programmer TL866II PLUS works well with the test harness.
4. Magnifying glass or loupe. This is useful when inspecting the board for corrosion, broken tracks or poor solder joints.
5. Soldering iron and solder. This can be used to replace or repair parts.
6. Cassette cable. This is used to test the cassette port on the model T.

Construction

The construction of the boards should be straightforward some of the parts might not be required depending on how the boards will be used. Only one ROM board is required, the choice of the ROM board format is a personal preference.

Consideration should be given to the type of pins etc used to insert into the ROM socket of the M100. They should be considered a consumable item, as they are very likely to break with constant insertion-removal from an IC socket. For this reason the BOM for the ROM boards uses headers to accommodate pins for insertion into the sockets. Female pin headers are then used to insert into the ROM sockets and onto the ROM board. The parts are identified in the Annex C parts list.

The connection test board is powered by the system bus +5V line this should illuminate the power LED when connected correctly. The use of the connection test board is optional however all tests dependent on that board will fail. The serial test port has jumpers for the CTS, DSR, RTS and DTR lines which can be removed during the test to confirm their operation as well as to connect test equipment. Similarly the RX-TX lines are looped back via a header that allows connection to external test equipment.

The remote lead for the cassette cable is plugged into the 2.5mm socket on the test board. It is also connected to one of the onboard LEDs. The LED should blink during the testing as the remote feature is turned on and off.

Loading the firmware onto the ROM board

The blank EEPROM on the ROM board needs to be programmed with the required test suite before use. The supplied .ASM file is TASM compatible and uses the 8085 CPU option. It should be possible to use other assemblers with some modification of the directives or label syntax. The assembler should be configured to produce Intel

HEX format for loading into the EEPROM programmer. Annex B contains the .bat file used to assemble the test program.

Both formats of the ROM board were designed to minimize their size and allow greater access to the motherboard chipset consequently it is difficult to use the ZIF socket directly on an EEPROM programmer – the PCB blocks the lever on the ZIF socket. If the board will only be programmed once or very infrequently then it is possible to raise the ROM board higher using another socket, the STANDARD ROM option can then be used to program the board. The slide switches should be set to PROG and RUN/PROG.

An alternative approach is to use a ribbon cable fitted with a 28pin IDC DIP header on one end and a 28pin IDC female header on the other. The DIP header is easily fitted into the programmer ZIF socket and the header can then be plugged onto the male header on the ROM board. This arrangement is very convenient if the board will be reprogrammed frequently during a debug session. The slide switches should still be set to PROG and RUN/PROG.

Configuration

The configuration of the Test Harness only varies slightly for the two supported Model Ts.

M100

The model 100 fortunately has a ROM socket which makes it very easy to insert the ROM test board. However the model 100 has two different ROM socket styles: Original and Standard. The Original format is primarily found on early versions of the M100 they are identified by PLX110CH1X stamped on the PCB. This requires the use of the ORIGINAL headers on the ROM board. The Standard format is identified by PLX110EH1X stamped on the PCB. This requires the use of the STANDARD headers on the ROM board.

The system bus connection on the model 100 uses a 40pin IC socket. This connection will require the use of a 40pin IC header to 40pin header. The ribbon cable can be a simple straight through connection without any need to twist the cable as is normally required for connection to a DVI box.

The remaining connectors are straightforward connections to their respective ports.

The WR- line on the ROM board has to be connected to M20/Pin 7, this is the buffered WR- line from the 80C85.

T102

The model 102 is slightly more difficult to work on as it must be removed from the case and spread out in order to access the ICs which are on both sides of the motherboard. This can make it awkward to connect the ROM board and the required jumpers to make the ROM board operational. Take great care not to

damage either the LCD screen or keyboard cables it is very easy to crack the copper traces inside the cables or rip off the edge fingers when inserting the cables into their sockets. The LCD screen and keyboard do not need to be attached when testing, their tests will show as fail but the rest of the tests will run.

The model 102 unfortunately does not use a ROM socket (unless it has been modified) this means that IC test clips are needed to clip onto the T102 ROM. The header on the ROM test board can be used to connect to the IC test clip via Dupont cables. In addition the CS- line (pin 20) to the ROM needs to be cut in order to disable the onboard ROM and allow the ROM board to take over the motherboard. The track near the pin can be cut and repaired very easily. The T102 ROM is a standard ROM so that is the only option available for this machine. The T102 PCB is stamped with PLX120CH1X just for confirmation. NOTE: The IC test clip can be any size greater than 28pins, there is plenty of room for the clip to overhang the board.

The system bus connection on the model 102 is found on the rear of the unit and the connection test board can be plugged directly into this port. There is no need to make a cable. However because of how the model 102 is configured the board might have to inserted “upside down”.

The remaining connectors are straightforward connections to their respective ports from the connection test board.

The WR- line on the ROM test board has to be connected to M20/Pin 3, this is the buffered WR- line from the 80C85. The CS- line on the ROM test board has to be connected to M5/Pin 4 in order to allow access to the ROM on the test board.

Prerequisite

The following items need to be considered before using the ROM test board.

- Power supply operational. Before running the test harness it is important that the power supply is working correctly.
- Recap. As the boards to be tested are over 35yo it is very likely that some or all of the electrolytic capacitors are bad. It is recommended that at least the caps listed in Annex A are replaced before testing further. This might actually resolve many issues on the board.
- Replace NiCd battery. If the backup NiCd battery has not been replaced it is very likely bad and should be replaced as a matter of course. It can be replaced with a NiMH battery of the same style. Or in some cases it could be replaced with a Supercap. The Supercap will not last as long as a NiMH battery but should give sufficient time to change the AA batteries.



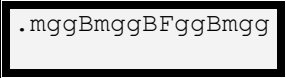
Hints and tips for debugging M100 and T102 motherboards

The following section gives some insight into things to look for when debugging M100 and T102 motherboards.

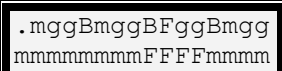
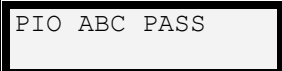
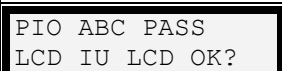
- The M100/T102 boards were sometimes not washed properly after manufacture leaving solder flux on the board. Over the years the solder flux will corrode copper tracks causing breaks in the connections. When inspecting a board look for flux that has not been removed and check for continuity of the traces. This effect seems to occur most around connectors or sockets. The trace might look OK however the copper has usually been transformed into an open trace.
- On the M100 motherboards there can be dry solder joints that have failed over time. The bad joints usually have a silver crystalline appearance or may show as breaks. Reheating the bad joint with fresh solder will usually fix this problem.
- On the M100/T102 boards some of the traces are very fine and can be over etched cause the traces to break particularly around through-hole components.
- The Electrolytic caps will fail over time and can either leak or outgas onto the board. If the caps leak their chemicals can easily destroy nearby copper traces causing them to become open circuit. Again the trace could appear as a copper trace but it might have become a non-conductive trace. This is a particular problem in the power supply area where important traces run under or near the caps. Therefore it is imperative to clean the area under the cap and inspect for damage. Outgassing can cause corrosion of nearby parts but generally this does not have much of a severe impact on the board however it could damage the LCD screen or keyboard near those parts.
- Battery acid leakage on the motherboards is a big problem in some cases. Generally this can be more severe on the T102 motherboards as the battery box is attached directly to the board. The acid damage is very difficult to deal with and cleaning the board can simply reactivate the acid causing more damage. Any gas from the acid can also damage nearby components such as the LCD display edge connector or the LCD panel itself.

Test Coverage

The following table lists the test in order of application. It also highlights the area or chips being tested. If a test fails the remaining test should be allowed to execute as this may shed more light on the location of the fault condition.

Test Name	Example Screen Display	Description	M100 Coverage	T102 Coverage
CPU		The first test simply confirms the CPU and the identified ICs are functional by writing to the diagnostic screen (DS). If the 'CPU' text does not appear then the first area to check is the CPU area.	RESET circuit M19 – 80C85 M21 – 'H244 M20 – 'H244 M2 – 'H245 M1 – 'H373 M5 – H139 (1,2,3,4) M12 – ROM X2 - XTAL	RESET circuit M19 – 80C85 M21 – 'H244 M20 – 'H244 M2 – 'H245 M1 – 'H373 M5 – H139 (1,2,3,4) M12 – ROM X2 - XTAL
RAM pt 1	 	<p>The RAM tests are broken into several parts to focus on different parts of the RAM modules. For the M100 the modules are made up of 4 x 2K blocks so there could be individual failures that might go undetected with tests for an 8K block. The first line of the screen provides information on the four RAM modules. Each module accounts for 4 characters and are sequenced: 3, 2, 1 and 0. There are four tests in part 1 as follows:</p> <ol style="list-style-type: none"> 1. Battery backup. This is only valid if the test has been run once and the unit power cycled. The test looks for a specific pattern at a certain address to see if the memory has been retained. If successful the DS will show 'B' for that module, or a '.' if the test fails. 2. Complete RAM write-read test. Each location is written to and read back with a sequence of pre-stored patterns. Any location that fails to read back correctly stops the test and will cause and 'F' to be printed on screen. If the RAM passes then 'm' will be printed. This test may take a while to run if the RAM is good. 3. First page RAM test. This test writes 1..255 into the first 255 locations in order to test the address selection for the RAM module and that each location is uniquely addressed. If the test passes it will print 'g', a failure will print an 'H'. 4. Address line test. This test checks each of the A0..A7 address lines to make sure they are operational. If the test passes it will print 'g' otherwise it will print a number to indicate which address line has failed. It should be noted that failed lines may mask other failures. 	M6 – RAM M7 – RAM M8 – RAM M9 – RAM M3 – 'H138 M4 – 'H138 D22 – Diode, as part of the VB battery backup operations	M6 – RAM M7 – RAM M8 – RAM M9 – RAM M5 – 'H138 M37 – 'H00 (8,9,10,11,12,13) M27 – 'H11 (4,5,6) D22 – Diode, as part of the VB battery backup operations

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Test Name	Example Screen Display	Description	M100 Coverage	T102 Coverage
RAM pt 2		Part 2 of the RAM tests exercises each of the CS- lines running to each of the modules on the M100 or the decode logic on the T200. The bottom line of the DS is used to display the 16 'CS' lines starting from the left for module 3 and ending on the right for module 0. If the test is successful for that line an 'm' is displayed if it fails then and 'F' is printed. In the case of an M100 this could indicate which 2K RAM has failed. In the case of the T102 it simply means the RAM chip has failed.	M6 – RAM M7 – RAM M8 – RAM M9 – RAM M3 – 'H138 (Y0-Y7) M4 – 'H138 (Y0-Y7)	M6 – RAM M7 – RAM M8 – RAM M9 – RAM M5 – 'H138 M37 – 'H00 (8,9,10,11,12,13)
PIO		<p>The PIO test checks that the Port A and Port B registers can be written to and read from using the same test pattern as that used for the RAM tests. In the case of Port B the power off bit is masked so it does not turn off the machine! If either Port A or Port B fails then further testing is aborted as all other parts of the M100/T102 rely on the PIO to operate. In this case the test program will display four options a Port A write of 00H and FFH and the read back and the same for Port B. The test will then halt the CPU.</p> <p>If Port A and Port B test out successfully then Port C is read and the status of the LPT busy lines checked. If this fails then the PIO test fails. The other lines associated with Port C are tested in their relevant sections.</p> <p>The timer portion of the PIO is tested when the serial port is tested.</p> <p>The control register can only be indirectly tested however if subsequent tests fail then it can be assumed that the PIO has a problem. The problem could be a failed IC or failed traces on the board due to corrosion.</p>	M25 – 81C55 M16 – 'H138 (Y3) Registers tested and lines into 81C55. The Port A, B and C output lines are not tested by this test except indirectly via the data written to the ports.	M25 – 81C55 M16 – 'H138 (Y3) M17 – 'H00 (1,2,3) Registers tested and lines into 81C55. The Port A, B and C output lines are not tested by this test except indirectly via the data written to the ports.
LCD		<p>The screen should be observed during this test run. The LCD is first checked by initializing the column drivers, this involves resetting them via software, setting the counters for up mode, turning on the screen and checking the busy bit clears. If the initialization is successful then 'I' is printed on the DS. If the column drivers are set to up mode then 'U' is printed on the DS. If one or both of these operations fail then 'FAIL' is printed on the DS. The failure could occur if the screen is disconnected or faulty.</p> <p>If the screen passes initialization then it is cleared by printing 'X' to all locations. After which each of the 8 lines is printed with text. The screen should show no missing pixels, blank lines or rows. This is a visual check, as the hardware cannot directly test the LCD panel is working.</p>	M25 – 81C55 (Port A, Port B [PB0, PB1]) M17 – 'H00 (1,2,3,8,9,10,11,12,13) M16 – 'H138 (Y7)	M25 – 81C55 (Port A, Port B [PB0, PB1]) M17 – 'H00 (4,5,6,11,12,13) M16 – 'H138 (Y7)

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Test Name	Example Screen Display	Description	M100 Coverage	T102 Coverage
CLK	01001115350 PASS 01001115356	The clock IC is tested by initializing it with a pre-stored date and time. The IC is then allowed to run for ~6 secs and read back. The new time is compared to the old time and if the new time is more than 6s from the start time the test is successful and 'PASS' is printed on the screen. Otherwise 'FAIL' is printed.	M25 – 81C55 (37, PA0-PA4) M18 – uPD1990AC M14 – 'H175 (10) M13 – 'H32 (4,5,6) M16 – 'H138 (Y6) X1 – XTAL	M25 – 81C55 (37, PA0-PA4) M18 – uPD1990AC M14 – 'H175 (10) M26 – 'H32 (8,9,10) M16 – 'H138 (Y6) X1 – XTAL
RST 7.5	01001115356 05 01001115401 PASS	The RST7.5 interrupt is driven by the TP output from the clock IC to provide the regular 'tick' for the model T. Once the clock IC has been configured in the previous test the RST7.5 interrupt is enabled and the number of 'ticks' is counted over a set period. The period is determined by software delay loops. In this case it is set to 6s. If the required number of 'ticks' occur in 6s then the test is considered to have succeeded and 'PASS' is printed on the DS, if not then 'FAIL' is printed.	M18 – uPD1990AC (TP) M19 – 80C85 (7)	M18 – uPD1990AC (TP) M19 – 80C85 (7)
Serial Port Pt 1	CTRL BITS PASS RT/CT 1 DS/DT 1	<p>The serial port is tested in two parts using the connection test board. The first part of the test confirms that the RTS, DTS, DTR and DSR lines toggle. The RTS and CTS lines are looped back as are the DSR and DTR lines. First the lines are set to 1 and then 0, each time the looped back line is checked to confirm the value. If the values are good then the test is successful otherwise the test fails and the DS will show which line(s) have failed in the loopback. Subsequent testing could be done to cross link to the other lines and see where the fault goes to isolate the problem. For example link RTS-DSR and CTS-DTR and see which line is faulty. Further testing might be required to determine which part is faulty.</p> <p>The test also tests the PIO Port C pins related to CTS (PC4) and DSR (PC5), plus the PIO Port B pins RTS (PB7) and DTR (PB6)</p>	M35 – 4904 (3,4,5,6,8,9,10,11) M25 – 81C55 (2,5,32,35,36) M33 – 'H157 (5,11,7,9) M24 – 'H32 (8,9,10) M34 – 4904 (1,2)	M25 – 81C55 (2,5,32,35,36) M33 – 'H157 (5,11,7,9) M24 – 14584 (8,9,12,13) M35 – 14584 (3,4,5,6,8,9,10,11) M38 – 'H02 (8,9,10,11,12,13) M34 – 14584 (10,11)
Serial Port Pt 2	LOOPBACK PASS C 04 TX 00 RX 00	<p>The second part of the serial test involves a loop back of the TX and RX lines. In this test 256 bytes from 0 to 255 are transmitted and received. If any byte does not check then the test fails. This test uses the RST6.5 interrupt to run the test. In addition the PIO timer register is configured for 19,200bps as well as configuring the IM6402 for 8bits + No Parity + 1 stop. The TX pin could be monitored externally to verify the functionality. PIO pin PB3 is used to control the switch to the RS232 port from the modem.</p> <p>The bottom line of the DS shows the TX and RX byte being sent/received. The C value is that read from the serial comms register M23 (M100/T102).</p>	M35 – 4904 (1,2,12,13) M25 – 81C55 (32) M33 – 'H157 (2,4) M24 – 'H32 (11,12,13) M34 – 4904 (1,2) M23 – 'H244 (4,6,11,13) M22 – IMS6402 M26 – 'H02 (11,12,13) M16 – 'H138 (Y5,Y7)	M35 – 14584 (1,2,12,13) M24 – 14584 (10,11) M25 – 81C55 (32) M33 – 'H157 (2,4) M23 – 'H244 M4 – 'H244 M22 – IMS6402 M38 – 'H02 (4,5,6) M16 – 'H138 (Y5,Y7) M34 – 14584 (10,11)

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Test Name	Example Screen Display	Description	M100 Coverage	T102 Coverage
System Bus	<div>SYS BUS PASS WR 00 RD 00 S 7F</div>	<p>The System Bus test simply writes/reads a sequence of patterns to one address on the system bus. It is a basic loopback test. If all the bytes are successfully written/read the test is successful otherwise it fails. The lower line of the DS indicates the progress of the test by showing the byte being written/read.</p> <p>The S portion of the lower line shows the state of the 4 DIP switches on the header board. This is another address on the header board that effectively tests the A0 and A1 lines. The DIP switches could also be used to change the tests etc during a run if required. Currently they are ignored by V2.5, although changing their value during the test will be reflected on the DS.</p>	<p>M10 – Sys bus SKT M16 – ‘H138 (Y0) INTR & INTA not tested</p>	<p>M10 – Sys bus plug M16 – ‘H138 (Y0) M17 – ‘H00 (8,9,10) M40 – ‘H244 M41 – ‘H367 M42 – ‘H367 M43 – ‘H11 M35 – ‘H245 INTR & INTA not tested</p>
LPT Port Pt 2	<div>LPT I/F PASS WR 00 RD 00</div>	<p>The printer port tests are split into two parts. The first part of the test writes a sequence of bytes onto the printer port that are latched on the connection test board. The system bus is then used to read the latch and compare the read value with that written on the port. If all the test patterns match then the test was successful otherwise it fails.</p> <p>The lower line of the DS shows the progress of the write/read test.</p>	<p>M19 – 80C85 (RST 6.5) M25 – 81C55 (Port A) M16 – ‘H138 (Y6,Y7) M13 – ‘H32 (4,5,6) M14 – ‘H175 (7) M32 – ‘H244 T8 – Trans</p> <p>The system bus is used to confirm the LPT output.</p>	<p>M19 – 80C85 (RST 6.5) M25 – 81C55 (Port A) M16 – ‘H138 (Y6,Y7) M13 – ‘H32 (4,5,6) M14 – ‘H175 (7) M32 – ‘H367 M10 – ‘H367</p> <p>The system bus is used to confirm the LPT output.</p>
LPT Port Pt 1	<div>Busy- 01 Busy 01</div>	<p>The second part of the printer test exercises the BUSY and BUSY- lines on the port. This is achieved by writing a 0 and 1 into the printer latch (used in the previous test) and checking that the data read back is correct. If the test fails it should be left as ‘?’ on the screen. This also tests the PIO Port C register for PC0 (BUSY) and PC1 (BUSY-).</p>	<p>M25 – 81C55 (38,39) M16 – ‘H138 (Y7)</p>	<p>M25 – 81C55 (38,39) M16 – ‘H138 (Y7)</p>
BCR Port	<div>BCR I/F LP FA CT 00 PASS</div>	<p>The BCR port test checks the RST 5.5 and PIO Port PC3 (BCR). The printer port latch is used to toggle the BCR input pin a set number of times. This is counted using an RST 5.5 routine. In addition the PIO pin is checked to make sure it is a logic 1, if it is not the count is not incremented. At the end of the test the count should match the number of cycles. If the counts do not match the test fails.</p> <p>The lower line of the DS shows the status of the test.</p>	<p>M19 – 80C85 (RST 5.5) M25 – 81C55 (1) M16 – ‘H138 (Y7) M34 – 4904 (8,9)</p>	<p>M19 – 80C85 (RST 5.5) M25 – 81C55 (1) M16 – ‘H138 (Y7) M34 – 14584 (8,9)</p>

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Test Name	Example Screen Display	Description	M100 Coverage	T102 Coverage
OPT ROM	OPTROM SWITCHED RAM 0	The OPTROM switch is tested by copying code from the ROM into a good RAM module. This code is then called from the ROM during the test. During execution the code switches to the OPTROM and reads address locations 40H to 48H storing the results in preset RAM locations, the code then switches back to the ROM. The ROM checks the RAM locations do not read 'No Optrom' if this is the case then the switch to the OPTROM was successful otherwise it failed.	M5 – 'H139 (5) M14 – 'H175 (2) M16 – 'H138 (Y6) M13 – 'H32 (4,5,6)	M5 – 'H139 (5) M14 – 'H175 (2) M16 – 'H138 (Y6) M13 – 'H32 (4,5,6)
		The lower line of the DS indicates which RAM module was used to run the test. Generally the lowest numbered good RAM module is used to run the test.		
Keyboard	KEYBOARD KEY: 01 X	The keyboard test requires some interaction to press the desired keys. When a key is pressed the key char/function and the keyboard matrix status are displayed on the lower line of the DS. If a key is not working then this could mean the key contact is bad, the keyboard PCB trace is bad (e.g. corroded) or the keyboard buffers on the motherboard are bad. The problem can be further diagnosed by reference to the keyboard matrix in the relevant reference manual. If a key on the same col or row as a failed key works then it would indicate a bad key, for example. It should be noted that the keyboard PCB is not a direct physical analog some of the tracks split in the middle to run back to the relevant pin. This could mean some keys on a row or column will work while others do not.	M25 – 81C55 (Port A, PB0) M15 – 'H244 M13 – 'H32 (1,2,3) M16 – 'H138 (Y5) Keyboard array is tested by pressing keys.	M25 – 81C55 (Port A, PB0) M3 – 'H367 M15 – 'H367 M13 – 'H32 (1,2,3) M16 – 'H138 (Y5) M26 – 'H32 (4,5,6) Keyboard array is tested by pressing keys.
		If no key is pressed for 10s the test ends and moves on. This is to prevent the case of a bad keyboard causing the test to stall. Pressing ctrl-break will cause the keyboard test to terminate immediately.		
Cassette Remote	CAS REMOTE PASS	The cassette remote control is tested using the connection test board. In this case the remote is set on and off and this is confirmed via the connection board. When the remote is being tested the clicking of the RY1 relay should be audible. The RM LED on the connection test board should blink during the test.	M14 – 'H175 (15) M16 – 'H138 (Y6) M13 – 'H32 (4,5,6) M34 – 4904 (3,4) T6 – Trans RY1 – Relay	M14 – 'H175 (15) M16 – 'H138 (Y6) M13 – 'H32 (4,5,6) M34 – 4904 (3,4) T6 – Trans RY1 – Relay

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Test Name	Example Screen Display	Description	M100 Coverage	T102 Coverage
Cassette Write		The cassette tests are best conducted using a PC/MAC running an audio playback/record program. Audacity works very well for this purpose.	M34 – 4904 (12,13) M19 – 80C85 (SOD)	M34 – 14584 (1,2) M19 – 80C85 (SOD)
	CAS AUDIO TEST REC[GRY]ctl-brk	The first test involves writing a header (AAH and sync sequence) to the cassette output. Before starting the test by pressing ctrl-break the recorder should be started. When the header has been written the recorded output can be examined to determine if the test has passed.		
		If no action is taken for 10s the test ends and moves on. This is to prevent the case of a bad keyboard causing the test to stick. Pressing shift-break will cause the cassette test to terminate immediately.		
Cassette Read		The play back test is best conducted using a .wav file from a pre-recorded software program, any of the many downloadable examples will work. The header recorded in the previous test could also be used. This test may require some tuning of the volume settings to make the test successful. Once started the test does not time out nor is it possible to break out.	M30 – TL064 (8,9,10) M34 – 4904 (10,11) M19 – 80C85 (SID)	M30 – TL064 (14,15,20) M34 – 14584 (5,6) M19 – 80C85 (SID)
	CAS AUDIO TEST PLAY[BLK]ctl-brk	The test can be started and then the audio file played into the port. If a header and sync sequence is detected then the test will pass and display 7FH as the received sync sequence. Otherwise it will remain searching for the header until reset.		
Power Down	WAIT FOR PWR OFF (c) 4/2020 V2.5	This is the final screen showing the test version and copyright information. The screen will change to a powering off screen after about 10s. The powering off screen will then be displayed for ~2s before the unit powers off. This tests the power off circuits on the board.	M27 – 'H11 (1,2,3,11,12,13) M28 – 'H13	M27 – 'H11 (1,2,3,11,12,13) M28 – 'H13 T20 - Trans
	Powering off! (c) 4/2020 V2.5			

Annex A

Electrolytic Capacitors

The following capacitors should be replaced as part of any refurbishment of the M100 or T102 motherboard. When replacing the capacitors check underneath and around the area to look for corroded tracks. A number of critical tracks run under several of the capacitors and may appear intact when they are in fact corroded.

Reference	Value, Voltage
C49, C50, C54, C55	10 μ F, 16V
C78	3.3 μ F, 50V
C82	4.7 μ F, 25V
C83	470 μ F, 10V
C84	470 μ F, 6.3V
C85	33 μ F, 10V
C86	100 μ F, 6.3V
C90	1 μ F, 50V
C92	0.47 μ F, 50V

Annex B

TASM Batch File

Windows Batch file used to generate the test firmware. The tasm assembler location will vary depend on how it is installed.

```
C:\tasm32-1\tasm -g0 -85 %1
@echo off
del *.hex
ren *.obj *.hex
```


Annex C

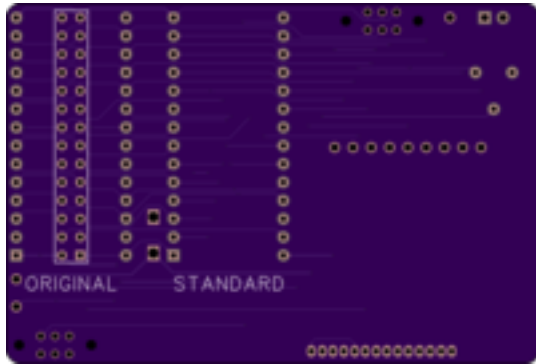
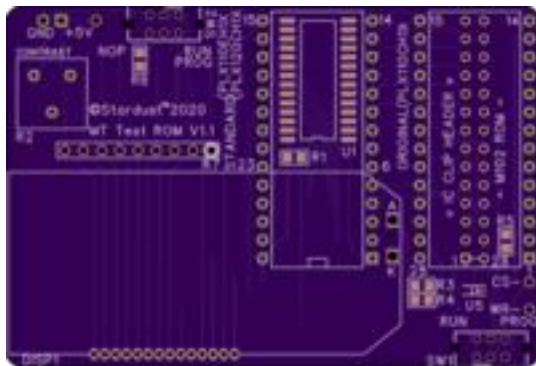
Board layouts and parts list.

In addition to the following boards these extra parts are also required:

2 x Test clips, XKMGRY, 461-1011-ND, MICRO-HOOK GRAY 0.025" SQ PINS

1 x Flat ribbon cable to program ROM board. Made up of 28pin IDC DIP Header and 28pin IDC Header.

ROM Board Type 1



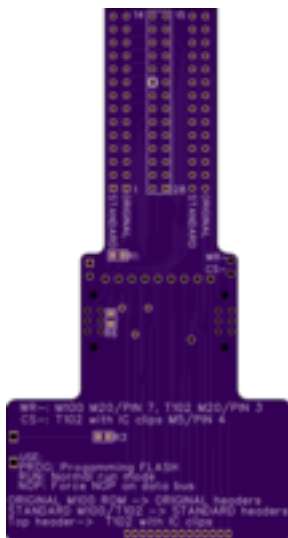
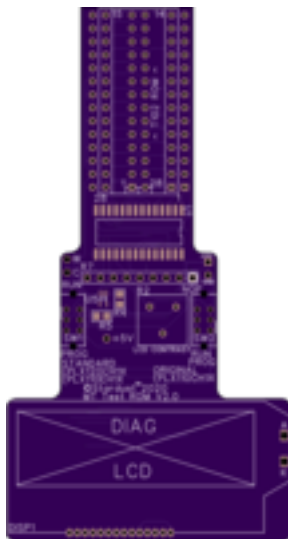
Parts List for Rectangular ROM Board

Reference	Digi-Key Part Number	Qty	Man. Part Number	Description
Used as the consumable pins for the ROM socket	1175-1525-5-ND	1	220-1-28-006	CONN HDR DIP MALE PIN 28POS GOLD
DISP1	NHD-C0216AZ-FSW-GBW-ND	1	NHD-C0216AZ-FSW-GBW	LCD MOD 32DIG 16X2 TRANSFLCT WHT
R1, R4, R5, R6	311-100KCRCT-ND	4	RC0805FR-07100KL	RES SMD 100K OHM 1% 1/8W 0805
R2	3386F-203LF-ND	1	3386F-1-203LF	TRIMMER 20K OHM 0.5W PC PIN TOP

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R7	4609X-AP1-103LFCT-ND	1	4609X-AP1-103LF	RES ARRAY 8 RES 10K OHM 9SIP
ROM Headers	952-1938-ND	2	D01-9973242	CONN SOCKET SIP 32POS GOLD
SW1, SW2	EG1941-ND	2	EG2208	SWITCH SLIDE DPDT 200MA 30V
U1	AT28C256-15SU-TCT-ND	1	AT28C256-15SU-T	IC EEPROM 256K PARALLEL 28SOIC
U5	74AHC1G02SE-7DICT-ND	1	74AHC1G02SE-7	IC GATE NOR 1CH 2-INP SOT353

ROM Board Type 2 (T-Board)



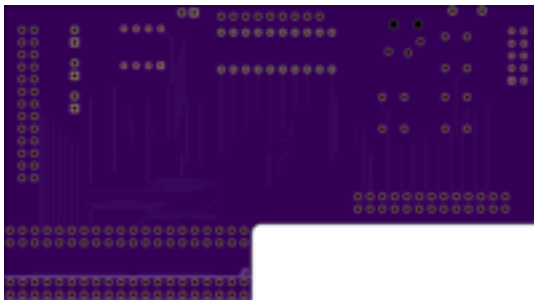
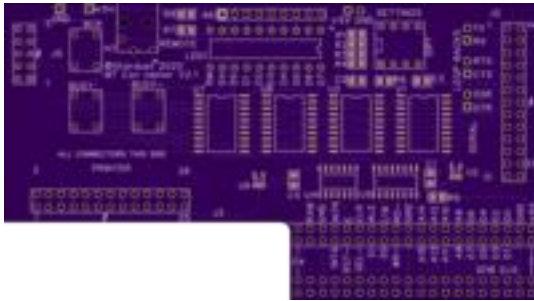
Parts List for T shaped ROM Board

Reference	Digi-Key Part Number	Qty	Man. Part Number	Description
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Test Harness Reference Manual V1.0

Reference	Digi-Key Part Number	Qty	Man. Part Number	Description
Used as the consumable pins for the ROM socket	1175-1525-5-ND	1	220-1-28-006	CONN HDR DIP MALE PIN 28POS GOLD
ROM Headers	SAM1140-14-ND	2	SDL-114-TT-11	CONN RCPT 28POS 0.1 TIN PCB
DISP1	NHD-C0216AZ-FSW-GBW-ND	1	NHD-C0216AZ-FSW-GBW	LCD MOD 32DIG 16X2 TRANSFLCT WHT
R1, R4, R5, R6	311-100KCRCT-ND	4	RC0805FR-07100KL	RES SMD 100K OHM 1% 1/8W 0805
R7	4609X-API-103LFCT-ND	1	4609X-API-103LF	RES ARRAY 8 RES 10K OHM 9SIP
SW1, SW2	EG1941-ND	2	EG2208	SWITCH SLIDE DPDT 200MA 30V
U1	AT28C256-15SU-TCT-ND	1	AT28C256-15SU-T	IC EEPROM 256K PARALLEL 28SOIC
U5	74AHC1G02SE-7DICT-ND	1	74AHC1G02SE-7	IC GATE NOR 1CH 2-INP SOT353
R2	3386F-203LF-ND	1	3386F-1-203LF	TRIMMER 20K OHM 0.5W PC PIN TOP

Connection Test board



Parts List for Connection Test Board

Reference	Digi-Key Part Number	Qty	Man. Part Number	Description
BCR test plug.	LFL09H-ND	1	410F0-09-1-00	CONN D-SUB RCPT 9POS IDC
Serial test plug.	HMM25H-ND	1	A-DSF 25LPIII/Z	CONN D-SUB PLUG 25POS IDC
BCR test header.	ED10500-ND	1	101-106	CONN SOCKET 10POS IDC GOLD

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Serial header Printer header (2)	ED10505-ND	3	101-266	CONN SOCKET 26POS IDC GOLD
BUSY, BUSY-, BCR test switches (optional)	450-1650-ND	3	1825910-6	SWITCH TACTILE SPST-NO 0.05A 24V
Shorting pins for loopbacks	S9001-ND	3	SPC02SYAN	CONN JUMPER SHORTING GOLD FLASH
Shorting headers pins	S1211EC-02-ND	3	PRPC002SFAN-RC	CONN HEADER VERT 2POS 2.54MM
C1, C2, C3, C4	399-1284-1-ND	4	C0805C105K4RACTU	CAP CER 1UF 16V X7R 0805
DIP1	GH7170-ND	1	76SB04T	SWITCH ROCKER DIP SPST 150MA 30V
H7	CP-M2509N-ND	1	MJ-2509N	CONN JACK MONO 2.5MM R/A
J1	3M15457-ND	1	30340-5002HB	CONN HEADER R/A 40POS 2.54MM
J2,J3	377-2269-ND	2	BC-32677	CONN HEADER VERT 26POS 2.54MM
J5	ED1543-ND	1	302-S101	CONN HEADER VERT 10POS 2.54MM
LED1	1080-1183-ND	1	MV54164	LED BARGRAPH 10-SEG HI EFF GREEN
R1, R2, R3, R4, R5, R9	311-100KCRCT-ND	6	RC0805FR-07100KL	RES SMD 100K OHM 1% 1/8W 0805
R6	4609X-101-102LF-ND	1	4609X-101-102LF	RES ARRAY 8 RES 1K OHM 9SIP
R7, R8	311-1.0KARCT-ND	2	RC0805JR-071KL	RES SMD 1K OHM 5% 1/8W 0805
U1,U7	296-1203-1-ND	2	SN74HC573ADWR	IC OCT D-TYPE LATCH 20-SOIC
U2,U6	296-1092-1-ND	2	SN74AHC1G14DBVR	IC INVERTER SCHMITT 1CH SOT23- 5
U3,U8	296-1196-1-ND	2	SN74HC244DWR	IC BUFFER NON-INVERT 6V 20SOIC
U4	296-1199-1-ND	1	SN74HC32DR	IC GATE OR 4CH 2-INP 14SOIC
U5	296-4540-1-ND	1	SN74AHC138DR	IC 3-8 LINE DECODR/DEMUX 16- SOIC