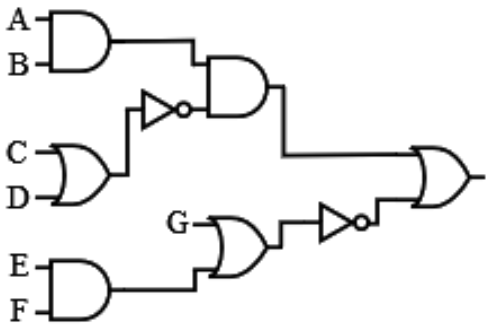
作業一

繳交期限：04/25 10：10

1. Implement logic gates below.

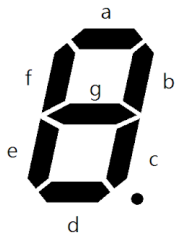


2. Use one-bit full adder to implement a 4-bit binary adder.

3. Implement the truth table below.

S	D_1	D_0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

4. Design a Verilog module that takes in a four-digit input signal in 8421-BCD encoding and uses a seven-segment display to output the corresponding decimal value.



Digits	8421-BCD				Individual Segments						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	1	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	1	1	0	0

格式要求:

1. 本次作業請使用 Gate level 撰寫
2. 每題皆須包含可執行之專案檔，程式中包含註解
3. 每題皆須 是單獨資料夾，全部壓縮成一個壓縮檔上傳
4. 必須包含 Testbench 之 Wave 執行截圖 (radix 須為 Unsigned decimal)

殼以參考: https://www.electronicshub.org/binary-adder-and-subtractor/

助教聯絡資訊: MCAS.E9.111@gmail.com