LCLS Digital BPM Interface
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Register Map

Register Map

Register	Function			
0x00	CSR	Control and Status Register		
0x01	CAL	Calibration Attenuation Register		
0x02	ATT1	Attenuation Register		
0x03	ATT2	Attenuation Register		
0x04	LMT	Limit Trip Register		
0x05	VER	Version Register		
0x06	TRG	Self Trigger Register		
0x10	TRIG2AMP	Delay from Trigger to AMP ON	10us Ticks	
0x11	AMP2RF1	Delay from AMP On to first RF Pulse	>0 33ns Ticks	
0x12	RF12RF2	Delay from RF1 to RF2 pulse excluding the width from register 0x13 and Off Time from register 0x14	33ns Ticks	
0x13	RFWIDTH	Width of the RF Pulse	>0 33ns Ticks	
0x14	OFFTIME	Delay from RF Pulse off to change of Control switches	>0 33ns Ticks	
0x3E	BOOT	Boot control	*Future feature	
0x3F	JTAG	JTAG Reprogram control	*Future feature	

Register Description

CSR Register (0x0)

Bit	Name	Use		Default
[7..6]			Read Only	
[5]	ForceLongReset			
[4]	ForceShortReset			
[3..2]	CAL_OSC	Calibration Oscillator mode	‘11’ => OFF ‘10’ => OFF ‘01’ => ON ‘00’ => AUTO	‘00’
[1..0]	CAL MODE	Calibration Mode Select	‘11’ => Nothing ‘10’ => BOTH ‘01’ => GREEN ‘00’ => RED	‘10’

CAL Register (0x1)

Bit	Name	Use		Default
[7..5]			‘0000’	
[4..0]	CALATT	Calibration attenuation	1 dB step	‘11111’

ATT Register 1 (0x2)

Bit	Name	Use		Default
[7..4]			‘0000’	
[3..0]	ATT1	First Stage Attenuation	1 dB step	‘1111’

ATT Register 2 (0x3)

Bit	Name	Use		Default
[7..4]			‘0000’	
[3..0]	ATT2	Second Stage Attenuation	1 dB step	‘1111’

LMT Register (0x4)

Bit	Name	Use		Default
[7..1]			‘0000’	
[0]	TRP	Limit Trip Latch	‘1’ => Resets the latch	

VER Register (0x5)

Bit	Name	Use		Default
[7]				0
[6..5]	Board ID	Board ID	‘01’ = BRD1 ‘00’ => BRD0	
[4..0]	Version	Version Number	Read Only	

TRG Register (0x6) (Dataless)

Bit	Name	Use		Default
	TRG	Self Trigger		

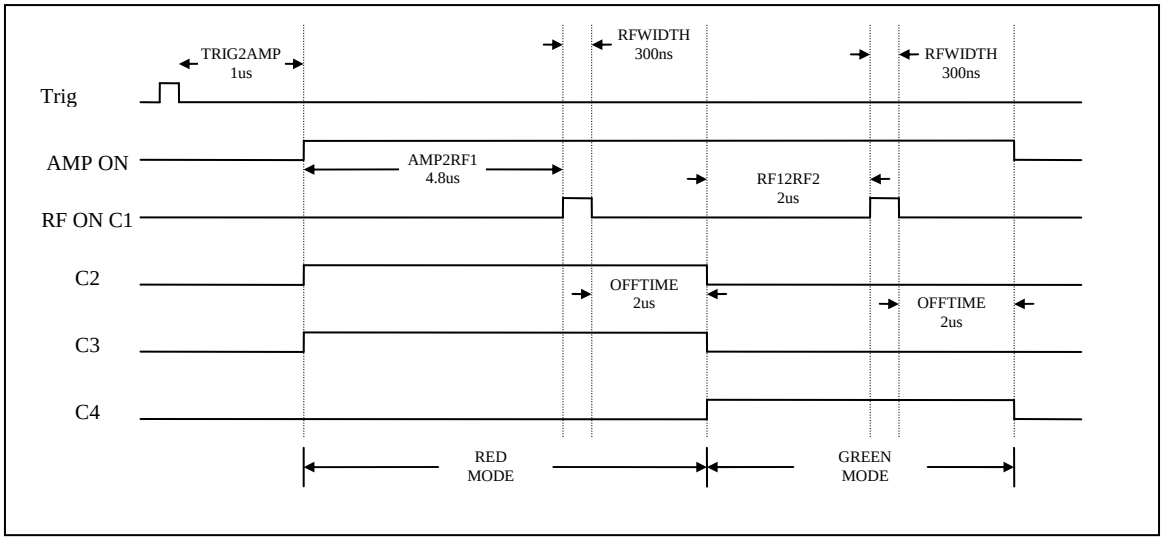
Boot Register (0xE) (Future Feature)

Bit	Name	Use	
[3]			
[2]	Reboot	Reboot XILINX	Reboot XILINX from the selected Prom.
[1]	SELECT	Boot Selection	‘0’ => Primary Boot Prom ‘1’ => Secondary Boot Prom
[0]	SEL_CLK	Set value of SEL Clock	Value of the SELECT bit is loaded into the select latch

JTAG Register (0xF) (Future Feature)

Bit	Name	Use		Default
[3]	TDO	TDO from PROM		
[2]	TCK	TCK to PROM		
[1]	TDI	TDI to PROM		
[0]	TMS	TMS to PROM		

Calibration Timing



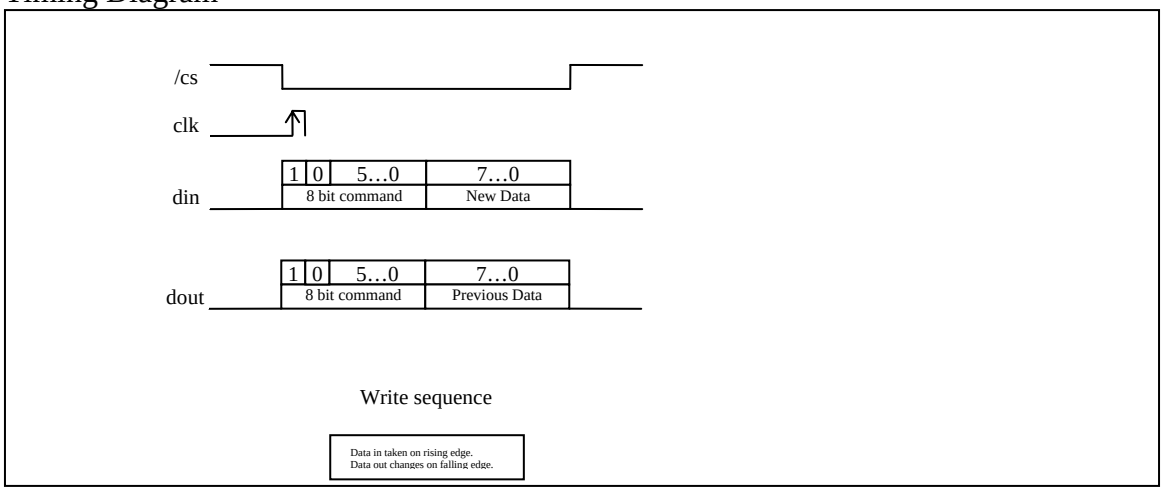
Trigger Handshake

QSPI CS2 and CS3 were converted into Trigger Handshake lines in Version 4. QSPI_CS3 is now a digital output that is latched high when the BPM receives a trigger. This signal is cleared by putting a high on QSPI_CS2, which is now an input.

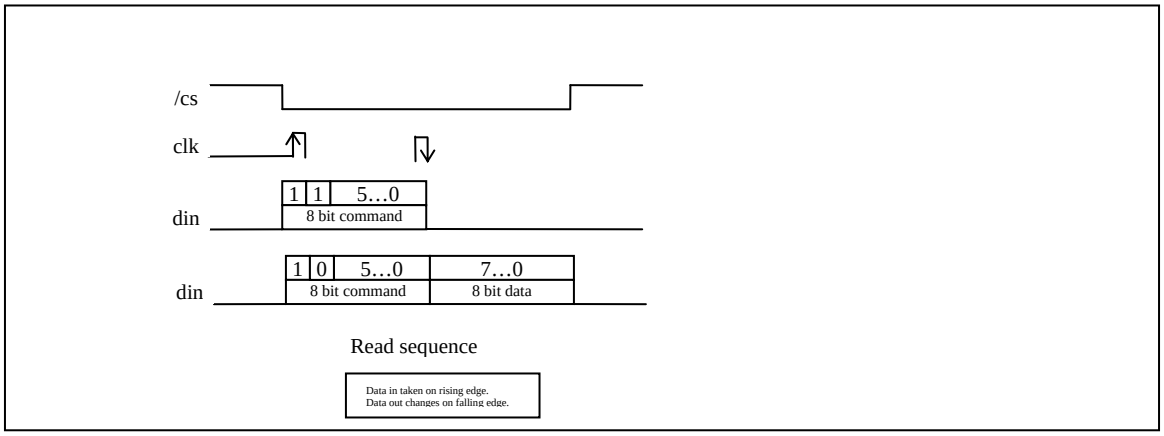
QSPI Interface

The QSPI interface uses a 2 byte format. The first byte is the command byte that indicates a read or write operation and the register value. The second byte is the data to read or write. The QSPI interface can run at up to 20Mhz clock rate.

Timing Diagram



During a write cycle, the 8 bit command is echoed back and the previous contents of the selected register is returned. The register is updated with the new data at the end of the cycle.



During a read cycle, the 8 bit command is echoed back and the current contents of the selected register is returned.

Command Format

Bit	Function			
[7]	Start Bit	‘1’		
[6]	R/W	‘1’ => Read Register ‘0’ => Write Register		
[5..0]	Register	Select Register to read or write		

Data Format

Bit	Function			
[7..0]	Data			

Hex ASCII RS232 Mode

The hex ASCII RS232 mode is meant for operation from a terminal emulator when the PAC module is not connected to do QSPI or Binary RS232 operation. The RS232 port operates at 115200Baud, Even Parity, 8 bit data, 1 stop bit.

Format 0XAADD <CRLF>

Where:

AA is the 6 bit Address in hex from 0 to 3F. The bit 6 indicates a write or a read.

0 => Write

1 => Read

DD is the 7 bit Data in hex from 00 to FF

Binary RS232 Mode (Obsolete in version 20)

The Binary RS232 mode is to be used by a computer interface, either the PAC or a smart terminal interface. The first byte has a ‘start’ bit in the MSB followed by a write or read bit, and then a 6 bit address field. Since none of the BPM registers are more than 7 bits, the second byte has a ‘0’ in the MSB followed by 7 bits of data.

Format AD
Where:

A

7	6	5..0
1	0 => Write 1 => Read	Register Address

D

7	6..0
0	Data

Revision History

Version	Date		
V00	10/25/06	Changed Trip from 4 to 1 bit	
	11/29/06	Moved ATT_CNTL1A1 from 180 to the correct pin 108	
	12/19/06	Updated the QSPI interface and documentation	
		Found all chip selects on the PAC connector were connected together.	Fixed layout
		RS232 Tx and Rx swapped	
		3.3 and 5.0 volt sides of the buffers were swapped.	
V03	01/18/07	Added registers to control timing	
		60Mhz only operation	
	02/13/07	Inverted long and short reset outputs	
V04	03/05/07	Added Trigger/Trigger Ack handshake. Used QSPI CS3 for Trigger Set, QSPI CS2 for Trigger Reset	
		Changed design to use 60Mhz X 2 to reduce jitter. Was 60Mhz/2 Multiply Timing parameters by 4 by adding 2 zeros before the counters.	
		Compile time ~ 3.0min	
V20	12/13/07	Added Calibration Oscillator control in CSR	
		Changed ATT2 from 4 to 5 bit	
		Saturate Attenuator registers	
V21	10/23/08	Put Attenuators to full scale during calibration	