



1. Description

1.1. Project

Project Name	AudioCat
Board Name	NUCLEO-U5A5ZJ-Q
Generated with:	STM32CubeMX 6.9.2
Date	09/22/2023

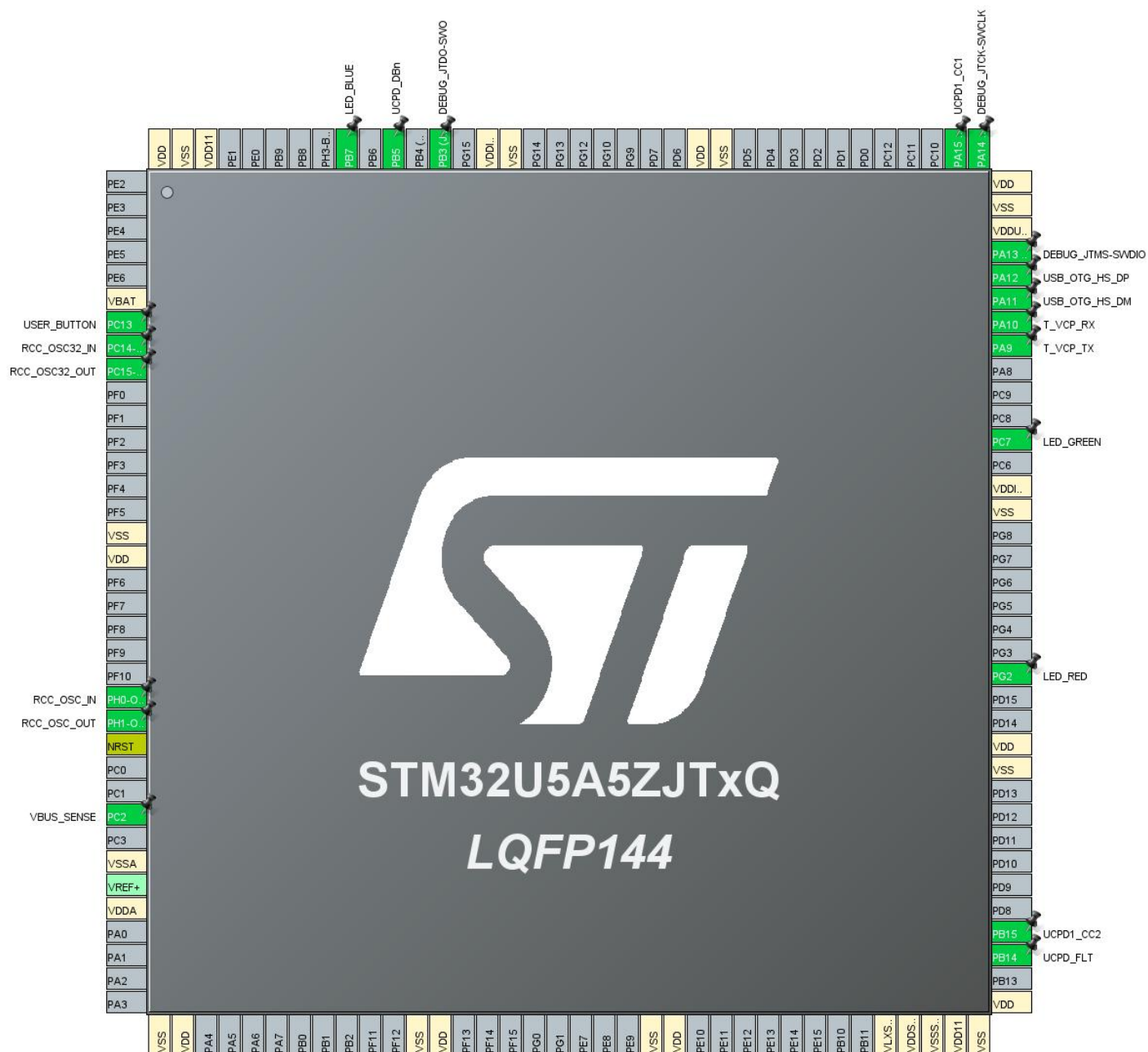
1.2. MCU

MCU Series	STM32U5
MCU Line	STM32U595/5A5
MCU name	STM32U5A5ZJTxD
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	ARM Cortex-M33
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2. Pinout Configuration



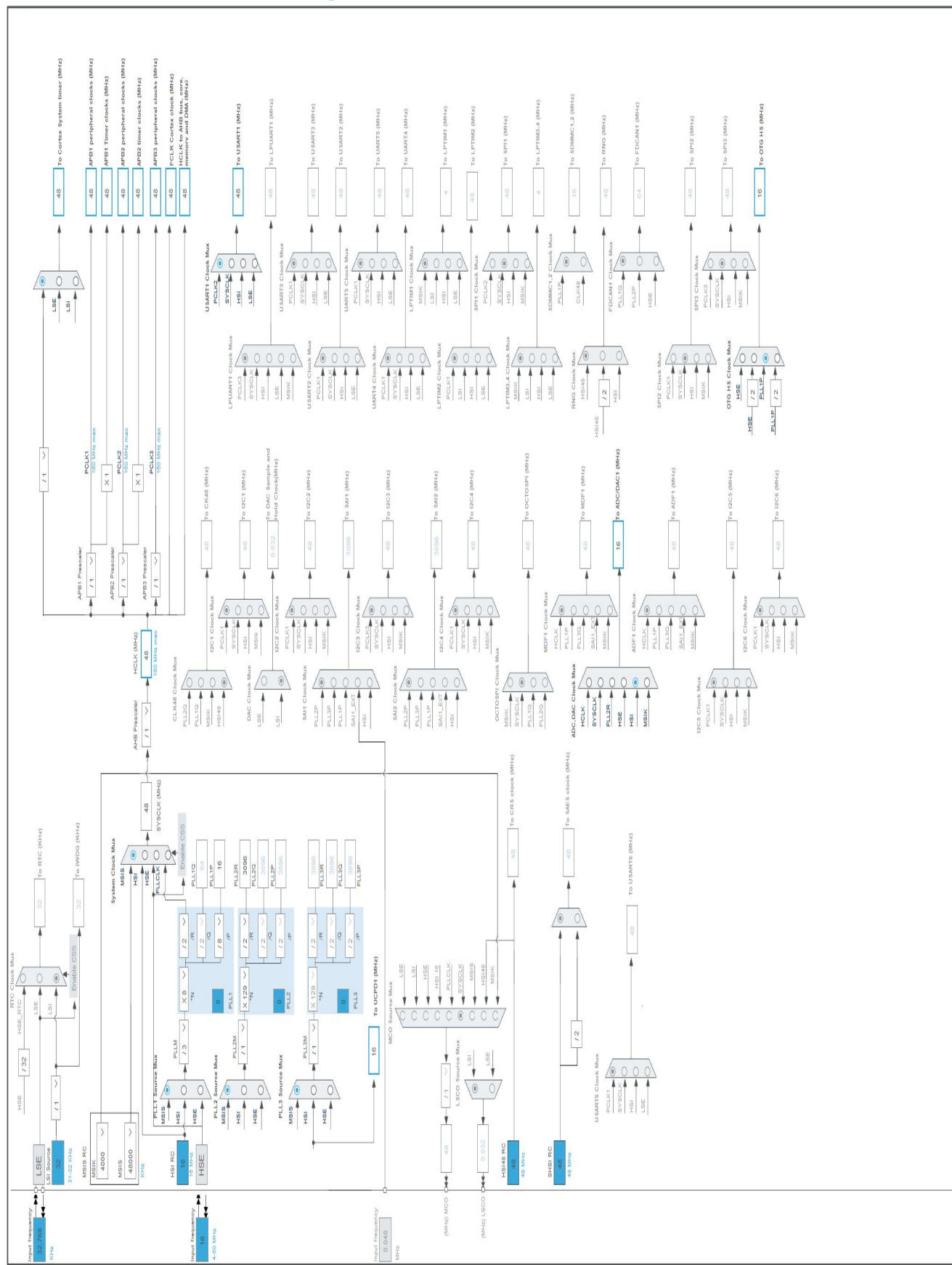
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	USER_BUTTON
8	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
16	VSS	Power		
17	VDD	Power		
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
25	NRST	Reset		
28	PC2	I/O	ADC1_IN3	VBUS_SENSE
30	VSSA	Power		
32	VDDA	Power		
37	VSS	Power		
38	VDD	Power		
48	VSS	Power		
49	VDD	Power		
58	VSS	Power		
59	VDD	Power		
68	VLXSMPS	Power		
69	VDDSMPS	Power		
70	VSSSMPS	Power		
71	VDD11	Power		
72	VSS	Power		
73	VDD	Power		
75	PB14 *	I/O	GPIO_Input	UCPD_FLT
76	PB15	I/O	UCPD1_CC2	
83	VSS	Power		
84	VDD	Power		
87	PG2 *	I/O	GPIO_Output	LED_RED
94	VSS	Power		
95	VDDIO2	Power		
97	PC7 *	I/O	GPIO_Output	LED_GREEN
101	PA9	I/O	USART1_TX	T_VCP_TX
102	PA10	I/O	USART1_RX	T_VCP_RX
103	PA11	I/O	USB_OTG_HS_DM	
104	PA12	I/O	USB_OTG_HS_DP	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
105	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
106	VDDUSB	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
110	PA15 (JTDI)	I/O	UCPD1_CC1	
120	VSS	Power		
121	VDD	Power		
129	VSS	Power		
130	VDDIO2	Power		
132	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	
134	PB5 *	I/O	GPIO_Output	UCPD_DBN
136	PB7 *	I/O	GPIO_Output	LED_BLUE
142	VDD11	Power		
143	VSS	Power		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	AudioCat
Project Folder	C:\Users\Shraddha BLS\STM32CubeIDE\workspace_1.13.2\AudioCat
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_U5 V1.3.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC1_Init	ADC1
4	MX_ICACHE_Init	ICACHE
5	MX_UCPD1_Init	UCPD1
6	MX_USART1_UART_Init	USART1
7	MX_USB_OTG_HS_HCD_Init	USB_OTG_HS
8	MX_MEMORYMAP_Init	MEMORYMAP

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32U5
Line	STM32U595/5A5
MCU	STM32U5A5ZJTxxQ
Datasheet	not yet available

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

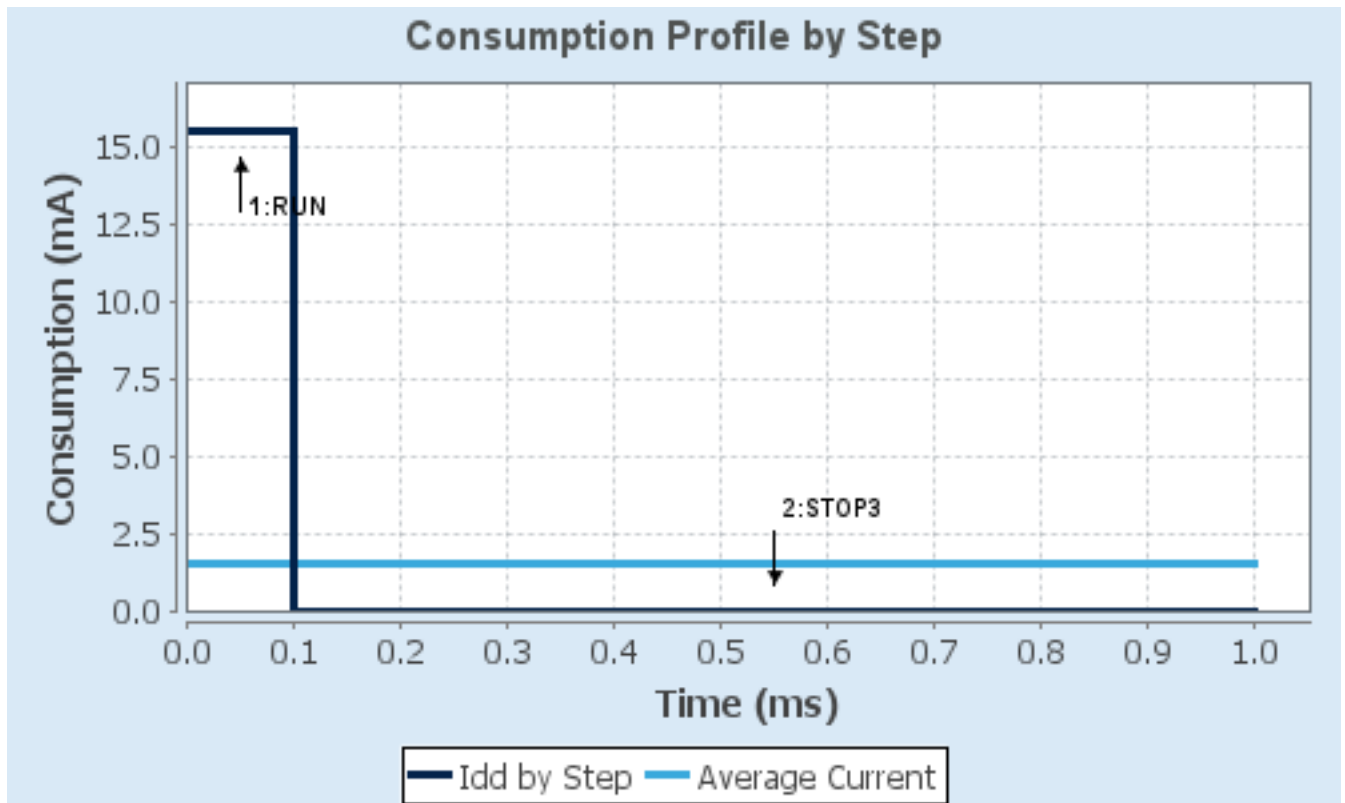
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP3
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Medium	NoRange/SMPS
Fetch Type	FLASH- PwrDwnBank2/ART/Cache- 2Ways/AlgoType- ReducedCode	FLASH
CPU Frequency	160 MHz	0 Hz
Clock Configuration	HSE BYP PLL ALL RAM RETENTION	ALL_CLOCKS_OFF
Clock Source Frequency	16 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	15.5 mA	1.85 μ A
Duration	0.1 ms	0.9 ms
DMIPS	240.0	0.0
Ta Max	138.42	140
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	1.55 mA
Battery Life	2 months, 30 days, 5 hours	Average DMIPS	24.0 DMIPS

1.6. Chart



2. Peripherals and Middlewares Configuration

2.1. ADC1

IN3: IN3 Single-ended

2.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 14-bit resolution

Data Alignment Right alignment

Gain Compensation 0

Scan Conversion Mode Disabled

End Of Conversion Selection End of single conversion

Low Power Auto Wait Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

Overrun behaviour Overrun data preserved

Trigger Frequency High frequency

Conversion Data Management Mode Regular Conversion data stored in DR register only

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable

Enable Regular Oversampling Disable

Oversampling Ratio 1

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Left Bit Shift No bit shift

Rank 1

Channel Channel 3

Sampling Time 5 Cycles

Offset Number No offset

Monitored by None

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

2.2. DEBUG

Debug: Trace Asynchronous Sw

2.3. ICACHE

Mode: 1-way (direct mapped cache)

2.4. LPBAM

mode: LPBAM Scenario uses resources from Smart Run Domain only

mode: LPBAM Scenario is hosted by LPDMA1

2.5. LPBAMQUEUE

mode: QUEUE MODE

2.5.1. Parameter Settings:

DMA Channel Configuration:

Priority Low

DMA Channel Interrupt Configuration:

Data Transfer Error Interrupt Disable

Update Link Error Interrupt Disable

User Setting Error Interrupt Disable

Transfer Complete Interrupt Disable

Trigger Overrun Interrupt Disable

2.6. MEMORYMAP

mode: Activated

2.7. PWR

mode: Dead Battery Signals disabled

mode: Power saving mode

mode: Privilege attributes

mode: Control Vdda isolation

2.7.1. Power Saving:

System power supply:

Power Regulator

SMPS *

SRAM power down in Run mode:

SRAM1 power down in Run mode	Disable
SRAM2 power down in Run mode	Disable
SRAM3 power down in Run mode	Disable
SRAM4 power down in Run mode	Disable
SRAM5 power down in Run mode	Disable

SRAM power down in Stop mode:

SRAM1 Page1 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page2 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page3 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page4 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page5 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page6 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page7 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page8 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page9 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page10 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page11 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page12 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM2 Page1 power down in Stop (0, 1, 2) mode	Disable
SRAM2 Page2 power down in Stop (0, 1, 2) mode	Disable
SRAM3 Page1 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page2 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page3 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page4 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page5 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page6 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page7 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page8 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page9 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page10 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page11 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page12 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page13 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM4 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page1 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page2 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page3 power down in Stop (0, 1, 2, 3) mode	Disable

SRAM5 Page4 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page5 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page6 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page7 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page8 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page9 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page10 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page11 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page12 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page13 power down in Stop (0, 1, 2, 3) mode	Disable
ICACHE power down in Stop (0, 1, 2, 3) mode	Disable
DCACHE1 power down in Stop (0, 1, 2, 3) mode	Disable
DCACHE2 power down in Stop (0, 1, 2, 3) mode	Disable
DMA2D RAM power down in Stop (0, 1, 2, 3) mode	Disable
PKA32 RAM power down in Stop (0, 1, 2, 3) mode	Disable
PERIPH RAM power down in Stop (0, 1, 2, 3) mode	Disable
GRAPHIC PRAM power down in Stop (0, 1, 2, 3) mode	Disable
DSI RAM power down in Stop (0, 1, 2, 3) mode	Disable
SRAM fast wakeup:	
SRAM4 fast wakeup from Stop (0, 1, 2, 3) modes	Disable

2.7.2. PWR Privilege :

Privilege PWR:

PWR Privilege	Disable
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2.8. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

2.8.1. RCC Privilege :

Privilege RCC:

Privilege of RCC Non-Secure Items	Disable
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2.8.2. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
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Flash Latency(WS) 1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
MSI Calibration Value 16
MSIS/MSIK Auto Calibration Disabled
HSE Startup Timeout Value (ms) 100
LSE Startup Timeout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 3

PLL1/2/3 Parameters:

PLL1M BOOST EPOD Clock Divider 4
PLL1 input frequency range Between 8 and 16 MHz

Low Power Parameters:

MSI in Stop mode Disabled
HSI in Stop mode Disabled

2.9. SYS

Timebase Source: SysTick

2.10. UCPD1

UCPD Mode: Sink

2.10.1. Parameter Settings:

Version 1.0

2.11. USART1

Mode: Asynchronous

2.11.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200
Word Length 8 Bits (including Parity)
Parity None
Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit
Over Sampling 16 Samples

Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration
Autonomous Mode	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.12. USB_OTG_HS

Internal HS Phy: Host_Only

2.12.1. Parameter Settings:

Host Channels	16
Speed	High Speed 480MBit/s
Enable internal IP DMA	Disabled
Physical interface	Internal HS Phy
Use external vbus	Enabled
Signal start of frame	Disabled

OTG PHY reference clock selection:

Ref Clock Selection	16 Mhz
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* User modified value

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC2	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	VBUS_SENSE
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
	PB3 (JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
UCPD1	PB15	UCPD1_CC2	Analog mode	No pull-up and no pull-down	n/a	
	PA15 (JTDI)	UCPD1_CC1	Analog mode	No pull-up and no pull-down	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	T_VCP_TX
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	T_VCP_RX
USB_OTG_HS	PA11	USB_OTG_HS_DM	n/a	n/a	n/a	
	PA12	USB_OTG_HS_DP	n/a	n/a	n/a	
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USER_BUTTON
	PB14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	UCPD_FLT
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RED
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GREEN
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UCPD_DBn
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_BLUE

3.2. GPDMA1

3.3. LINKEDLIST

3.4. LPDMA1

3.5. NVIC configuration

3.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
Flash non-secure global interrupt	unused		
RCC non-secure global interrupt	unused		
EXTI Line13 interrupt	unused		
ADC1_2 global interrupt	unused		
USART1 global interrupt	unused		
USB OTG HS global interrupt	unused		
FPU global interrupt	unused		
UCPD1 global interrupt	unused		
Instruction cache global interrupt	unused		

3.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

* User modified value

4. System Views

4.1. Category view

4.1.1. Current

Middleware

System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Thermal	Utilities	Other
CORTEX_M33 ✓	ADC1 ✓		UCPD1 ✓				DEBUG ✓	PWR ✓	LINKEDLIST	
GPDMA1			USART1 ✓							
GPIO ✓			USB_HS ✓							
ICACHE ✓										
LPDMA1										
NVIC ✓										
RCC ✓										
SYS ✓										

5. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32u5_bsd.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32u5_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32u5_svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32u5_series_product_overview.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32ulp.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32u5.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2834-how-to-get-the-best-adc-accuracy-in-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2867-oscillator-

design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3236-increase-the-number-of-touchkeys-for-touch-sensing-applications-on-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3960-esd-considerations-for-touch-sensing-applications-on-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4013-stm32-crossseries-timer-overview-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4229-how-to-implement-a-vocoder-solution-using-stm32-microcontrollers-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4277-using-stm32-device-pwm-shutdown-features-for-motor-control-and-digital-power-conversion-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4299-improve-conducted-noise-robustness-for-touch-sensing-applications-on-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4310-sampling-capacitor-selection-guide-for-touch-sensing-applications-on-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4312-design-with-

surface-sensors-for-touch-sensing-applications-on-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4316-tuning-a-touch-sensing-application-on-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4635-minimization-of-power-consumption-using-lpuart-for-stm32-microcontrollers-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4759-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-microcontrollers-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4776-generalpurpose-timer-cookbook-for-stm32-microcontrollers-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4803-highspeed-si-simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4861-lcdtft-display-controller-ltdc-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4894-eeeprom-emulation-techniques-and-software-for-stm32-microcontrollers-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4908-stm32-usart-automatic-baud-rate-detection-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4989-stm32-microcontroller-debug-toolbox-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4992-stm32-mcus-secure-firmware-install-sfi-overview-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5020-digital-camera-interface-dcmi-on-stm32-mcus-stmicroelectronics.pdf

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