

Electromagnetic Calorimeter System Operations Manual

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Abstract

This document provides an overview of the CLAS12 Electromagnetic Calorimeter (EC) System and serves as an Operations Manual for the detector. Instructions are provided for shift workers related to basic steps of operating and monitoring the HV controls, monitoring the detector system and responding to alarms, and knowing when to contact the on-call personnel. More complete details are also provided for EC system experts regarding the channel mapping to the readout electronics, the cable connections and routing in Hall B, higher-order high voltage system operations, and detector servicing. This document also provides references to the available EC documentation and a list of personnel authorized to perform EC system repairs and modify system settings.

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1 EC Overview

The CLAS12 EC package includes the legacy CLAS6 electromagnetic calorimeters (ECAL) and new pre-shower calorimeter (PCAL) modules installed just upstream of ECAL. Six sectors of EC in CLAS12 will be used primarily for identification of electrons, photons (including $\pi^0 \rightarrow 2\gamma$ decays), and neutrons. Both PCAL and ECAL are triangular-shaped sampling calorimeters. The calorimeter design uses a lead-scintillator sandwich consisting of alternating layers of 1-cm thick scintillators and 2 mm thick lead sheets. At 11 GeV the total thickness corresponds to about 21 radiation lengths. Scintillator layers are grouped into three stereo views, called U, V, and W, which are readout using photomultiplier tubes (PMT). Specifications for each calorimeter are outlined below.

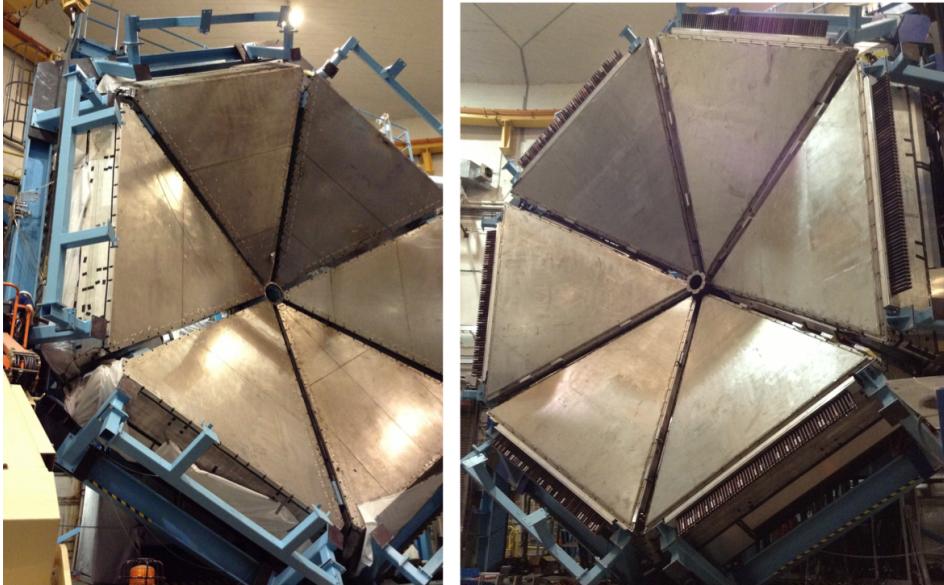


Figure 1.1: Photographs of the ECAL (left) and PCAL (right) calorimeter modules installed on the Forward Carriage in Hall B. The Forward Carriage is roughly 10 m in diameter.

Parameter	Design Value
PCAL	
Calorimeter type	Sampling, lead-scintillator
Number of modules	6
Module shape and dimensions	Triangle, base 394.3 cm height 385.3 cm
Total coverage area	45 m ²
Distance from Target	7.0 m
Angular coverage	$\theta: 5^\circ \rightarrow 35^\circ, \phi: 50\% \text{ at } 5^\circ \rightarrow 85\% \text{ at } 35^\circ$
Lead sheets	2.2 mm thick (two pieces)
Number of scintillator layers	15 per module
Number of lead sheets	14 per module
Number of stereo readout views	3 (5 scintillator layers per view)
Scintillator material	Extruded polystyrene w/ 2 fiber holes
Scintillator core	Dow Styron 663 W
Scintillator cladding	Polystyrene with 12% TiO ₂ (0.25 mm)
Scintillator strip dimensions	1 x 4.5 x 2.5-394(U)432(V,W) cm
Scintillator readout	WLS fibers (Kuraray Y-11 1mm DC)
Scintillators/module	U:84 V:77 W:77
Scintillators readout/module	U:68 V:62 W:62
Number of WLS fibers	4 fibers/strip 1428/module
Number of readout channels	192 per module
Readout PMT	Hamamatsu R6095
Light yield	11-12 photo e-/MeV

Table 1: PCAL technical design parameters.

Parameter	Design Value
ECAL	
Calorimeter type	Sampling, lead-scintillator
Number of modules	6 (each module has inner/outer segmentation and readout)
Module shape and dimensions	Triangle, base 420 cm height 388.8 cm
Total Coverage Area	49 m ²
Distance from Target	7.5 m (target center to upstream face)
Angular Coverage	$\theta: 5^\circ \rightarrow 35^\circ, \phi: 50\% \text{ at } 5^\circ \rightarrow 85\% \text{ at } 35^\circ$
Lead sheets	2.387 mm thick (single piece)
Number of scintillator layers	39 per module (15 inner, 24 outer)
Number of lead sheets	38 per module
Number of stereo readout views	3 (5/8 scintillator layers per view for inner/outer)
Scintillator material	BC-412
Scintillator cladding	None. Teflon film (0.00762 cm) between layers.
Scintillator strip dimensions	1 x 10.0 x 15-420 cm
Scintillator readout	BCF98 3mm cladded optical fiber
Scintillators/module	U:36 V:36 W:36
Number of fibers	22 fibers per PMT, 110/176 per inner/outer view
Number of readout channels	216 per module
Readout PMTs	Phillips XP2262 and EMI 9954
Light yield	3-4 photo e-/MeV
Expected Performance	Value
Energy resolution	10%/ \sqrt{E} (ECAL+PCAL)
Position resolution	0.5 cm
Time resolution	500 ps

Table 2: ECAL technical design parameters.

A block diagram of the readout electronics for the EC system is shown in Figure 1.2. Signal cables are routed from the PMT locations on the calorimeter modules to UVA 122B splitter panels located on the front of the electronics racks. The cable connections are BNC at the PMT anode and LEMO at the splitter. From the splitter, patch cables are routed to VME DSC2 leading edge discriminators (for pulse timing measurements) and JLAB 250 MHz VME Flash ADCs (FADC250) (for pulse amplitude measurements.) The TDCs are CAEN VME 1190A with 100 ps LSB resolution. The FADC250 and DSC2/TDC modules are housed in separate VXS crates. The FADC250/VXS crate contains the Virtual Trigger Processor (VTP) in a special switched slot which will be used to process energy and hit data for trigger decision making.

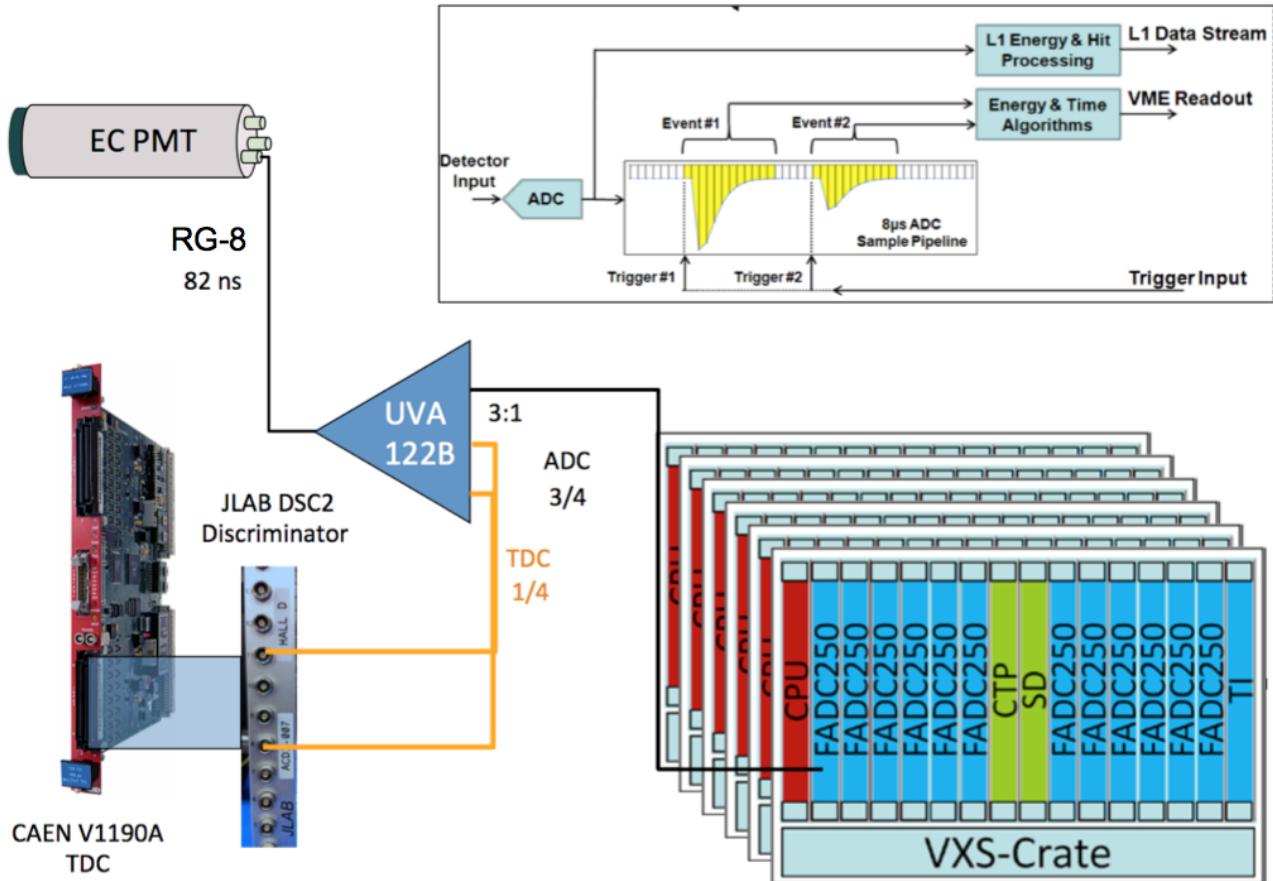


Figure 1.2: Schematic of signal readout electronics for ECAL system. Shown are the cable and split ratios for the ECAL PMTs. The PCAL case is similar but uses different split ratios. Not shown are HV connections. For ECAL transition patch cables were used at either end of the RG-8 signal cable, which are not shown here.

The electronics for each sector are located behind the detectors on the three levels of the Forward Carriage as follows:

- EC S1: FC Level 2 South (Beam left)
- EC S2: FC Level 3 South (Beam left)
- EC S3: FC Level 3 North (Beam right)
- EC S4: FC Level 2 North (Beam right)
- EC S5: FC Level 1 North (Beam right)
- EC S6: FC Level 1 South (Beam left)

Note that “South” refers to beam left and “North” to beam right (closer to the Pie Tower).

Figure 1.3 shows the Forward Carriage rack locations for the ECAL VME electronics and signal cable patch panels. Note the rack layout for beam left is a mirror image of the layout for beam right. Also the Level 1 rack

layout is different due to an alternate cable routing (discussed later). A photograph of the Sector 6 rack installation is shown in Figure 1.4.

The HV power supplies for all PMTs in each ECAL sector are either CAEN 1527LC mainframes or CAEN 4527 mainframes outfitted with negative polarity 24-channel A1535N cards which fit into slots at the rear of each mainframe. The HV mainframes that power the PCAL system are actually shared between the FTOF and the PCAL. The FTOF boards occupy slots 0 to 7 of each mainframe and the PCAL boards occupy slots 8 to 15 of each mainframe. These supplies are named HVFTOF n , $n=1\rightarrow 6$ (i.e. HVFTOF1 → HVFTOF6). The HV mainframes for the EC modules are named HVECAL n ($n=1\rightarrow 6$). Figure 1.3 shows the locations of the HV mainframes for each of the EC sectors on the Forward Carriage.

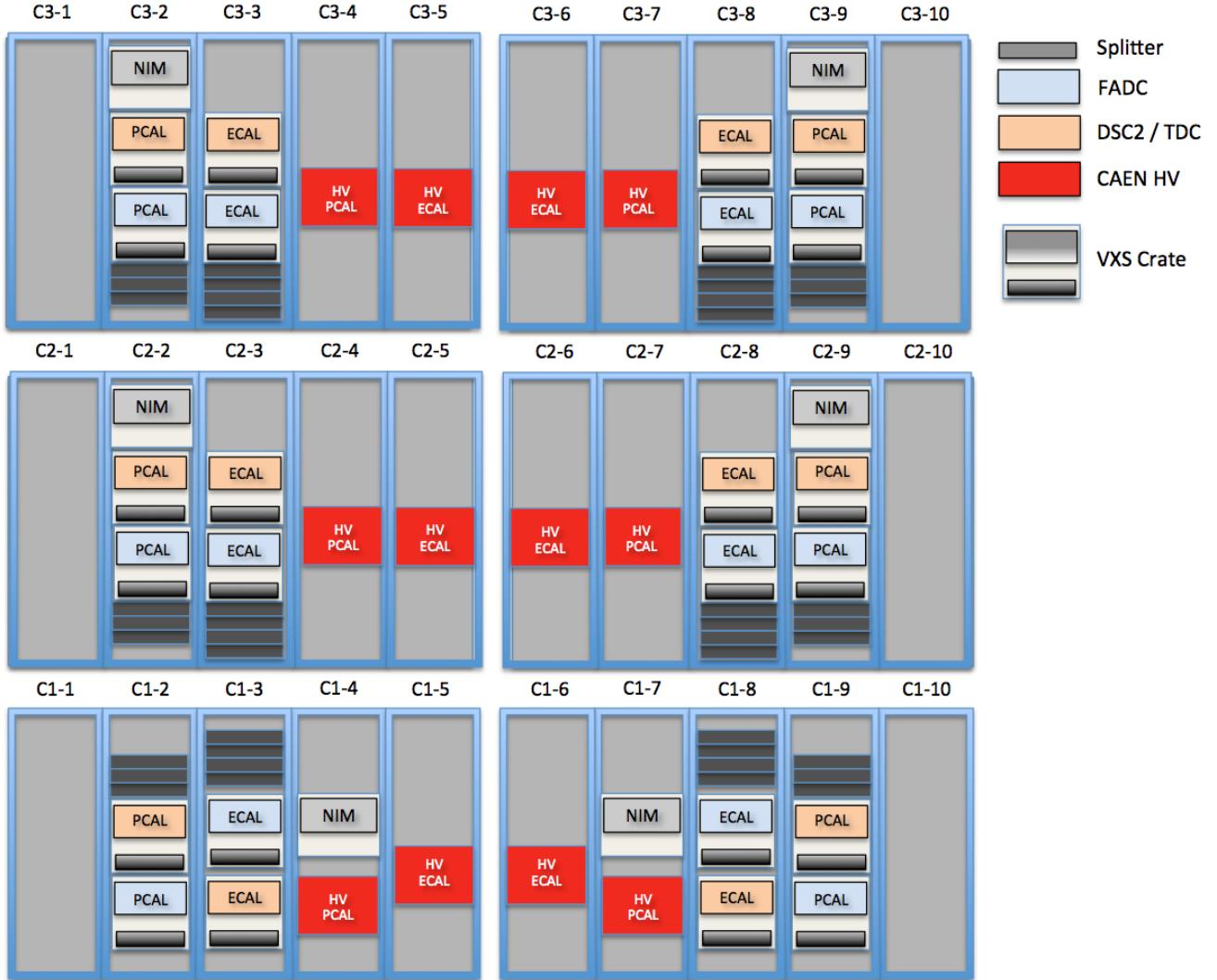


Figure 1.3: Schematic layout of the EC VME electronics, signal cable splitters, and HV power supplies in the electronics racks on each of the three levels of the Forward Carriage. The rack names on each level (c1, c2, and c3) are numbered 1 through 10.



Figure 1.4: Photograph of racks C1-6 through C1-10 (Sector 6) during cable installation. The rack with no cables installed (C1-8) houses four ECAL splitter panels (top), the FADC250 VXS crate (middle) and DSC2/TDC VXS crate (bottom). The CAEN HV mainframe *hvecal6* is at far left in rack C1-6, and the PCAL/FTOF mainframe *hvftof6* is to the right in rack C1-7.

2 Information for Shift Workers

2.1 Shift Worker Responsibilities

The shift worker in the Hall B Counting House has five responsibilities with regard to the EC system:

1. Updating the Hall B electronic logbook with records of problems or system conditions (see Section 2.1.1).
2. Contacting EC system on-called personnel for any problems that are discovered (see Section 2.1.2).
3. Responding to EC system alarms from the Hall B alarm handler (see Section 2.1.3).
4. Turning on or off the high voltage for the EC system using the HV control interface (see Section 2.2).
5. Monitoring the hit occupancy scalers for the system (see Section 2.3).

2.1.1 Updating the Logbook

The electronic logbook HBLOG:

<https://logbooks.jlab.org/book/HBLOG>

is set up to run on a specified terminal in the Hall B Counting House. Shift workers are responsible for keeping an up-to-date and accurate record of any problems or issues concerning the EC system. For any questions regarding the logbook, its usage, or on what is considered to be a “logbook worthy” entry, consult the assigned shift leader.

Note the shift worker should follow all posted or communicated instructions about entering ECAL scaler screens into the e-log. This is typically done once per 8-hour shift as directed on the shift checklist.

2.1.2 Contacting EC System Personnel

As a general rule, shift workers should spend no more than 10 to 15 minutes attempting to solve any problem that arises with the EC system. At that point they should contact the assigned EC on-call worker to either provide advice on how to proceed or to address the problem. **The EC on-call phone number is (757)-810-1489.**

This document is divided into a section for shift workers and EC system experts. Only EC system experts (as listed in Section 5) are authorized to make changes to the EC parameter settings, to work on the hardware or electronics, or to modify the DAQ system software. This division between shift worker responsibilities and expert responsibilities is essential in order to protect and safeguard the equipment, to ensure data collection is as efficient as possible, and to minimize down time. If the shift worker has any question regarding how to proceed when an issue arises, the shift leader should be consulted.

2.1.3 Hall B Alarm Handler

The BEAST alarm handler system running in the Counting House monitors the entire Hall B Slow Controls system. This include HV and LV systems, gas systems, torus and solenoid controls, subsystem environment controls (e.g. temperature, humidity), and pulser calibration systems (among several others). The system runs on a dedicated terminal in the Counting House. One of the main responsibilities of the shift worker is to respond to alarms from this system, either by taking corrective action or contacting the appropriate on-call personnel. Instructions and details on the alarm handler for Hall B are given in Ref. [2].

For the EC system, the only element of the system monitored by the alarm handler is the HV system. Whenever any PMT HV either trips off or changes beyond a pre-determined window an alarm will sound. The alarm handler will identify the specific channel (or channels) causing the alarm. These channels can be reset either through the alarm handler or through the nominal EC HV control screens. These channels should be reset only after identifying the cause of the alarm. Beam-current related trips can be reset immediately once beam conditions have stabilized. Instability in the HV due to a malfunction in the PMT, HV divider or HV power supply should be diagnosed and noted in the e-log so repairs can be made at the next Hall entry.

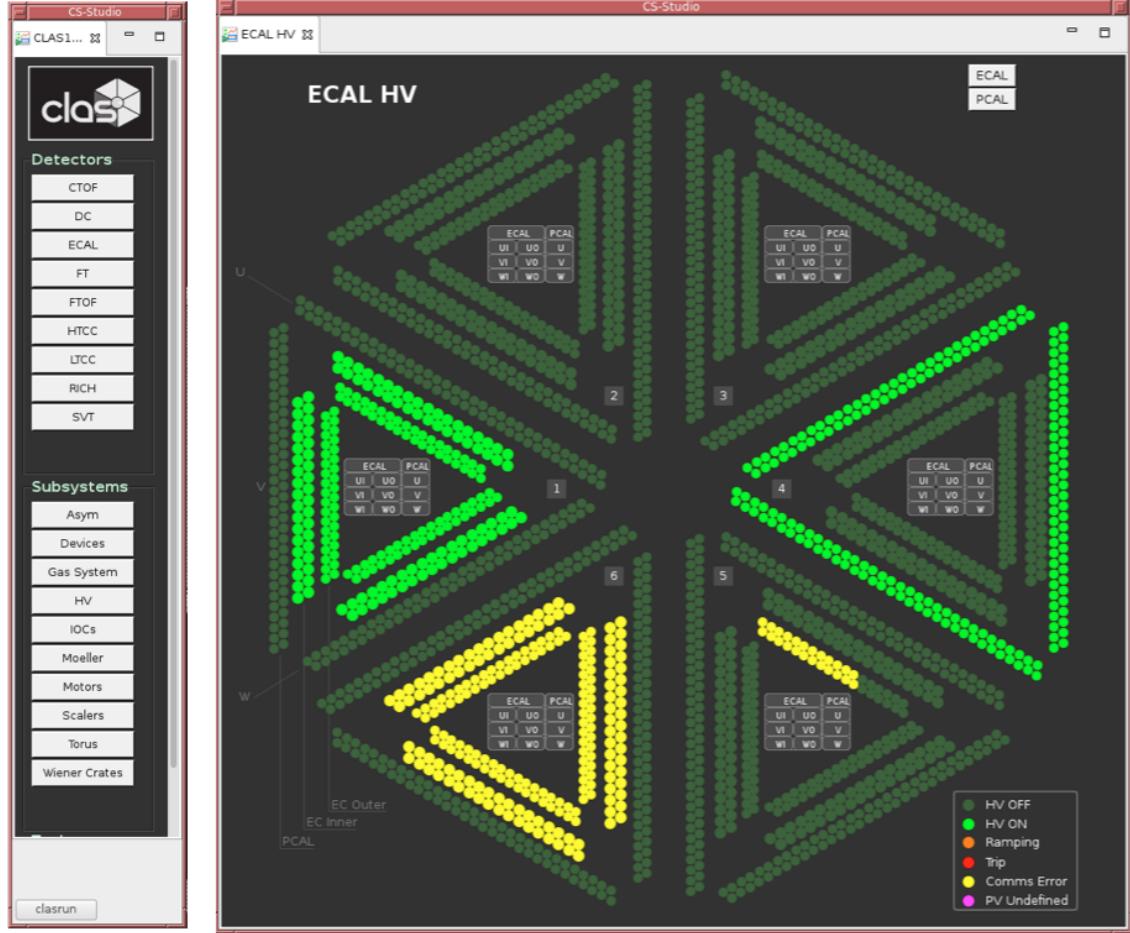


Figure 2.1: Left: The CS-Studio interface used for the Slow Controls of the CLAS12 detectors and subsystems. ECAL HV controls may be accessed through either the “ECAL” button under Detectors or the “HV” button under Subsystems. Right: Detector based ECAL HV display and control interface. For each sector the outermost triangle represents the PCAL, while ECinner and ECouter are the middle and innermost triangles respectively. Individual PMT HV channel controls are indicated by small circles. HV channel status is indicated by the colormap at lower right. An entire sector of PMTs (EC+PCAL) may be turned on and off by clicking the sector number at the apex of the triangle.

2.2 High Voltage Controls

Control of the EC HV mainframes is through the Hall B CS-Studio suite, which is an Eclipse-based collection of tools used as an interface to the EPICS Slow Control system. To start the user interface on any terminal in the Hall B Counting House, enter the command `clascss`. Figure 2.1 shows the control panel that is launched.

HV controls are presented in two ways: either mapped to the physical detector (sector,layer,component) or mapped to the HV mainframe (crate,slot,channel). To access detector-based EC HV controls, click on the “ECAL” button on the Detectors list. This pops up a sub-menu of all Slow Controls subprograms for the ECAL system. Clicking on “EC HV” will bring up the HV control panel shown in Figure 2.1 (right). This interface allows simple ON/OFF HV operations which are detailed in Figure 2.2.

For the shift worker the most common operations are turning off and on large groups of PMTs. These group operations are accessed via the pop-up menus which appear when clicking on the labels shown in Figure 2.2 and described below:

1. Turning on and off all PMTs within a single sector.
2. Turning on and off all PMTs within a single calorimeter (ECAL or PCAL).
3. Turning on and off all PMTs within a single U,V,W view of a single calorimeter.

In addition to group ON/OFF operations it may be occasionally necessary to access single PMTs in order to enable, disable, change the HV or alter various set-points for that specific PMT. This is accomplished by either clicking on the “Controls” selection in Figure 2.2 which brings up all PMTs corresponding to a (U,V,W) view, or clicking on the circular icon corresponding to the desired PMT (see Figure 2.3) to bring up just the panel for that PMT.

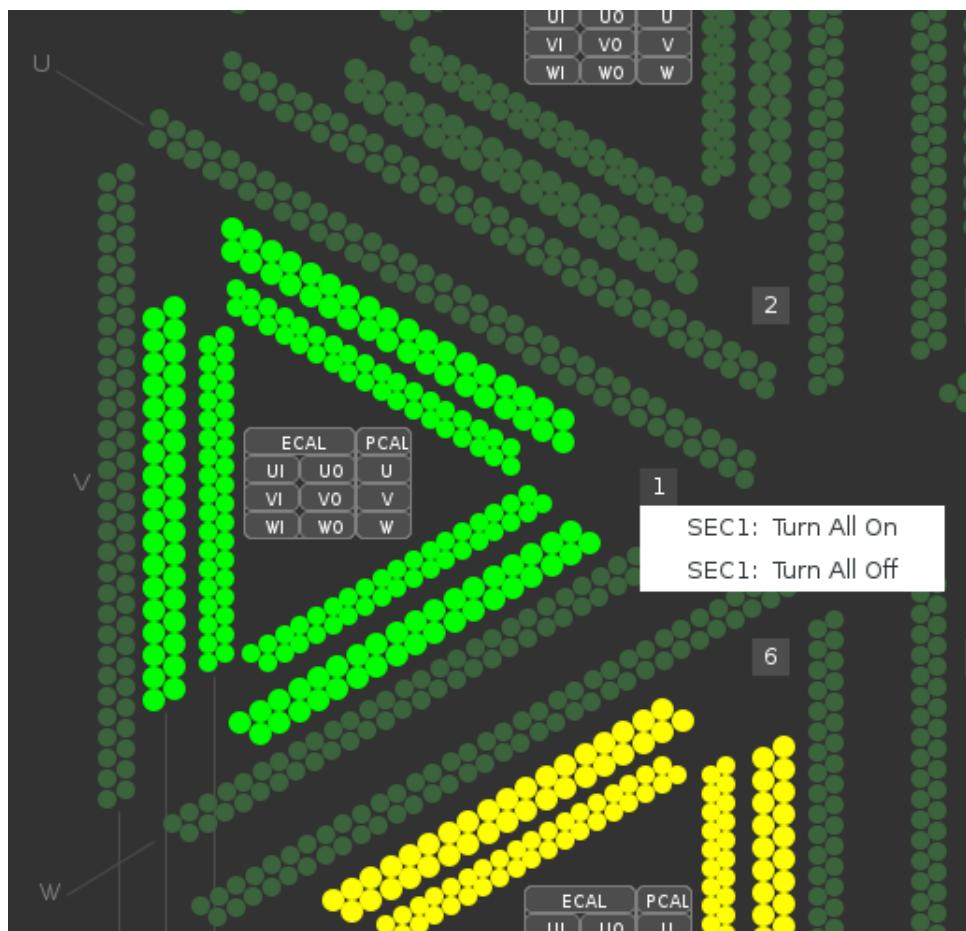


Figure 2.2: Detail of Fig. 2.1 which shows sector “1” has been selected, activating the pop-up option menu. Individual controls for modules are labeled “ECAL”, “PCAL” and for individual views “U,V,W” which provide similar pop-up menus as shown. Control of individual PMTs within a view is possible by clicking the circular elements.

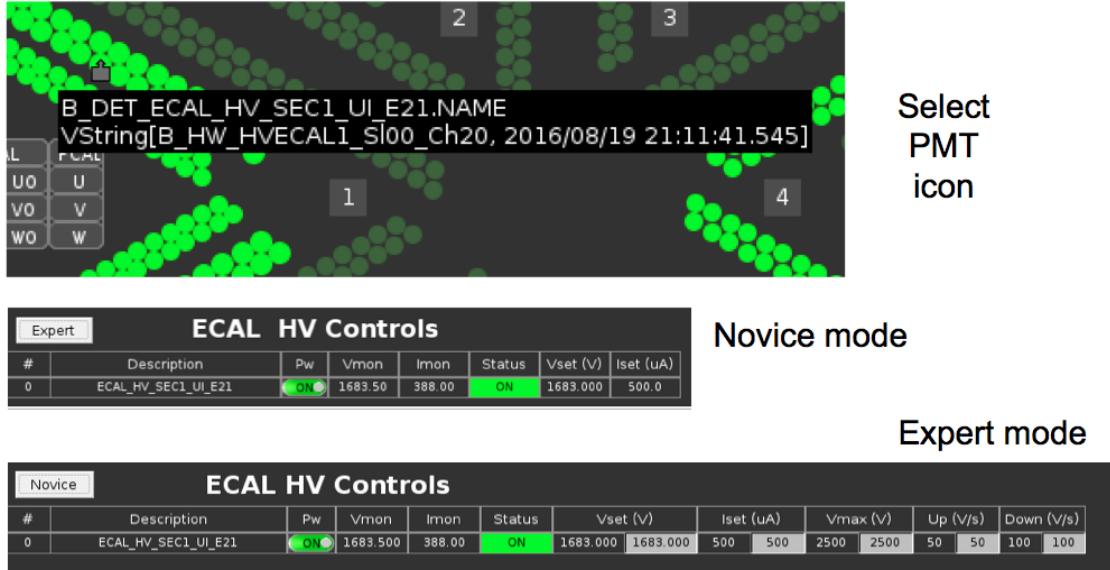


Figure 2.3: ECAL HV displays for single PMT HV controls. Hover the mouse over the PMT icons to view popup of EPICS Property Value (PV) identifier. Select the desired PMT to bring up Novice mode controls (middle) which allow only OFF/ON control via the Pw (power) button. Click Expert button to bring up controls for voltage (Vset), maximum HV divider current (Iset), maximum HV (Vmax), HV ramp rates (Up,Down). Note these settings apply only to the PMT selected, not all PMTs.

If a single PMT is selected, a window similar to Fig. 2.3 (middle) is displayed. This window shows the monitored channel voltage and current V_{mon} (V) and I_{set} (μ A), the channel status (OFF, ON), and the demand or set channel voltage V_{set} (V). Also shown is the maximum permissible HV divider current I_{set} (μ A). This interface would be used by shift workers to enable or disable a PMT via the Pw button.

In the upper left corner of the window is a button marked “Expert” that brings up the window shown at the bottom of Fig. 2.3. This window allows changes to the system settings for the maximum channel current, maximum channel voltage setting, and the channel HV ramp up and ramp down rates. Clicking on the “Novice” button in the upper left corner toggles between the expert and novice screens. **The expert screen should only be used by the list of authorized EC personnel given in Section 5.**

The HV Control Interface screen (see Fig. 2.1) also provides a color key to indicate the channel status:

- HV off - no highlight color (channel color dark green)
- HV on - bright green
- HV ramping up or ramping down - orange
- HV trip - red
- Communication problem - yellow
- Undefined channel status - magenta

When HV controls are unresponsive or HV monitoring stripcharts appear to become static it is likely to be an EPICS communication error due to an IOC process that cannot communicate with the hardware or a server. Sometimes the hardware is at fault and has to be rebooted or power-cycled. Usually this requires an IOC reboot. Controls for monitoring IOC status and rebooting frozen IOCs are available from several menus. For the EC HV system the IOC screen can be reached from the CSS menu via the “IOCs/IOC Health” button under Subsystems (see Figure 2.4.) To reboot the IOC for a specific mainframe, click on the “Reboot” button corresponding to the desired mainframe.

The screenshot shows the EPICS IOC Health interface. At the top left, there is a vertical navigation menu titled "Subsystems" with options: Beamline, Cameras, DAQ, Gas, HV, and IOCs. Below this is a section titled "IOC Health" containing "IOC Heartbeats", "CA Gateway Stats (clonodb3)", "CA Gateway Stats (clonioc1)", and "Clonioc Stats". The main area is a table titled "IOC Health" with the following columns: IOC Name, Hostname, Up Time, Heartbeat, Expert, Soft Reboot, Last Reboot, Console, Hard Reboot, and Status. The table lists six entries for ioccaenhv_HVECAL1 through ioccaenhv_HVECAL6, all connected and in "ok" status. It also lists six entries for ioccaenhv_HVFTOF1 through ioccaenhv_HVFTOF6, all connected and in "ok" status.

IOC Name	Hostname	Up Time	Heartbeat	Expert	Soft Reboot	Last Reboot	Console	Hard Reboot	Status
ioccaenhv_HVECAL1	clonioc2.jlab.org	3 days, 23:19:06	343146			08/31/2017 16:00:59			ok
ioccaenhv_HVECAL2	clonioc2.jlab.org	3 days, 23:19:05	343145			08/31/2017 16:00:59			ok
ioccaenhv_HVECAL3	clonioc2.jlab.org	3 days, 23:19:06	343146			08/31/2017 16:00:58			ok
ioccaenhv_HVECAL4	clonioc2.jlab.org	3 days, 23:19:06	343146			08/31/2017 16:00:58			ok
ioccaenhv_HVECAL5	clonioc2.jlab.org	3 days, 23:19:06	343146			08/31/2017 16:00:59			ok
ioccaenhv_HVECAL6	clonioc2.jlab.org	4 days, 00:08:26	346106			08/31/2017 15:11:38			ok
ioccaenhv_HVFTOF1	clonioc2.jlab.org	3 days, 23:19:09	343149			08/31/2017 16:00:55			ok
ioccaenhv_HVFTOF2	clonioc2.jlab.org	3 days, 23:19:08	343148			08/31/2017 16:00:56			ok
ioccaenhv_HVFTOF3	clonioc2.jlab.org	3 days, 23:19:12	343152			08/31/2017 16:00:52			ok
ioccaenhv_HVFTOF4	clonioc2.jlab.org	3 days, 23:19:12	343152			08/31/2017 16:00:52			ok
ioccaenhv_HVFTOF5	clonioc2.jlab.org	3 days, 23:19:09	343149			08/31/2017 16:00:55			ok
ioccaenhv_HVFTOF6	clonioc2.jlab.org	3 days, 23:19:14	343154			08/31/2017 16:00:51			ok

Figure 2.4: EPICS IOC status and controls are available from the CSS Main Menu by clicking on “IOC” under “Subsystems”, then clicking on “IOC Health”. Choose the “High Voltage” tab for HV Mainframe IOCs. Reboots will be necessary whenever HV Mainframes are power-cycled or otherwise interrupted. Also if this screen shows a purple “Disconnected” in the Status column, or if the Heartbeat column is not incrementing a reboot will be necessary.

2.3 Detector Monitoring

A hierarchy of monitoring tools exist to study the performance of the Forward Carriage detector systems:

- ROOT based (FCMON)
- EPICS/JAVA based (CSSCLAS, COATJAVA)
- Full DAQ based (CODA, CSSCLAS, COATJAVA)

2.3.1 FCMON

One of the earliest tools developed is a ROOT-based GUI called FCMON [3] to monitor and display scalers for the Forward Carriage detectors. To launch FCMON from any Counting House computer, type *fcmon*. This brings up the window as shown in Figure 2.5 (left). This tool enables display of scaler data from all forward carriage front-end electronics (TDC discriminators and FADCs) for each of the six CLAS12 sectors. To use the interface for EC, click on the sector of interest in the left column, click on ECAL or PCAL in the center column, and then click on the source of the scalers in the third column. To bring up the scaler display screens, select “Scalers” under the “Monitor” drop down menu as shown in Figure 2.5 (right).

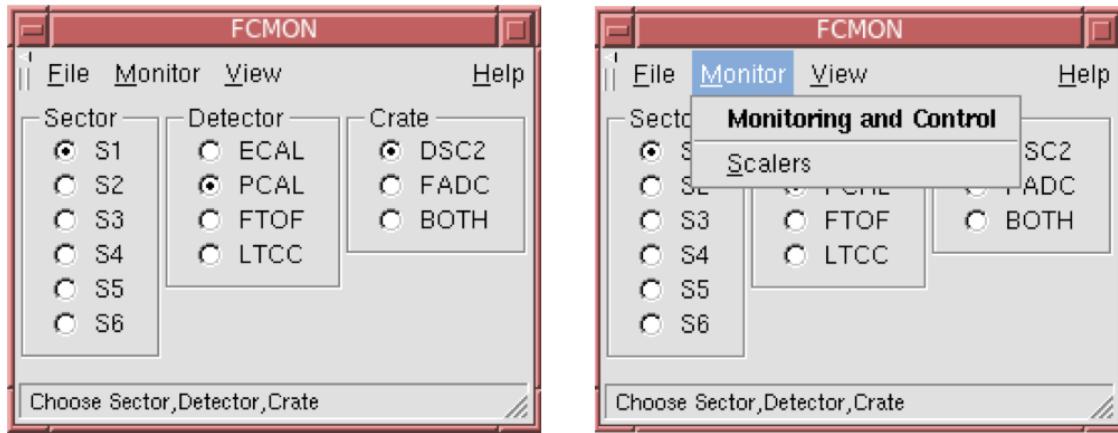


Figure 2.5: Forward Carriage scaler display program *fcmon*. (Left) Main screen. (Right) Menu selection to access scaler display window. Click on “scalers”.

The EC scalers can be monitored in one of three different ways by selecting the appropriate tab at the top of the scaler display screen (see Fig. 2.6). These three modes include:

- Slots: Scaler rate values (Hz) displayed for each VXS crate slot, channel housing the DSC2 or FADC modules.
- Rates: Scaler rate values (Hz) plotted for each physical EC detector channel.
- Stripcharts: Scaler rate values (Hz) plotted as a 2D strip chart (rate (z) vs. counter (y) vs. time (x))

Note that neither the DAQ nor EPICS is required to be running to use this tool, although the FADCs must have been initialized by a DAQ PRESTART for FADC scaler readout to work. Therefore, FCMON is the most direct tool for determining if the front-end electronics are receiving the intended signals from the PMTs. If holes develop in higher level occupancy plots derived from DAQ or online analysis, the first diagnostic step is to determine whether the hole is in the FADC or TDC channel or both and if the HV for the affected PMT is on and if the HV divider current is non-zero. Both FCMON and the HV Control GUIs previously discussed can provide this information. More consolidated screens are available with JAVA/EPICS tools discussed in the next section.

2.3.2 JAVA/EPICS Screens

Various CSS/JAVA based screens exist which collate information from EPICS and can be used to cross-check the direct scaler readout available from FCMON. Most of these screens are available from the *clascss* main menu and are described in Figures 2.7-2.10.

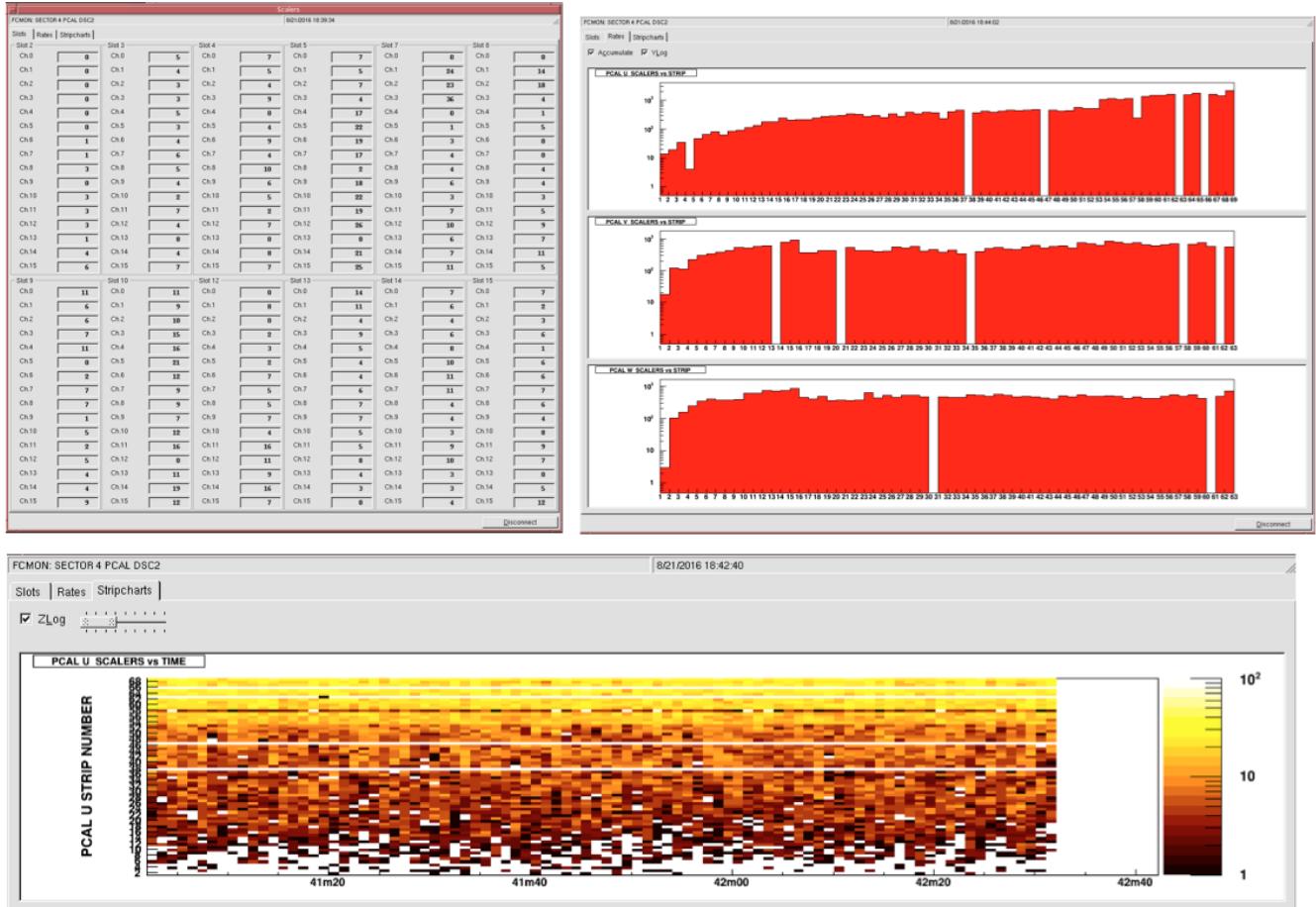


Figure 2.6: Display modes of FCMON Scalers GUI. Top Left: Slot,channel readout Top Right: Rates vs. PMT number and U,V,W view Bottom: 2D stripchart showing rates vs. time.

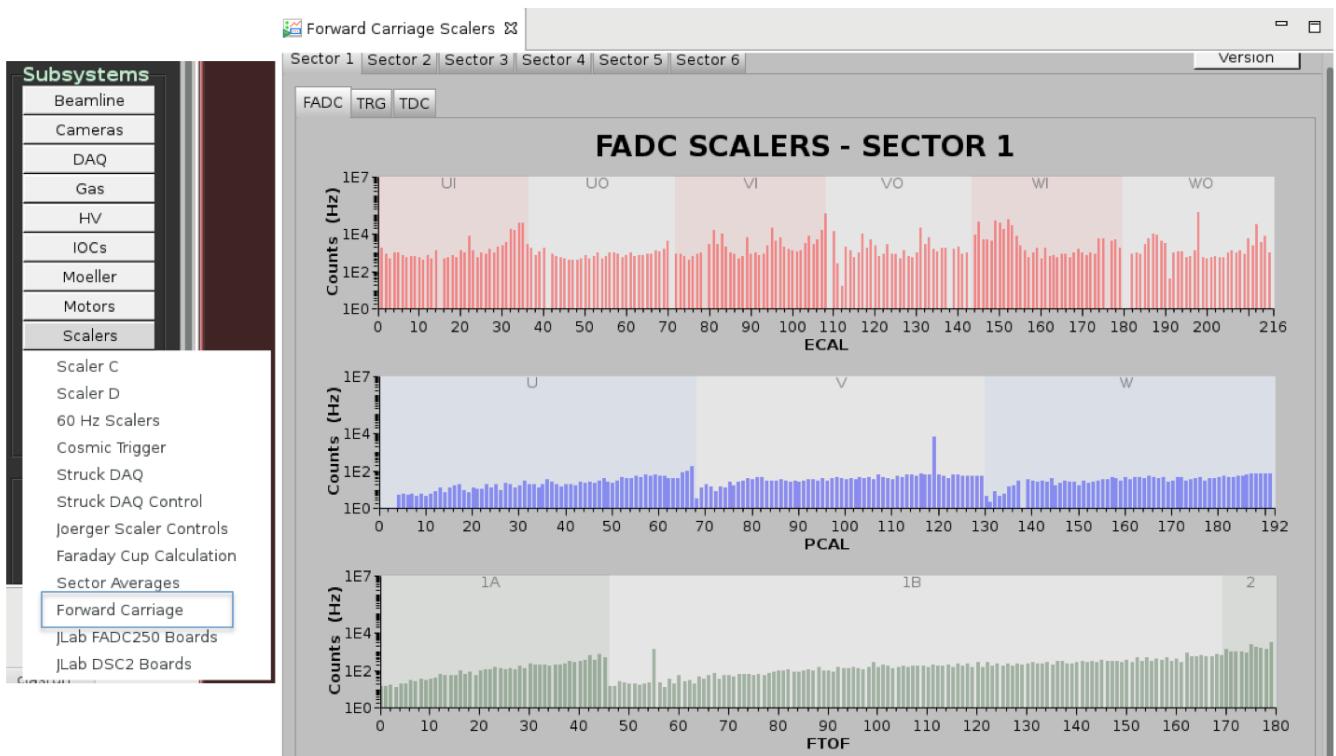


Figure 2.7: CSS/JAVA screen (right) obtained by clicking the “Forward Carriage” submenu item from the Subsystems/Scalers button of the main CSS menu (left). Scaler rates in Hz are shown for ECAL, PCAL and FTOF detectors, including all layers identified by shaded segments and labels. Buttons for sector number and scaler type are also provided.

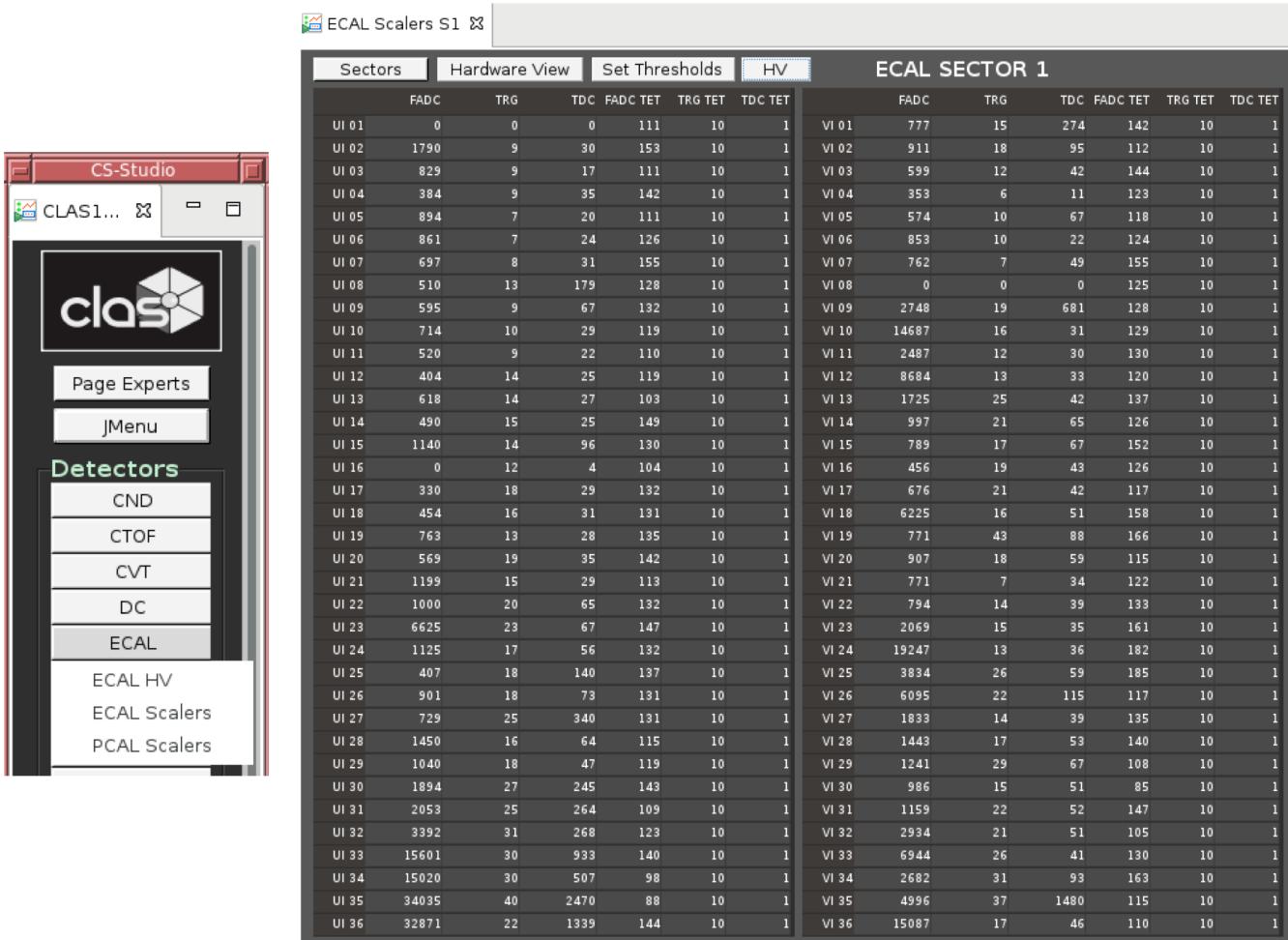


Figure 2.8: CSS/JAVA screen (right) obtained by clicking the “ECAL Scalers” submenu item from the ECAL button of the main CSS menu (left). Rows designate PMT locations. Columns show scaler rates (Hz) for flash ADCs (FADC) and TDC discriminators (TRG and TDC). Corresponding thresholds are in columns labeled FADC TET, TRG TET and TDC TET. Units are pedestal+threshold for FADC and millivolts for TRG and TDC.

ECAL Scalers S1 - FADC

Sectors	Scaler Type	Compact View	ECAL SECTOR 1 - FADC	
B_DET_ECAL_FADC_SEC1_UI_E01	B_HW_ADCECAL1_Sl03_Ch00	0	B_DET_ECAL_FADC_SEC1_VI_E01	B_HW_ADCECAL1_Sl05_Ch04 837
B_DET_ECAL_FADC_SEC1_UI_E02	B_HW_ADCECAL1_Sl03_Ch01	1766	B_DET_ECAL_FADC_SEC1_VI_E02	B_HW_ADCECAL1_Sl05_Ch05 931
B_DET_ECAL_FADC_SEC1_UI_E03	B_HW_ADCECAL1_Sl03_Ch02	743	B_DET_ECAL_FADC_SEC1_VI_E03	B_HW_ADCECAL1_Sl05_Ch06 601
B_DET_ECAL_FADC_SEC1_UI_E04	B_HW_ADCECAL1_Sl03_Ch03	311	B_DET_ECAL_FADC_SEC1_VI_E04	B_HW_ADCECAL1_Sl05_Ch07 440
B_DET_ECAL_FADC_SEC1_UI_E05	B_HW_ADCECAL1_Sl03_Ch04	928	B_DET_ECAL_FADC_SEC1_VI_E05	B_HW_ADCECAL1_Sl05_Ch08 543
B_DET_ECAL_FADC_SEC1_UI_E06	B_HW_ADCECAL1_Sl03_Ch05	838	B_DET_ECAL_FADC_SEC1_VI_E06	B_HW_ADCECAL1_Sl05_Ch09 889
B_DET_ECAL_FADC_SEC1_UI_E07	B_HW_ADCECAL1_Sl03_Ch06	717	B_DET_ECAL_FADC_SEC1_VI_E07	B_HW_ADCECAL1_Sl05_Ch10 822
B_DET_ECAL_FADC_SEC1_UI_E08	B_HW_ADCECAL1_Sl03_Ch07	504	B_DET_ECAL_FADC_SEC1_VI_E08	B_HW_ADCECAL1_Sl05_Ch11 0
B_DET_ECAL_FADC_SEC1_UI_E09	B_HW_ADCECAL1_Sl03_Ch08	609	B_DET_ECAL_FADC_SEC1_VI_E09	B_HW_ADCECAL1_Sl05_Ch12 2686
B_DET_ECAL_FADC_SEC1_UI_E10	B_HW_ADCECAL1_Sl03_Ch09	664	B_DET_ECAL_FADC_SEC1_VI_E10	B_HW_ADCECAL1_Sl05_Ch13 15339
B_DET_ECAL_FADC_SEC1_UI_E11	B_HW_ADCECAL1_Sl03_Ch10	568	B_DET_ECAL_FADC_SEC1_VI_E11	B_HW_ADCECAL1_Sl05_Ch14 2575
B_DET_ECAL_FADC_SEC1_UI_E12	B_HW_ADCECAL1_Sl03_Ch11	453	B_DET_ECAL_FADC_SEC1_VI_E12	B_HW_ADCECAL1_Sl05_Ch15 8799
B_DET_ECAL_FADC_SEC1_UI_E13	B_HW_ADCECAL1_Sl03_Ch12	648	B_DET_ECAL_FADC_SEC1_VI_E13	B_HW_ADCECAL1_Sl06_Ch00 1841
B_DET_ECAL_FADC_SEC1_UI_E14	B_HW_ADCECAL1_Sl03_Ch13	541	B_DET_ECAL_FADC_SEC1_VI_E14	B_HW_ADCECAL1_Sl06_Ch01 946
B_DET_ECAL_FADC_SEC1_UI_E15	B_HW_ADCECAL1_Sl03_Ch14	1139	B_DET_ECAL_FADC_SEC1_VI_E15	B_HW_ADCECAL1_Sl06_Ch02 787
B_DET_ECAL_FADC_SEC1_UI_E16	B_HW_ADCECAL1_Sl03_Ch15	0	B_DET_ECAL_FADC_SEC1_VI_E16	B_HW_ADCECAL1_Sl06_Ch03 453
B_DET_ECAL_FADC_SEC1_UI_E17	B_HW_ADCECAL1_Sl04_Ch00	302	B_DET_ECAL_FADC_SEC1_VI_E17	B_HW_ADCECAL1_Sl06_Ch04 651
B_DET_ECAL_FADC_SEC1_UI_E18	B_HW_ADCECAL1_Sl04_Ch01	485	B_DET_ECAL_FADC_SEC1_VI_E18	B_HW_ADCECAL1_Sl06_Ch05 6229
B_DET_ECAL_FADC_SEC1_UI_E19	B_HW_ADCECAL1_Sl04_Ch02	735	B_DET_ECAL_FADC_SEC1_VI_E19	B_HW_ADCECAL1_Sl06_Ch06 738
B_DET_ECAL_FADC_SEC1_UI_E20	B_HW_ADCECAL1_Sl04_Ch03	545	B_DET_ECAL_FADC_SEC1_VI_E20	B_HW_ADCECAL1_Sl06_Ch07 940
B_DET_ECAL_FADC_SEC1_UI_E21	B_HW_ADCECAL1_Sl04_Ch04	1261	B_DET_ECAL_FADC_SEC1_VI_E21	B_HW_ADCECAL1_Sl06_Ch08 735
B_DET_ECAL_FADC_SEC1_UI_E22	B_HW_ADCECAL1_Sl04_Ch05	975	B_DET_ECAL_FADC_SEC1_VI_E22	B_HW_ADCECAL1_Sl06_Ch09 775
B_DET_ECAL_FADC_SEC1_UI_E23	B_HW_ADCECAL1_Sl04_Ch06	6987	B_DET_ECAL_FADC_SEC1_VI_E23	B_HW_ADCECAL1_Sl06_Ch10 2109
B_DET_ECAL_FADC_SEC1_UI_E24	B_HW_ADCECAL1_Sl04_Ch07	1171	B_DET_ECAL_FADC_SEC1_VI_E24	B_HW_ADCECAL1_Sl06_Ch11 20059
B_DET_ECAL_FADC_SEC1_UI_E25	B_HW_ADCECAL1_Sl04_Ch08	566	B_DET_ECAL_FADC_SEC1_VI_E25	B_HW_ADCECAL1_Sl06_Ch12 4051
B_DET_ECAL_FADC_SEC1_UI_E26	B_HW_ADCECAL1_Sl04_Ch09	898	B_DET_ECAL_FADC_SEC1_VI_E26	B_HW_ADCECAL1_Sl06_Ch13 6196
B_DET_ECAL_FADC_SEC1_UI_E27	B_HW_ADCECAL1_Sl04_Ch10	849	B_DET_ECAL_FADC_SEC1_VI_E27	B_HW_ADCECAL1_Sl06_Ch14 1935
B_DET_ECAL_FADC_SEC1_UI_E28	B_HW_ADCECAL1_Sl04_Ch11	1279	B_DET_ECAL_FADC_SEC1_VI_E28	B_HW_ADCECAL1_Sl06_Ch15 1474
B_DET_ECAL_FADC_SEC1_UI_E29	B_HW_ADCECAL1_Sl04_Ch12	962	B_DET_ECAL_FADC_SEC1_VI_E29	B_HW_ADCECAL1_Sl07_Ch00 1268
B_DET_ECAL_FADC_SEC1_UI_E30	B_HW_ADCECAL1_Sl04_Ch13	1912	B_DET_ECAL_FADC_SEC1_VI_E30	B_HW_ADCECAL1_Sl07_Ch01 957
B_DET_ECAL_FADC_SEC1_UI_E31	B_HW_ADCECAL1_Sl04_Ch14	2147	B_DET_ECAL_FADC_SEC1_VI_E31	B_HW_ADCECAL1_Sl07_Ch02 1171
B_DET_ECAL_FADC_SEC1_UI_E32	B_HW_ADCECAL1_Sl04_Ch15	3389	B_DET_ECAL_FADC_SEC1_VI_E32	B_HW_ADCECAL1_Sl07_Ch03 2935
B_DET_ECAL_FADC_SEC1_UI_E33	B_HW_ADCECAL1_Sl05_Ch00	15929	B_DET_ECAL_FADC_SEC1_VI_E33	B_HW_ADCECAL1_Sl07_Ch04 6998
B_DET_ECAL_FADC_SEC1_UI_E34	B_HW_ADCECAL1_Sl05_Ch01	14981	B_DET_ECAL_FADC_SEC1_VI_E34	B_HW_ADCECAL1_Sl07_Ch05 2697
B_DET_ECAL_FADC_SEC1_UI_E35	B_HW_ADCECAL1_Sl05_Ch02	34148	B_DET_ECAL_FADC_SEC1_VI_E35	B_HW_ADCECAL1_Sl07_Ch06 4983
B_DET_ECAL_FADC_SEC1_UI_E36	B_HW_ADCECAL1_Sl05_Ch03	33088	B_DET_ECAL_FADC_SEC1_VI_E36	B_HW_ADCECAL1_Sl07_Ch07 15021

Figure 2.9: CSS/JAVA screen obtained by clicking the “Hardware View” button on the screen shown in Figure 2.8. Columns show the detector based (sector, layer, PMT) and hardware based (crate, slot, channel) designations of each scaler along with the rate in Hz. This screen can be used to identify the electronics location of occupancy holes involving bad LEMO cables between the patch panels and front-end electronics or possible dead electronic channels.

ECAL Scalers S3 WI

ECAL SECTOR 3 WI

	FADC	TRG	TDC	FADC TET	TRG TET	TDC TET	VMon	IMon
WI01	0	0	0	80	10	1	1414	0
WI02	10125	1	2	121	10	1	1764	404
WI03	2837	13	274	105	10	1	1692	390
WI04	2157	27	382	113	10	1	1862	459
WI05	10033	59	3843	87	10	1	1940	461
WI06	46139	46	8826	129	10	1	1852	438
WI07	102796	23	745	119	10	1	1794	428
WI08	219841	47	1725	97	10	1	1768	408
WI09	35164	52	6471	150	10	1	2036	486
WI10	51997	33	4066	114	10	1	1840	437
WI11	10204	10	37	140	10	1	1788	424
WI12	4056	18	43	121	10	1	1770	407
WI13	3822	23	791	139	10	1	1926	463
WI14	0	0	0	127	10	1	1793	419
WI15	13275	46	1085	143	10	1	1893	440
WI16	15863	18	48	164	10	1	1736	394
WI17	14466	49	106	137	10	1	2144	404
WI18	3676	26	53	148	10	1	1922	448
WI19	981	16	49	125	10	1	1856	433
WI20	469	3	20	124	10	1	1962	458
WI21	1609	23	72	146	10	1	1832	422
WI22	2608	21	47	135	10	1	1820	424
WI23	1218	15	38	83	10	1	1804	430
WI24	2015	13	40	122	10	1	1834	425
WI25	1454	19	63	133	10	1	1746	405
WI26	935	26	57	141	10	1	1788	414
WI27	2173	33	144	105	10	1	1759	414
WI28	1353	18	39	147	10	1	1745	403
WI29	3793	26	68	135	10	1	1829	430
WI30	4274	19	77	115	10	1	1824	422
WI31	1240	1	15	130	10	1	1888	441
WI32	2750	43	883	126	10	1	1574	352
WI33	2977	30	289	104	10	1	1832	424
WI34	1352	29	85	126	10	1	1770	412
WI35	710	31	127	124	10	1	1884	436
WI36	0	0	0	147	10	1	1	0

VMon OK, IMon=0: Bad HV divider, SHV connector or HV distribution box

VMon OK, IMon OK, FADC OK, TDC ~ 0: Bad TDC patch cable

VMon OK, IMon OK, FADC=0, TDC=0: Bad LEMO or BNC connection between PMT and patch panel

Vmon=0, IMon=0: HV tripped or disabled

Figure 2.10: CSS/JAVA screen obtained by clicking the “HV” button on the screen shown in Figure 2.8. Columns labeled VMon and IMon show the monitored PMT HV and HV divider string current, respectively. Units are volts and microamps, respectively. This screen enables the user to diagnose occupancy holes seen in the scaler data, as shown by the examples denoted by the blue arrows.

2.3.3 COATJAVA Utilities

3 Information for Subsystem Experts

3.1 Subsystem Expert Responsibilities

The EC subsystem experts have several key responsibilities:

1. Complete hot checkout sign-off before the start of each run period (see Section 3.1.1).
2. Respond to calls on the on-call phone to resolve issues with the EC system that are necessary during data taking (see Section 3.1.2).
3. Take periodic HV gain calibration runs and adjust the system HV settings (see Section 3.1.3).
4. Make repairs to the hardware during maintenance periods (see Section 3.4).

3.1.1 Hot Checkout

Prior to the start of each physics running period, each subsystem group leader is responsible to review the components of their systems to be sure that they are fully operational. This review is referred to as “hot checkout”. The hot checkout is an online checklist for each system that includes a sign-off for all hardware elements of the system (e.g. HV, LV, detectors, gas, pulser). For the EC system, the hot checkout includes verification that all detectors are operational and that all signals are present as seen through the scaler displays. Fig. 3.1 shows screenshots of the hot checkout interface from a development version of the system. Under the heading “Hall B CLAS12 Detector”, open the list for the EC system. All entries for EC must be verified as ready. Note that often as part of the system checkout before the start of a run period, an initial HV gain calibration is completed (see Section 3.1.3). Reminders to complete the system hot checkout will be sent out shortly before the start of a given run period with the required deadline for completing the work.

3.1.2 On-call Responsibilities

Each subsystem will organize a list of on-call experts who will take responsibility for carrying a cell phone to allow 24 hour access to experts who can address any problems that arise during the physics running period. The phone numbers of all subsystem experts are posted on the run page. Any problems that cannot be quickly solved by the shift workers, where quickly amounts to 10 to 15 minutes, should result in a call to the relevant expert cell phone.

The on-call experts can often diagnose problems over the telephone, but there are times where they will have to go to the Counting House to more fully address the issues. One of the important responsibilities of the on-call experts is to make practical decisions regarding which problems require access to Hall B for immediate attention and when they can be delayed to periods when the accelerator is down or other work is scheduled in the hall. For the EC system, usually problems with a single channel are not important enough to stop the data acquisition. The normal mode of operation after initial investigation of a bad channel, is to turn off the HV for that channel until access can be made for a more detailed investigation. This work should be coordinated with the Run Coordinator.

Note: It is the responsibility of the EC on-call expert to review all issues that they cannot resolve with the EC subsystem Group Leader as soon as is reasonable.

3.1.3 HV Gain Calibrations

The HV gain calibrations for the EC system are typically completed before the start of each run period, as well as several times during the run period when there is opportunity. The HV gain calibration procedure employs a cosmic ray trigger defined either ECAL or PCAL. The ADC spectra for each counter are fit to ensure that the minimum ionizing particle peak appears at a specific location in the ADC range corresponding to a specific gain. The end result of the gain calibration amounts to adjusting the system HV settings to position the ADC peaks at their assigned locations.

The calibration suite for the EC system includes both an online and an offline component. The online component is used to calibrate the PMT gains and the output is a table of PMT HV settings that are downloaded into the HV power supplies. The offline component is used to determine the parameters to optimize the absolute energy calibration and resolution of the system. Full documentation on using EC calibration, including tutorials for using the code, are included on the EC web page. [4].

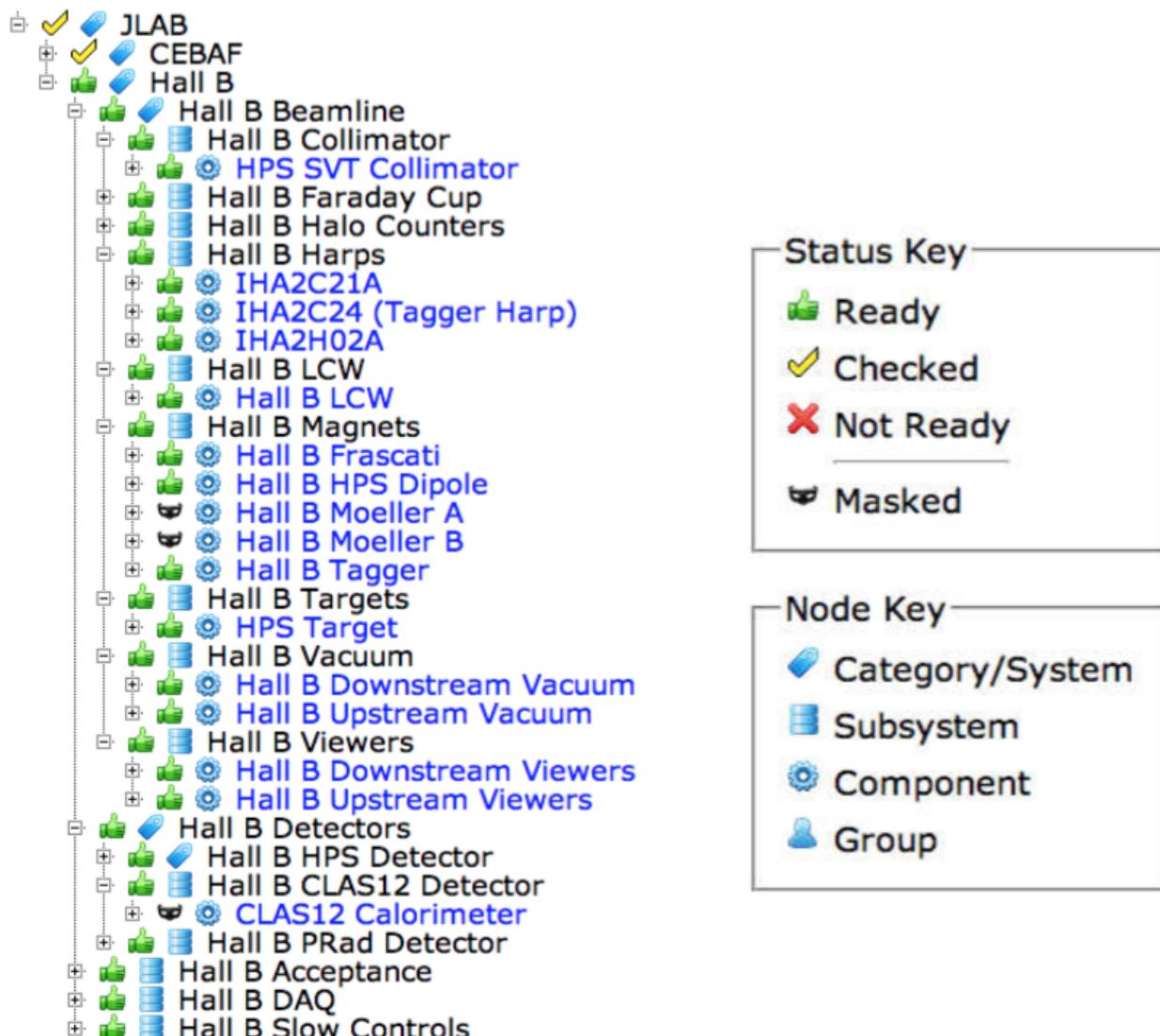


Figure 3.1: Screenshots of the development version of the Hall B hot checkout screens. The EC system will appear under the “Hall B CLAS12 Detector” heading. All entries for EC have been to verified as functional and all items listed as “Not Ready” must be changed over to “Ready”.

3.2 HV System Operations

3.2.1 Setting HV Channel Parameters

The CS-Studio program is used to monitor the HV settings of the EC system and to toggle the HV off and on for individual or multiple channels in the system. As discussed in Section 2.2, there is also the option to adjust settings channel-by-channel using the HV “expert” screen shown in Fig. 2.3. Here the parameters, V_{set} , I_{set} , V_{max} , and the HV ramp up and ramp down rates, can be entered directly into the parameter fields. This “expert” screen should most properly be used only for viewing the channel parameter set values. Finally there are control scripts available in the event nominal settings need to be restored. From the computers in the Hall B Counting House, the scripts are located in the sector subdirectories located in the path: `/home/clasrun/ecal/hv/sn`, and `/home/clasrun/pcal/hv/sn` where sn corresponds to $s1$ to $s6$ for $S1 \rightarrow S6$. There are five scripts available for setting these HV channel parameters:

- `loadhvmax-sn`: Maximum HV limits for each supply channel (units = V)
- `loadi0-sn`: Maximum current limits for each supply channel (units = μ A)
- `loadrup-sn`: Voltage ramp up rates for each supply channel (units = V/s)
- `loadrdn-sn`: Voltage ramp down rates for each supply channel (units = V/s)
- `loadtrip-sn`: Maximum time duration for an overcurrent condition before the channel trips (units = s)

The nominal settings for the HV channel parameters are as follows:

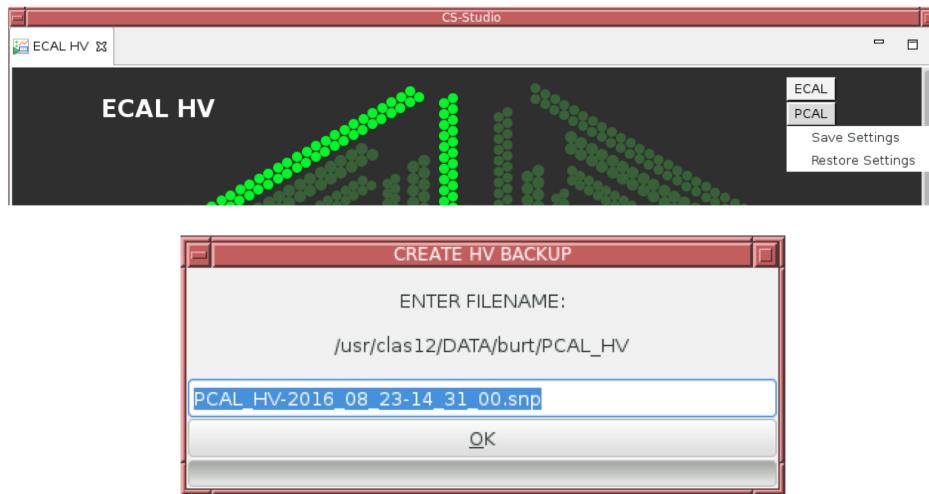
- HV values (PCAL): Typically in the range from -800 V to -950 V
- HV values (ECAL): Typically in the range from -1500 V to -2000 V
- HV values (PCAL): Typically in the range from -800 V to -950 V
- HV_{max} values: PCAL: -1100 V, ECAL: -2500 V
- i_{max} values: 500 μ A
- HV ramp up rate: 50 V/s
- HV ramp down rate: 100 V/s
- Overcurrent duration before trip: 1 s

Individual HV values and the enable/disable status of each PMT are created by the monitoring and calibration programs and these values are stored in a separate database. There are no backup scripts for setting these values since they are time-dependent and have to be carefully managed. Nevertheless save and restore values can be archived from the EC HV control screen (see Section 3.2.2).

3.2.2 HV Save and Restore

The EC HV interface allows all system channel settings to be saved into a file or loaded from an archived file by clicking on the “ECAL” or “PCAL” button in the upper right corner of the main HV screen (see Fig. 2.1). The files created are referred to as “BURT” backup files, where BURT is an acronym for “Backup and Restore Tool”. BURT is a utility for saving the HV system settings into an ascii file readable by the EPICS Slow Control system.

After clicking on the detector button, a sub-menu appears as shown in Fig. 3.2 to select “Save Settings” or “Restore Settings”. Clicking on “Save Settings” brings up a window “CREATE HV BACKUP” as shown at bottom, displaying the save file path and the selected file name that contains the system name along with the date and time. If the “Restore Settings” option is chosen, the window shown in Fig. 3.3 comes up showing the saved ECAL or PCAL HV restore files available to select from. Selecting a file and clicking on “OK” at the bottom of the window loads all channel parameters for the full HV system. Note that a new backup file should be created whenever any HV settings have changed, including HV values, channel parameter settings, and channel on/off settings.



<det>_HV-<year>_<month>_<date> - <hour>_<min>_<sec>.snp

Figure 3.2: Top: Choose the appropriate detector (ECAL or PCAL) for saving HV settings. The pop-up menu will allow you to select “Save Settings” or “Restore Settings”. Bottom: If “Save Settings” is chosen, a pop-up confirmation dialog will display the path and name of the BURT snapshot file, using the timestamp format shown at bottom. This name can be edited if desired.

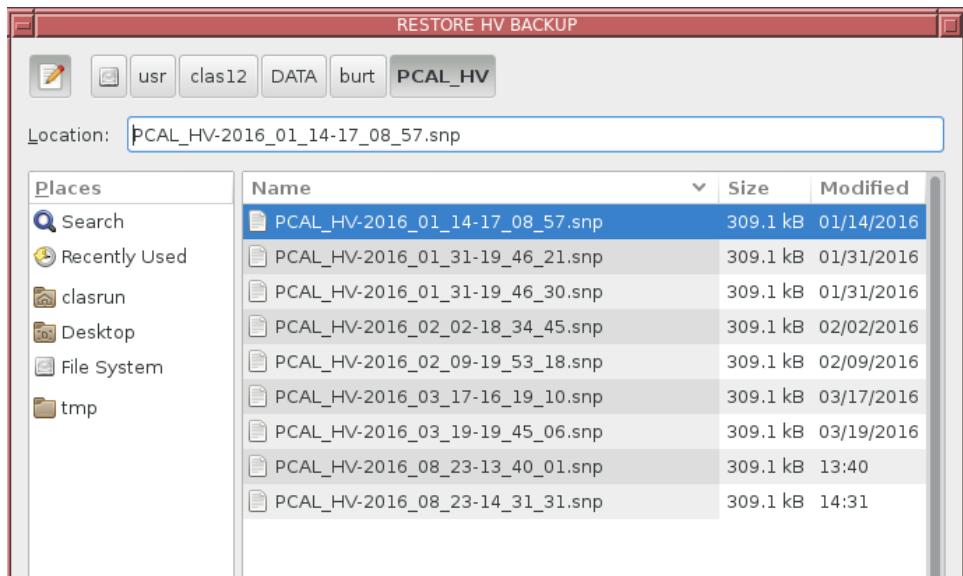


Figure 3.3: If “Restore Settings” is chosen, use the pop-up file chooser to select the snapshot file for restoring HV settings.

3.3 Cabling Details

3.3.1 Signal Cable Layout

The U,V,W PMTs for the ECAL modules are located at the rear (downstream) face of each triangle-shaped module (see Figure 3.4) and are distributed uniformly along its perimeter. There are two layers of PMTs: the top layer reads out the inner calorimeter (closest to the target) and the bottom layer reads out the outer calorimeter. The PMTs are also oriented parallel to the U,V,W strips within each module. HV and RG-8 signal cables are fastened to and routed along steel gratings running parallel to the calorimeter sides. RG-58 patch cables (16 ns delay) run from the PMT anode connector to the thicker and less flexible RG-8 cable. At the other end of the RG-8, a second connection is made to RG-58 patch cables (16 ns delay) connected to LEMO inputs at the rear of the UVA 122B splitter panels. These patch connections are illustrated by the photos in Figures 3.5 and 3.10.



Figure 3.4: Placement of ECAL U,V,W PMTs at rear (downstream) side of Sector 2 module. Gratings are used to route HV and RG-8 signal cables.

The U,V,W PMTs for the PCAL modules are mounted along the sides of each module (see Figures 3.6 and 3.7). Due to geometry constraints the V,W PMTs for PCAL are located together on the same side (corresponding to V PMT side of the ECAL.) For PCAL only the U PMTs and cable connections are accessible from the Forward Carriage decks. Figure 3.8 shows a view of the PCAL U cable routing within the gap between adjacent ECAL modules, and Figure 3.9 shows the V,W cable routing for Sector 6. No patch cables are used for PCAL. The RG-58 signal cables have a BNC connector on the PMT end and a LEMO connector on the splitter panel end.

3.3.2 HV Cable Layout

HV cables generally run parallel or along the same general path as the signal cables for both PCAL and ECAL. HV cable connections to the rear of the CAEN mainframes are made using a JLAB built transition/distribution box which has 48 SHV input connectors and two output cables each terminated with a 24-pin Radiall connector designed to mate with the input connector on the A1535N cards (see Figure 3.10).

Both HV and signal cables from the EC system pass under the floor gratings on Levels 2 and 3. For Level 1 cables are routed through openings in the ceiling. Connections to the BNC-Lemo transition cables used for the ECAL RG-8 cables are made under the grating near the racks containing the ECAL splitter panels. A photo showing the floor grating removed is in Figure 3.10 (right).

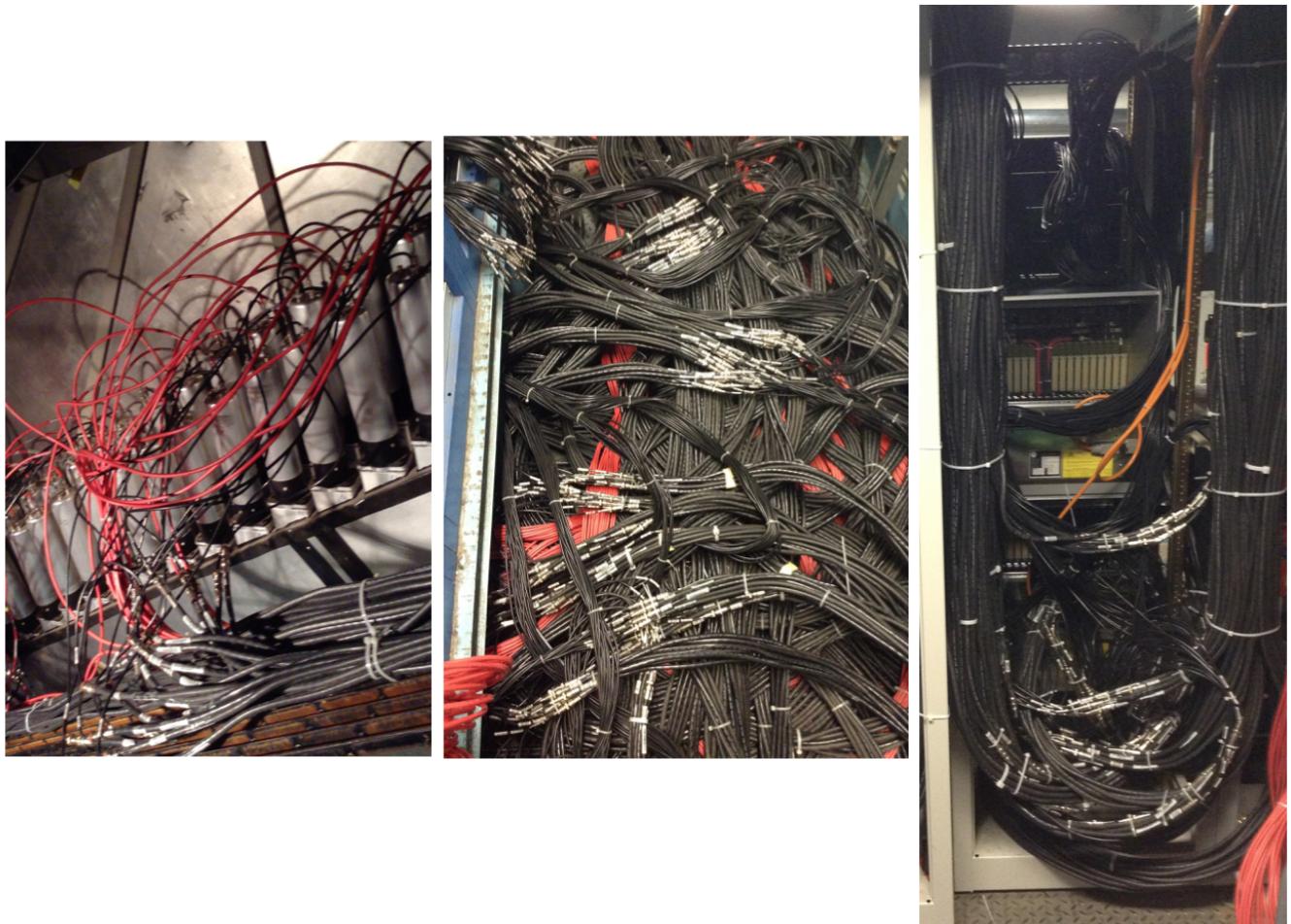


Figure 3.5: For ECAL two RG-58 16 ns patch cable connections are made to the RG-8 signal cable: at the PMT end and near the UVA 122B splitter panels at the electronic racks. Left: Connections made along the rail grating next to the PMTs. Middle: Connection made beneath the floor gratings on Levels 2 and 3 of the Forward Carriage. Right: Connections made within the electronics racks on Level 1.



Figure 3.6: Placement of PCAL U PMTs (left) and V,W PMTs (right). Photo taken in EEL Building.

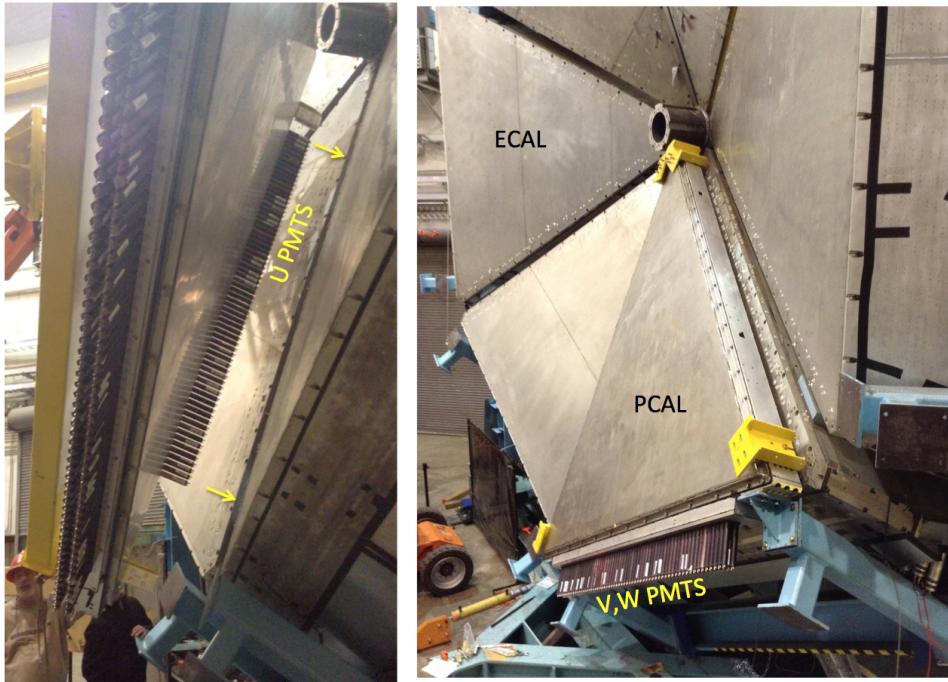


Figure 3.7: Orientation of PCAL U and V,W PMTs relative to ECAL. Photo taken in Hall B during installation of PCAL in Sector 5 of the Forward Carriage.

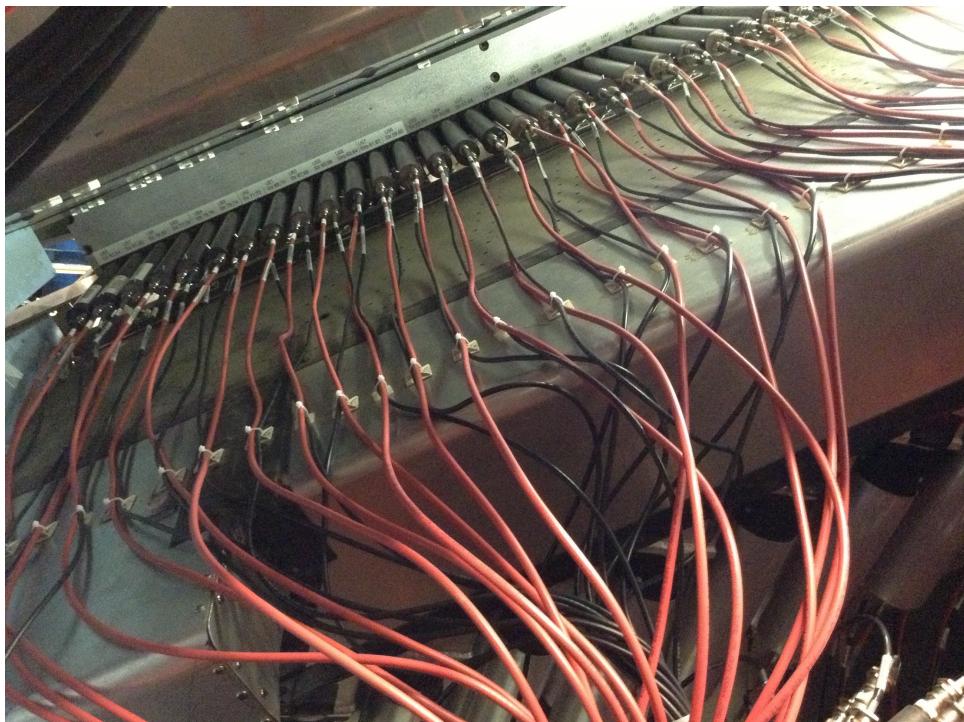


Figure 3.8: Routing of HV and RG-58 signal cables from U PMTs of PCAL. Cables pass through the gap in between adjacent ECAL modules (seen above and below in the photo.)

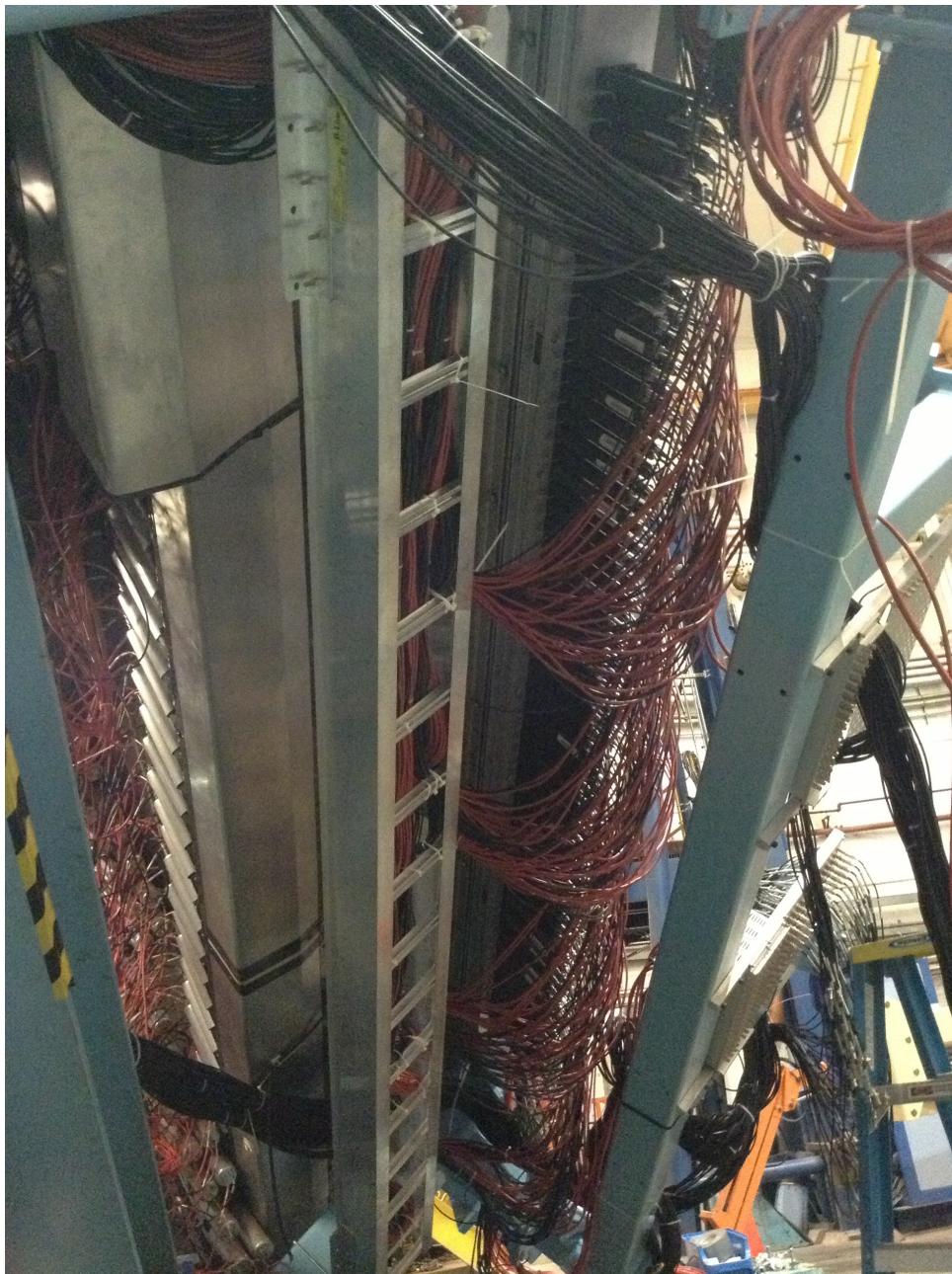


Figure 3.9: Routing of HV and RG-58 signal cables from V,W PMTs of PCAL. Cables are routed directly to cable trays mounted parallel to the V,W readout side for all modules. Only Sector 5 and Sector 6 (seen here) V,W PMTs are accessible from floor level with ladders. Other sectors require a man-lift for access. Also visible at left are the V PMTs for ECAL.

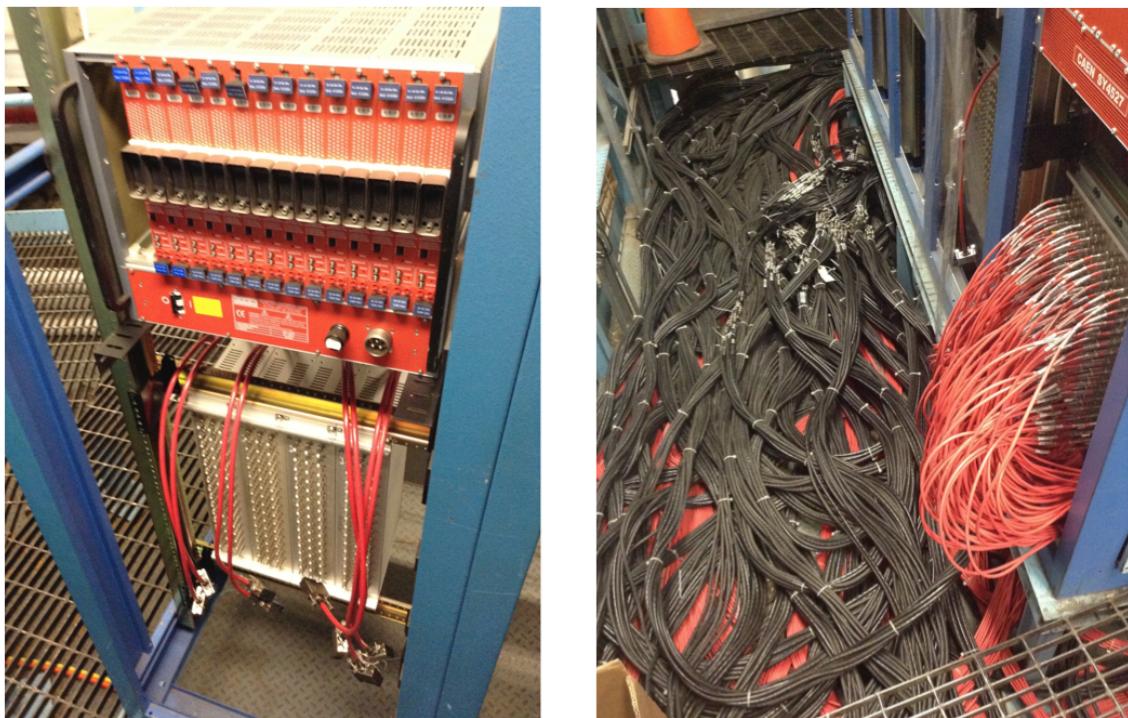


Figure 3.10: Left: Rear of CAEN HV mainframe (top) showing installed HV cards. At bottom are transition boxes with SHV input connectors and red output cables which mate with the HV cards. Right: Photographs of ECAL HV/signal cable bundles underneath floor gratings (which are removed here). Removal of floor gratings gives access to RG-8/RG-58 BNC/BNC connections visible at top. Also visible are HV cable connections to the HV distribution box (right).

3.3.3 Signal Splitters and Cable Maps

Both ECAL and PCAL rely on passive resistive splitters to distribute signals to the TDC and ADC VME/VXS crates. The split ratio is 2:1 for PCAL (using the UVA122D model) and 3:1 for ECAL (using the UVA122B model). For both calorimeters the larger signal goes to the FADC modules. Each splitter panel contains 64 channels using four sub-modules with 16 channels each. Thus PCAL, which has 192 PMTs per module, requires only 3 splitter panels and utilizes every channel. However ECAL, which has 216 PMTs per module (108 for EC inner and 108 for EC outer), requires four splitter panels, but does not utilize every channel. For both ECAL and PCAL, the input mapping to the splitters is sequential (in ascending U,V,W PMT order). For PCAL, there are no gaps, while for ECAL a gap is used to conveniently map the left and right halves of the splitters to EC inner and EC outer. This is shown in Figure 3.11. Note also that signal cables are mapped to the splitters in a vertical sequence rather than horizontal, in order to minimize patch cables crossing over each other in their path to the VME/VXS crate slots.

Mapping of patch cables from the splitter to electronics follows exactly the sequence used for the splitters, including the ECAL gaps. These maps are illustrated for the PCAL FADC VXS crate and DSC/TDC VME crate in Figures 3.12 and Figures 3.13. The corresponding ECAL maps are in Figures 3.14 and Figures 3.15. Note these maps are also loaded into the CCDB (Calibration Commissioning Data Base) as translation tables under the directory `/daq/tt/ec`.

HV cable maps are also sequential for both PCAL and ECAL and there are no gaps and no spare channels. The HV cable maps for PCAL and ECAL are shown in Figures 3.16 and 3.17.

3.3.4 Altering Cable Maps

The nominal procedure if there is a problem with a VME electronics board is to replace the board with a spare unit. However, for testing purposes, it might be necessary to change a signal input at the FADC, discriminator, or TDC to an unused channel. For PCAL there are no unused channels, while for ECAL there are a total of eight unused channels for both FADCs and DSCs. Utilizing unused channels for the TDCs is limited due to the use of ribbon cable. Any remapping of channels must be done in coordination with the DAQ system expert in order to update the database translation tables. This operation is not something that is normally done and should not be attempted by shift workers or EC experts as it could lead to problems decoding the data.

Problems with channels within the HV system may arise due to connection failures at the 24 pin interface between the HV distribution box and the A1535N board, or failures of the board itself. The standard procedure when there is a problem with a CAEN HV board is to swap out the board (see Section 3.4.1). As indicated there are no spare channels in either ECAL or PCAL. An unlikely possibility is failure of a single slot in the HV mainframe, which would require moving a HV board to an unused slot. This would require reprogramming the EPICS Slow Controls database to ensure smooth operation of the HV Control GUIs and should be done only in consultation with a Slow Controls expert.

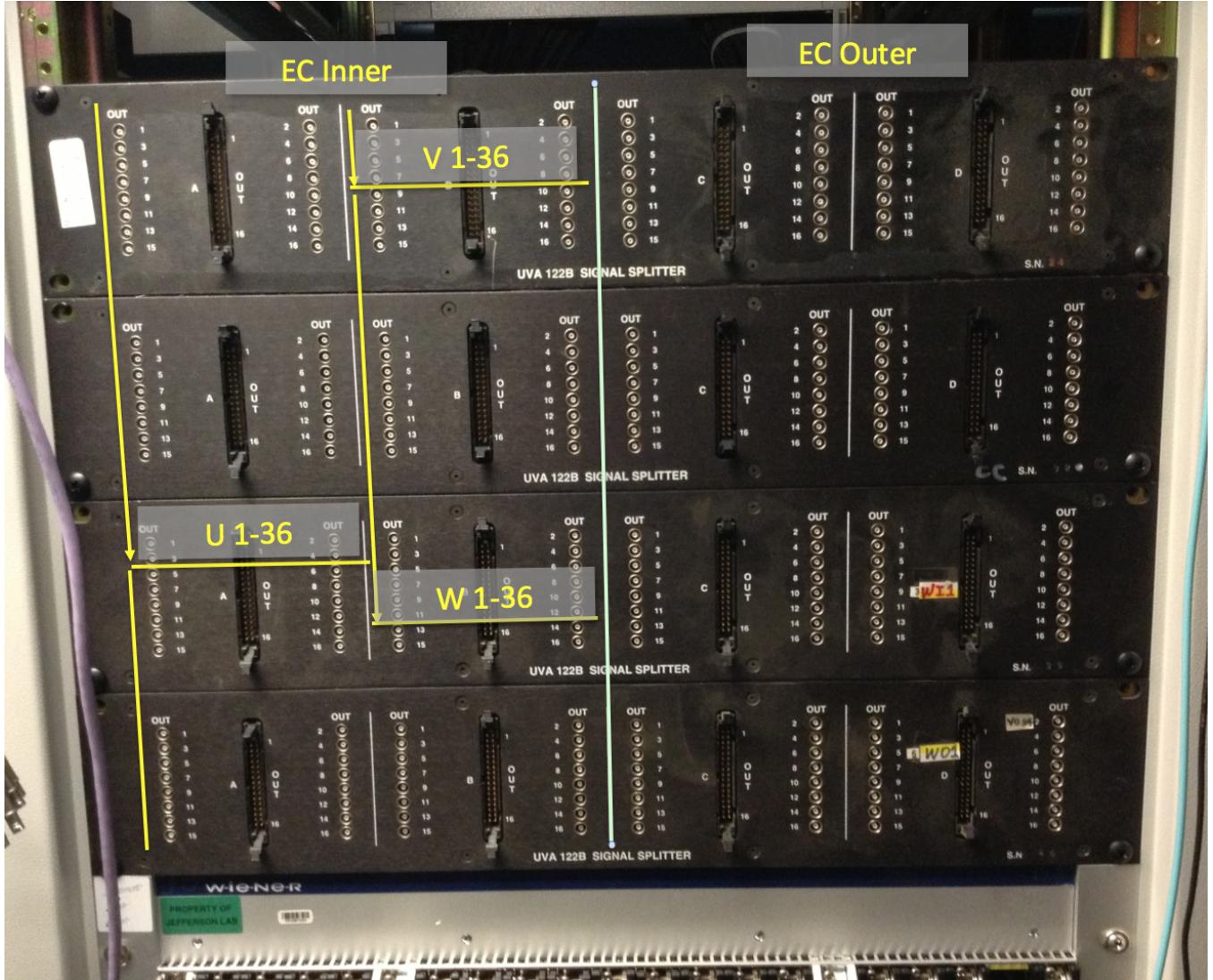


Figure 3.11: Photo of ECAL UVA122B splitter panels. LEMO inputs are in the rear. LEMO outputs are used for FADC connections and the mapping used for EC Inner is illustrated with the yellow overlay. The 17-pin connector is used for mini-coax connections to the DSC2 discriminators. The split ratio is 3:1, with 3/4 going to the FADC and 1/4 going to the DSC2. The EC Outer mapping is identical.

PCAL FADC MAP															
#	slot 2	slot 3	slot 4	slot 5	slot 6	slot 7	slot 8	slot 9	slot 10	slot 11	slot 12	slot 13	slot 14	slot 15	slot 16
15	U16	U32	U48	U64	V12	V28	V44	V60				W14	W30	W46	W62
14	U15	U31	U47	U63	V11	V27	V43	V59				W13	W29	W45	W61
13	U14	U30	U46	U62	V10	V26	V42	V58				W12	W28	W44	W60
12	U13	U29	U45	U61	V9	V25	V41	V57				W11	W27	W43	W59
11	U12	U28	U44	U60	V8	V24	V40	V56				W10	W26	W42	W58
10	U11	U27	U43	U59	V7	V23	V39	V55				W9	W25	W41	W57
9	U10	U26	U42	U58	V6	V22	V38	V54				W8	W24	W40	W56
8	U9	U25	U41	U57	V5	V21	V37	V53				W7	W23	W39	W55
7	U8	U24	U40	U56	V4	V20	V36	V52				W6	W22	W38	W54
6	U7	U23	U39	U55	V3	V19	V35	V51				W5	W21	W37	W53
5	U6	U22	U38	U54	V2	V18	V34	V50				W4	W20	W36	W52
4	U5	U21	U37	U53	V1	V17	V33	V49				W3	W19	W35	W51
3	U4	U20	U36	U52	U68	V16	V32	V48				W2	W18	W34	W50
2	U3	U19	U35	U51	U67	V15	V31	V47				W1	W17	W33	W49
1	U2	U18	U34	U50	U66	V14	V30	V46				W62	W16	W32	W48
0	U1	U17	U33	U49	U65	V13	V29	V45				W61	W15	W31	W47

*pcal-fadc-map.xlsx
Modified: December 12, 2013*

Figure 3.12: Electronics map for the input connections to the PCAL VME FADCs. Slots 11 and 12 are reserved for the Virtual Trigger Processor (VTP).

PCAL DISCRIMINATOR MAP															
#	slot 2	slot 3	slot 4	slot 5	slot 6	slot 7	slot 8	slot 9	slot 10	slot 11	slot 12	slot 13	slot 14	slot 15	slot 16
1	U1	U17	U33	U49	U65	V13	V29	V45	V61	W15	W31	W47			
2	U2	U18	U34	U50	U66	V14	V30	V46	V62	W16	W32	W48			
3	U3	U19	U35	U51	U67	V15	V31	V47	W1	W17	W33	W49			
4	U4	U20	U36	U52	U68	V16	V32	V48	W2	W18	W34	W50			
5	U5	U21	U37	U53	V1	V17	V33	V49	W3	W19	W35	W51			
6	U6	U22	U38	U54	V2	V18	V34	V50	W4	W20	W36	W52			
7	U7	U23	U39	U55	V3	V19	V35	V51	W5	W21	W37	W53			
8	U8	U24	U40	U56	V4	V20	V36	V52	W6	W22	W38	W54			
9	U9	U25	U41	U57	V5	V21	V37	V53	W7	W23	W39	W55			
10	U10	U26	U42	U58	V6	V22	V38	V54	W8	W24	W40	W56			
11	U11	U27	U43	U59	V7	V23	V39	V55	W9	W25	W41	W57			
12	U12	U28	U44	U60	V8	V24	V40	V56	W10	W26	W42	W58			
13	U13	U29	U45	U61	V9	V25	V41	V57	W11	W27	W43	W59			
14	U14	U30	U46	U62	V10	V26	V42	V58	W12	W28	W44	W60			
15	U15	U31	U47	U63	V11	V27	V43	V59	W13	W29	W45	W61			
16	U16	U32	U48	U64	V12	V28	V44	V60	W14	W30	W46	W62			
	DISC	DISC	DISC	DISC	TDC	DISC	DISC	DISC	DISC	DISC	DISC	DISC	DISC	DISC	TDC

*pcal-disc-map.xls
Modified 8/24/16*

Figure 3.13: Electronics map for the input connections to the PCAL VME discriminators. Twisted-pair ribbon cables make the connections to the V1190 TDCs is slots 6 and 16.

ECAL FADC MAP																	
#	slot 2	slot 3	slot 4	slot 5	slot 6	slot 7	slot 8	slot 9	slot 10	slot 11	slot 12	slot 13	slot 14	slot 15	slot 16	slot 17	slot 18
15	U16 INNER	U32 INNER	V12 INNER	V28 INNER	W8 INNER	W24 INNER	U16 OUTER			U32 OUTER	V12 OUTER	V28 OUTER	W8 OUTER	W24 OUTER			
14	U15 INNER	U31 INNER	V11 INNER	V27 INNER	W7 INNER	W23 INNER	U15 OUTER			U31 OUTER	V11 OUTER	V27 OUTER	W7 OUTER	W23 OUTER			
13	U14 INNER	U30 INNER	V10 INNER	V26 INNER	W6 INNER	W22 INNER	U14 OUTER			U30 OUTER	V10 OUTER	V26 OUTER	W6 OUTER	W22 OUTER			
12	U13 INNER	U29 INNER	V9 INNER	V25 INNER	W5 INNER	W21 INNER	U13 OUTER			U29 OUTER	V9 OUTER	V25 OUTER	W5 OUTER	W21 OUTER			
11	U12 INNER	U28 INNER	V8 INNER	V24 INNER	W4 INNER	W20 INNER	W36 INNER	U12 OUTER		U28 OUTER	V8 OUTER	V24 OUTER	W4 OUTER	W20 OUTER	W36 OUTER		
10	U11 INNER	U27 INNER	V7 INNER	V23 INNER	W3 INNER	W19 INNER	W35 INNER	U11 OUTER		U27 OUTER	V7 OUTER	V23 OUTER	W3 OUTER	W19 OUTER	W35 OUTER		
9	U10 INNER	U26 INNER	V6 INNER	V22 INNER	W2 INNER	W18 INNER	W34 INNER	U10 OUTER		U26 OUTER	V6 OUTER	V22 OUTER	W2 OUTER	W18 OUTER	W34 OUTER		
8	U9 INNER	U25 INNER	V5 INNER	V21 INNER	W1 INNER	W17 INNER	W33 INNER	U9 OUTER		U25 OUTER	V5 OUTER	V21 OUTER	W1 OUTER	W17 OUTER	W33 OUTER		
7	U8 INNER	U24 INNER	V4 INNER	V20 INNER	W4 INNER	W16 INNER	W36 INNER	U8 OUTER		U24 OUTER	V4 OUTER	V20 OUTER	V36 OUTER	W16 OUTER	W32 OUTER		
6	U7 INNER	U23 INNER	V3 INNER	V19 INNER	V19 INNER	W15 INNER	W31 INNER	U7 OUTER		U23 OUTER	V3 OUTER	V19 OUTER	V3 OUTER	V15 OUTER	W31 OUTER		
5	U6 INNER	U22 INNER	V2 INNER	V18 INNER	V18 INNER	W14 INNER	W30 INNER	U6 OUTER		U22 OUTER	V2 OUTER	V18 OUTER	V4 OUTER	V14 OUTER	W30 OUTER		
4	U5 INNER	U21 INNER	V1 INNER	V17 INNER	V17 INNER	W13 INNER	W29 INNER	U5 OUTER		U21 OUTER	V1 OUTER	V17 OUTER	V3 OUTER	V13 OUTER	W29 OUTER		
3	U4 INNER	U20 INNER	U6 INNER	U6 INNER	U6 INNER	W16 INNER	W28 INNER	U4 OUTER		U20 OUTER	V16 OUTER	V36 OUTER	V16 OUTER	V12 OUTER	W28 OUTER		
2	U3 INNER	U19 INNER	U5 INNER	V15 INNER	V15 INNER	V31 INNER	W27 INNER	U3 OUTER		U19 OUTER	U35 OUTER	V15 OUTER	V31 OUTER	V15 OUTER	V27 OUTER		
1	U2 INNER	U18 INNER	U4 INNER	V14 INNER	V14 INNER	V30 INNER	W26 INNER	U2 OUTER		U18 OUTER	U34 OUTER	V14 OUTER	V30 OUTER	V10 OUTER	W26 OUTER		
0	U1 INNER	U17 INNER	U3 INNER	V13 INNER	V13 INNER	W9 INNER	W29 INNER	U1 OUTER		U17 OUTER	U33 OUTER	V13 OUTER	V29 OUTER	W9 OUTER	W25 OUTER		

ecal-fadc-map.xlsx

Modified: August 24, 2016

Figure 3.14: Electronics map for the input connections to the ECAL VME FADCs. Slots 11 and 12 are reserved for the Virtual Trigger Processor (VTP).

ECAL DISCRIMINATOR MAP																	
#	slot 2	slot 3	slot 4	slot 5	slot 6	slot 7	slot 8	slot 9	slot 10	slot 11	slot 12	slot 13	slot 14	slot 15	slot 16	slot 17	slot 18
1	U1 INNER	U17 INNER	U33 INNER	V13 INNER	V29 INNER	W9 INNER	W25 INNER	U1 OUTER	U17 OUTER	U33 OUTER	V13 OUTER	V29 OUTER	W5 OUTER	W25 OUTER	W5 OUTER	W25 OUTER	
2	U2 INNER	U18 INNER	U34 INNER	V14 INNER	V30 INNER	W0 INNER	W26 INNER	U2 OUTER	U18 OUTER	U34 OUTER	V14 OUTER	V30 OUTER	W10 OUTER	W26 OUTER	W10 OUTER	W26 OUTER	
3	U3 INNER	U19 INNER	U35 INNER	V15 INNER	V31 INNER	W11 INNER	W27 INNER	U3 OUTER	U19 OUTER	U35 OUTER	V15 OUTER	V31 OUTER	W11 OUTER	W27 OUTER	W11 OUTER	W27 OUTER	
4	U4 INNER	U20 INNER	U36 INNER	V16 INNER	V32 INNER	W12 INNER	W28 INNER	U4 OUTER	U20 OUTER	U36 OUTER	V16 OUTER	V32 OUTER	W12 OUTER	W28 OUTER	W12 OUTER	W28 OUTER	
5	U5 INNER	U21 INNER	V1 INNER	V17 INNER	V33 INNER	W13 INNER	W29 INNER	U5 OUTER	U21 OUTER	V1 OUTER	V17 OUTER	V33 OUTER	W13 OUTER	W29 OUTER	W13 OUTER	W29 OUTER	
6	U6 INNER	U22 INNER	V2 INNER	V18 INNER	V34 INNER	W14 INNER	W30 INNER	U6 OUTER	U22 OUTER	V2 OUTER	V18 OUTER	V34 OUTER	W14 OUTER	W30 OUTER	W14 OUTER	W30 OUTER	
7	U7 INNER	U23 INNER	V3 INNER	V19 INNER	V35 INNER	W15 INNER	W31 INNER	U7 OUTER	U23 OUTER	V3 OUTER	V19 OUTER	V35 OUTER	W15 OUTER	W31 OUTER	W15 OUTER	W31 OUTER	
8	U8 INNER	U24 INNER	V4 INNER	V20 INNER	V36 INNER	W16 INNER	W32 INNER	U8 OUTER	U24 OUTER	V4 OUTER	V20 OUTER	V36 OUTER	W16 OUTER	W32 OUTER	W16 OUTER	W32 OUTER	
9	U9 INNER	U25 INNER	V5 INNER	V21 INNER	W1 INNER	W17 INNER	W33 INNER	U9 OUTER	U25 OUTER	V5 OUTER	V21 OUTER	W1 OUTER	W17 OUTER	W33 OUTER	W17 OUTER	W33 OUTER	
10	U10 INNER	U26 INNER	V6 INNER	V22 INNER	W2 INNER	W18 INNER	W34 INNER	U10 OUTER	U26 OUTER	V6 OUTER	V22 OUTER	W2 OUTER	W18 OUTER	W34 OUTER	W18 OUTER	W34 OUTER	
11	U11 INNER	U27 INNER	V7 INNER	V23 INNER	W3 INNER	W19 INNER	W35 INNER	U11 OUTER	U27 OUTER	V7 OUTER	V23 OUTER	W3 OUTER	W19 OUTER	W35 OUTER	W19 OUTER	W35 OUTER	
12	U12 INNER	U28 INNER	V8 INNER	V24 INNER	W4 INNER	W20 INNER	W36 INNER	U12 OUTER	U28 OUTER	V8 OUTER	V24 OUTER	W4 OUTER	W20 OUTER	W36 OUTER	W20 OUTER	W36 OUTER	
13	U13 INNER	U29 INNER	V9 INNER	V25 INNER	W5 INNER	W21 INNER		U13 OUTER	U29 OUTER	V9 OUTER	V25 OUTER	W5 OUTER	W21 OUTER		W21 OUTER		
14	U14 INNER	U30 INNER	V10 INNER	V26 INNER	W6 INNER	W22 INNER		U14 OUTER	U30 OUTER	V10 OUTER	V26 OUTER	W6 OUTER	W22 OUTER		W22 OUTER		
15	U15 INNER	U31 INNER	V11 INNER	V27 INNER	W7 INNER	W23 INNER		U15 OUTER	U31 OUTER	V11 OUTER	V27 OUTER	W7 OUTER	W23 OUTER		W23 OUTER		
16	U16 INNER	U32 INNER	V12 INNER	V28 INNER	W8 INNER	W24 INNER		U16 OUTER	U32 OUTER	V12 OUTER	V28 OUTER	W8 OUTER	W24 OUTER		W24 OUTER		
	DISC	DISC	DISC	DISC	TDC	DISC	TDC	DISC	DISC								

ecal-disc-map.xlsx
Modified: 8/24/16

Figure 3.15: Electronics map for the input connections to the ECAL VME discriminators. Twisted-pair ribbon cables make the connections to the V1190 TDCs is slots 6 and 16.

PCAL HV Mapping
pcal-hvmap.xlsx
1/6/16

Slot \ Ch	Det.														
8\00	U1	9\00	U25	10\00	U49	11\00	V5	12\00	V29	13\00	V53	14\00	W15	15\00	W39
8\01	U2	9\01	U26	10\01	U50	11\01	V6	12\01	V30	13\01	V54	14\01	W16	15\01	W40
8\02	U3	9\02	U27	10\02	U51	11\02	V7	12\02	V31	13\02	V55	14\02	W17	15\02	W41
8\03	U4	9\03	U28	10\03	U52	11\03	V8	12\03	V32	13\03	V56	14\03	W18	15\03	W42
8\04	U5	9\04	U29	10\04	U53	11\04	V9	12\04	V33	13\04	V57	14\04	W19	15\04	W43
8\05	U6	9\05	U30	10\05	U54	11\05	V10	12\05	V34	13\05	V58	14\05	W20	15\05	W44
8\06	U7	9\06	U31	10\06	U55	11\06	V11	12\06	V35	13\06	V59	14\06	W21	15\06	W45
8\07	U8	9\07	U32	10\07	U56	11\07	V12	12\07	V36	13\07	V60	14\07	W22	15\07	W46
8\08	U9	9\08	U33	10\08	U57	11\08	V13	12\08	V37	13\08	V61	14\08	W23	15\08	W47
8\09	U10	9\09	U34	10\09	U58	11\09	V14	12\09	V38	13\09	V62	14\09	W24	15\09	W48
8\10	U11	9\10	U35	10\10	U59	11\10	V15	12\10	V39	13\10	W1	14\10	W25	15\10	W49
8\11	U12	9\11	U36	10\11	U60	11\11	V16	12\11	V40	13\11	W2	14\11	W26	15\11	W50
8\12	U13	9\12	U37	10\12	U61	11\12	V17	12\12	V41	13\12	W3	14\12	W27	15\12	W51
8\13	U14	9\13	U38	10\13	U62	11\13	V18	12\13	V42	13\13	W4	14\13	W28	15\13	W52
8\14	U15	9\14	U39	10\14	U63	11\14	V19	12\14	V43	13\14	W5	14\14	W29	15\14	W55
8\15	U16	9\15	U40	10\15	U64	11\15	V20	12\15	V44	13\15	W6	14\15	W30	15\15	W54
8\16	U17	9\16	U41	10\16	U65	11\16	V21	12\16	V45	13\16	W7	14\16	W31	15\16	W55
8\17	U18	9\17	U42	10\17	U66	11\17	V22	12\17	V46	13\17	W8	14\17	W32	15\17	W56
8\18	U19	9\18	U43	10\18	U67	11\18	V23	12\18	V47	13\18	W9	14\18	W33	15\18	W57
8\19	U20	9\19	U44	10\19	U68	11\19	V24	12\19	V48	13\19	W10	14\19	W34	15\19	W58
8\20	U21	9\20	U45	10\20	V1	11\20	V25	12\20	V49	13\20	W11	14\20	W35	15\20	W59
8\21	U22	9\21	U46	10\21	V2	11\21	V26	12\21	V50	13\21	W12	14\21	W36	15\21	W60
8\22	U23	9\22	U47	10\22	V3	11\22	V27	12\22	V51	13\22	W13	14\22	W37	15\22	W61
8\23	U24	9\23	U48	10\23	V4	11\23	V28	12\23	V52	13\23	W14	14\23	W38	15\23	W62

The layout of the 6 FTOF/PCAL HV crates (one for each sector) is identical

Figure 3.16: HV mainframe PCAL channel assignments for each sector.

ECAL HV Mapping
ecal-hvmap.xlsx
8/24/16

Slot \ Ch	Det.																					
0\00	U1 INNER	1\00	U25 INNER	2\00	V13 INNER	3\00	W1 INNER	4\00	W25 INNER	5\00	U13 OUTER	6\00	V1 OUTER	7\00	V25 OUTER	8\00	W13 OUTER	8\00	W13 OUTER	8\00	W13 OUTER	8\00
0\01	U2 INNER	1\01	U26 INNER	2\01	V14 INNER	3\01	W2 INNER	4\01	W26 INNER	5\01	U14 OUTER	6\01	V2 OUTER	7\01	V26 OUTER	8\01	W14 OUTER	8\01	W14 OUTER	8\01	W14 OUTER	8\01
0\02	U3 INNER	1\02	U27 INNER	2\02	V15 INNER	3\02	W3 INNER	4\02	W27 INNER	5\02	U15 OUTER	6\02	V3 OUTER	7\02	V27 OUTER	8\02	W15 OUTER	8\02	W15 OUTER	8\02	W15 OUTER	8\02
0\03	U4 INNER	1\03	U28 INNER	2\03	V16 INNER	3\03	W4 INNER	4\03	W28 INNER	5\03	U16 OUTER	6\03	V4 OUTER	7\03	V28 OUTER	8\03	W16 OUTER	8\03	W16 OUTER	8\03	W16 OUTER	8\03
0\04	U5 INNER	1\04	U29 INNER	2\04	V17 INNER	3\04	W5 INNER	4\04	W29 INNER	5\04	U17 OUTER	6\04	V5 OUTER	7\04	V29 OUTER	8\04	W17 OUTER	8\04	W17 OUTER	8\04	W17 OUTER	8\04
0\05	U6 INNER	1\05	U30 INNER	2\05	V18 INNER	3\05	W6 INNER	4\05	W30 INNER	5\05	U18 OUTER	6\05	V6 OUTER	7\05	V30 OUTER	8\05	W18 OUTER	8\05	W18 OUTER	8\05	W18 OUTER	8\05
0\06	U7 INNER	1\06	U31 INNER	2\06	V19 INNER	3\06	W7 INNER	4\06	W31 INNER	5\06	U19 OUTER	6\06	V7 OUTER	7\06	V31 OUTER	8\06	W19 OUTER	8\06	W19 OUTER	8\06	W19 OUTER	8\06
0\07	U8 INNER	1\07	U32 INNER	2\07	V20 INNER	3\07	W8 INNER	4\07	W32 INNER	5\07	U20 OUTER	6\07	V8 OUTER	7\07	V32 OUTER	8\07	W20 OUTER	8\07	W20 OUTER	8\07	W20 OUTER	8\07
0\08	U9 INNER	1\08	U33 INNER	2\08	V21 INNER	3\08	W9 INNER	4\08	W33 INNER	5\08	U21 OUTER	6\08	V9 OUTER	7\08	V33 OUTER	8\08	W21 OUTER	8\08	W21 OUTER	8\08	W21 OUTER	8\08
0\09	U10 INNER	1\09	U34 INNER	2\09	V22 INNER	3\09	W10 INNER	4\09	W34 INNER	5\09	U22 OUTER	6\09	V10 OUTER	7\09	V34 OUTER	8\09	W22 OUTER	8\09	W22 OUTER	8\09	W22 OUTER	8\09
0\10	U11 INNER	1\10	U35 INNER	2\10	V23 INNER	3\10	W11 INNER	4\10	W35 INNER	5\10	U23 OUTER	6\10	V11 OUTER	7\10	V35 OUTER	8\10	W23 OUTER	8\10	W23 OUTER	8\10	W23 OUTER	8\10
0\11	U12 INNER	1\11	U36 INNER	2\11	V24 INNER	3\11	W12 INNER	4\11	W36 INNER	5\11	U24 OUTER	6\11	V12 OUTER	7\11	V36 OUTER	8\11	W24 OUTER	8\11	W24 OUTER	8\11	W24 OUTER	8\11
0\12	U13 INNER	1\12	V11 INNER	2\12	V25 INNER	3\12	W13 INNER	4\12	U1 OUTER	5\12	U25 OUTER	6\12	V13 OUTER	7\12	W1 OUTER	8\12	W25 OUTER	8\12	W25 OUTER	8\12	W25 OUTER	8\12
0\13	U14 INNER	1\13	V2 INNER	2\13	V26 INNER	3\13	W14 INNER	4\13	U2 OUTER	5\13	U26 OUTER	6\13	V14 OUTER	7\13	W2 OUTER	8\13	W26 OUTER	8\13	W26 OUTER	8\13	W26 OUTER	8\13
0\14	U15 INNER	1\14	V3 INNER	2\14	V27 INNER	3\14	W15 INNER	4\14	U3 OUTER	5\14	U27 OUTER	6\14	V15 OUTER	7\14	W3 OUTER	8\14	W27 OUTER	8\14	W27 OUTER	8\14	W27 OUTER	8\14
0\15	U16 INNER	1\15	V4 INNER	2\15	V28 INNER	3\15	W16 INNER	4\15	U4 OUTER	5\15	U28 OUTER	6\15	V16 OUTER	7\15	W4 OUTER	8\15	W28 OUTER	8\15	W28 OUTER	8\15	W28 OUTER	8\15
0\16	U17 INNER	1\16	V5 INNER	2\16	V29 INNER	3\16	W17 INNER	4\16	U5 OUTER	5\16	U29 OUTER	6\16	V17 OUTER	7\16	W5 OUTER	8\16	W29 OUTER	8\16	W29 OUTER	8\16	W29 OUTER	8\16
0\17	U18 INNER	1\17	V6 INNER	2\17	V30 INNER	3\17	W18 INNER	4\17	U6 OUTER	5\17	U30 OUTER	6\17	V18 OUTER	7\17	W6 OUTER	8\17	W30 OUTER	8\17	W30 OUTER	8\17	W30 OUTER	8\17
0\18	U19 INNER	1\18	V7 INNER	2\18	V31 INNER	3\18	W19 INNER	4\18	U7 OUTER	5\18	U31 OUTER	6\18	V19 OUTER	7\18	W7 OUTER	8\18	W31 OUTER	8\18	W31 OUTER	8\18	W31 OUTER	8\18
0\19	U20 INNER	1\19	V8 INNER	2\19	V32 INNER	3\19	W20 INNER	4\19	U8 OUTER	5\19	U32 OUTER	6\19	V20 OUTER	7\19	W8 OUTER	8\19	W32 OUTER	8\19	W32 OUTER	8\19	W32 OUTER	8\19
0\20	U21 INNER	1\20	V9 INNER	2\20	V33 INNER	3\20	W21 INNER	4\20	U9 OUTER	5\20	U33 OUTER	6\20	V21 OUTER	7\20	W9 OUTER	8\20	W33 OUTER	8\20	W33 OUTER	8\20	W33 OUTER	8\20
0\21	U22 INNER	1\21	V10 INNER	2\21	V34 INNER	3\21	W22 INNER	4\21	U10 OUTER	5\21	U34 OUTER	6\21	V22 OUTER	7\21	W10 OUTER	8\21	W34 OUTER	8\21	W34 OUTER	8\21	W34 OUTER	8\21
0\22	U23 INNER	1\22	V11 INNER	2\22	V35 INNER	3\22	W23 INNER	4\22	U11 OUTER	5\22	U35 OUTER	6\22	V23 OUTER	7\22	W11 OUTER	8\22	W35 OUTER	8\22	W35 OUTER	8\22	W35 OUTER	8\22
0\23	U24 INNER	1\23	V12 INNER	2\23	V36 INNER	3\23	W24 INNER	4\23	U12 OUTER	5\23	U36 OUTER	6\23	V24 OUTER	7\23	W12 OUTER	8\23	W36 OUTER	8\23	W36 OUTER	8\23	W36 OUTER	8\23

Figure 3.17: HV mainframe ECAL channel assignments for each sector.

3.4 System Failure Modes

For the EC detector, there are a number of usual “failure” modes with which the system expert should be familiar. These include the following:

- Replacing a HV board (see Section 3.4.1).
- Sudden ADC gain shift (see Section 3.4.2).
- High PMT dark current (see Section 3.4.3).
- Missing anode signal (see Section 3.4.4).
- Bad PMT (see Section 3.4.5).
- Readout electronics issues (see Section 3.4.6).
- IOC issues (see Section 3.4.7).

3.4.1 HV Board Replacement

The evidence for a bad HV board (A1535N) is either that the 24 channels associated with a single board won’t ramp up to full voltage before tripping off or bad voltage regulation. For the case of bad voltage regulation, the channels ramp up to full voltage but then fluctuate about the demand voltage setting by up to several hundred volts. Before deciding whether a HV board is bad, some investigation should be completed to ensure that a single HV channel is not causing the problems with the board, which could point to a problem with the PMT or voltage divider. If a board is deemed bad and needs to be replaced, the following steps are necessary:

1. Take a spare A1535N board from the storage area on the second level of the Pie Tower in Hall B.
2. Turn the front panel key on the HV supply to the “off” position and toggle the main power switch to “off” on the back of the HV supply.
3. On the back of the supply, remove the Radiall connector on the bad board.
4. Pull out the bad board, being careful of the Radiall connectors on the neighboring boards.
5. Install the new board and reconnect the Radiall connector.
6. Toggle the main power switch to “on” and turn the HV power supply on using the key on the front panel, putting the key in the “local” position.
7. Run all parameter scripts for the HV power supply to load all channel parameters. See instructions in Section 3.2.1.
8. Enter information on the new board and the old bad board into the Hall B equipment database (see the Appendix).
9. Leave the bad board on the RadCon Survey table in Hall B.

3.4.2 Sudden Gain Shift

Sometimes a sudden gain shift can appear in the ADC spectra for a given counter. There are a number of possible causes for such a condition.

- Problematic PMT - sometimes gain shifts can be attributed to a problem with a PMT that requires adjustment of the HV settings. Of course, PMT gain issues typically lead to a reduced gain that requires an increase of the HV.
- DAQ Problems - the most common cause for an apparent gain shift in the ADC spectra for a counter is due to problems with the FADC settings. Such problems can typically be diagnosed from pedestal shifts or widened pedestals. The pedestals can be checked by taking FADC data in “raw mode”.
- Light Leak - it is possible that a gain shift can be due to hardware damage or a light leak on the counter.

3.4.3 High PMT Dark Current

3.4.4 Missing Anode or Dynode Signal

3.4.5 Bad PMT

One of the most common failure modes of a PMT is a gradual loss of gain over the period of several years. This can be compensated by adjusting the HV to maintain the gain setting. The PMTs used in the EC system have maximum voltage ratings of -2500 V for the ECAL PMTs and -1100 V for the PCAL PMTs. Once the PMT HV is set to its maximum value and the gain falls below the nominal setting, the PMT should be flagged for replacement during the next servicing opportunity.

3.4.6 Readout Electronics Issues

Readout electronics issues, typically associated with all channels associated with a given discriminator board, TDC board, or FADC board, once diagnosed should be brought to the attention of the DAQ system expert for further diagnosis and attention.

3.4.7 IOC Issues

Loss of communication between the IOC and the HV mainframe is seen by a yellow color status for all HV channels in a given sector. The IOC should be reset following the instructions given in Section 2.2. If resetting the IOC does not solve the problems, contact the Slow Controls system expert.

3.5 Detector Repairs and Servicing

Repairs and servicing of the physical structure of the EC detectors is limited to maintaining light-tight tape seals along the known openings and sheet metal seams. Black 3M tape is visible in numerous locations and usually indicates where energized PMTs were able to detect significant light leaks. These seals must be maintained to prevent excessive count rates in the PMTs. Repair and replacement of defective PMTs and HV dividers will be necessary as time passes.

All EC detector repairs will be organized through the EC Group Leader in conjunction with the Hall B Work Coordinator to be scheduled during a planned major down time for Hall B.

4 Documentation

All current documentation for the EC system is located on the official EC web page [4]. A number of basic subsystem documents can be found there including:

- EC System Operations Manual (this document)
- EC Geometry Document
- EC Calibration Constants
- EC Monte Carlo Simulation Details
- EC Reconstruction Document
- Assorted photographs of the detector hardware

5 EC Authorized Personnel

Beyond turning on/off the EC system HV and monitoring the system scalers, all other operations and repairs are only to be carried out by the list of authorized personnel shown in Table 3. The list of authorized personnel for EC can only be modified by the EC Group Leader.

Name	Telephone	email	Area
Stepan Stepanyan	757-269-7196	stepanya@jlab.org	EC Group Leader
Cole Smith	434-249-4307	lcsmith@jlab.org	Hardware
Daniel Carman	757-269-5586	carman@jlab.org	Hardware
Sergey Boyarinov	757-269-5795	boyarinov@jlab.org	DAQ
Nathan Baltzell	757-269-5902	baltzell@jlab.org	Slow Controls

Table 3: EC detector authorized personnel.

6 Appendix: Hall B Instrumentation Database

When electronics modules or HV modules are removed from Hall B and replaced during servicing with new boards, the information regarding both the old board and the new board need to be entered into the Hall B Instrumentation Database. This database is accessed online at <http://clonwiki0.jlab.org> by clicking on the “Hall B Inventory” link. This brings up the access screen shown in Fig. 6.1. To enter information for the old component, search for it in the database using its property tag information. When the item shows up, click on the “Action” button for “Modify this item”. Be sure to change the location of the item to “Hall B Underground/RadCon Table” and change the status of the item to “Action needed/Broken”, as well as to leave the item on the RadCon survey table in Hall B. By entering this information, email will be sent to the property custodian to pick up the item for servicing. For the new component, be sure to also change the location as appropriate using the same approach.

The screenshot shows a web browser window with the URL clonwiki0.jlab.org. The page title is "JInventory database in use by CUE user 'carman' with 'read/write' access". The main content area is titled "Items" and contains a search form with fields for "Item ID", "Housing Parent | Ancestor", "Property Tag", "Short name and description", and "Brand-Format-Model". Below the search form is a table listing five equipment items:

Check	Property Tag (Serial number)	ID	Short name	Description	Housing	Custodian	Insert Date	Action
<input type="checkbox"/>	BI000471 (CEM-TI-204)	6275	TI board	JLAB TI	Hall B underground (5168) PI (Pie Tower) (5177) PI2-5 (rack) (5215) VME64x crate (5585) * slot 8	Sergey Boyarinov	2016-07-25 10:40:15	
<input type="checkbox"/>	BI000470 (CEM-TI-210)	6274	TI board	JLAB TI	Hall B underground (5168) PI (Pie Tower) (5177) PI2-5 (rack) (5215) VME64x crate (5585) * slot 15	Sergey Boyarinov	2016-07-25 10:37:23	
<input type="checkbox"/>	BI000469 (CEM-TI-207)	6273	TI board	JLAB TI	Hall B underground (5168) FC (Forward Carriage) (5169) C1-2 (rack) (5189) VME64x crate "tdcpcal5" (4353) * slot 21	Sergey Boyarinov	2016-07-20 14:25:22	
<input type="checkbox"/>	BI001406 (B55561)	6272	LeCroy VME board 1182	LeCroy VME board 1182 ADC	Bldg. 90 (EEL) (5173) 208A (room) (5252) WIENER VME Mini Crate (6267) * Slot 6		2016-06-27 15:51:23	
<input type="checkbox"/>	PPOM0712 (233)	6270	TDC 32 ch.	CAEN V775	Bldg. 90 (EEL) (5173) 208A (room) (5252) WIENER VME Mini Crate (6267)	Sergey Boyarinov	2016-06-27 15:46:32	
	BI001405	6260	Multicount DDC 32 ch.	CAEN V773	Bldg. 90 (EEL) (5173)	Sergey	2016-06-27	

Figure 6.1: Hall B equipment database web page.

References

- [1] Hall B Electronic Logbook: <https://logbooks.jlab.org/book/hblog>
- [2] Hall B BEAST alarm handler:
https://clasweb.jlab.org/wiki/index.php/Slow_Control_Alarms
- [3] FCMON:
<https://github.com/forcar/fc/wiki/FCMON>
- [4] EC web page:
https://clasweb.jlab.org/wiki/index.php/CLAS12_Forward_Electromagnetic_Calorimeter