Flash ADC board:

4ns

time

baseline

threshold

1. First hit above threshold: start sum window, add previous hit to it

2. First hit below threshold: add that hit to the window, close window; we have now ADC value and WINDOW_SIZE

3. Wait DELAY ns and send ADC valie to the CTP board
   (DELAY = DELAY0 – WINDOW_SIZE, where DELAY0 is delay constant for all channels, order of 128ns; this way sending time will be related to the beginning of the window)

4. Based on bandwidth 8GBit/s we can send 16bits per channel every 32ns including channels without info, or pack data

CTP board:

Flash ADC board signal processing logic
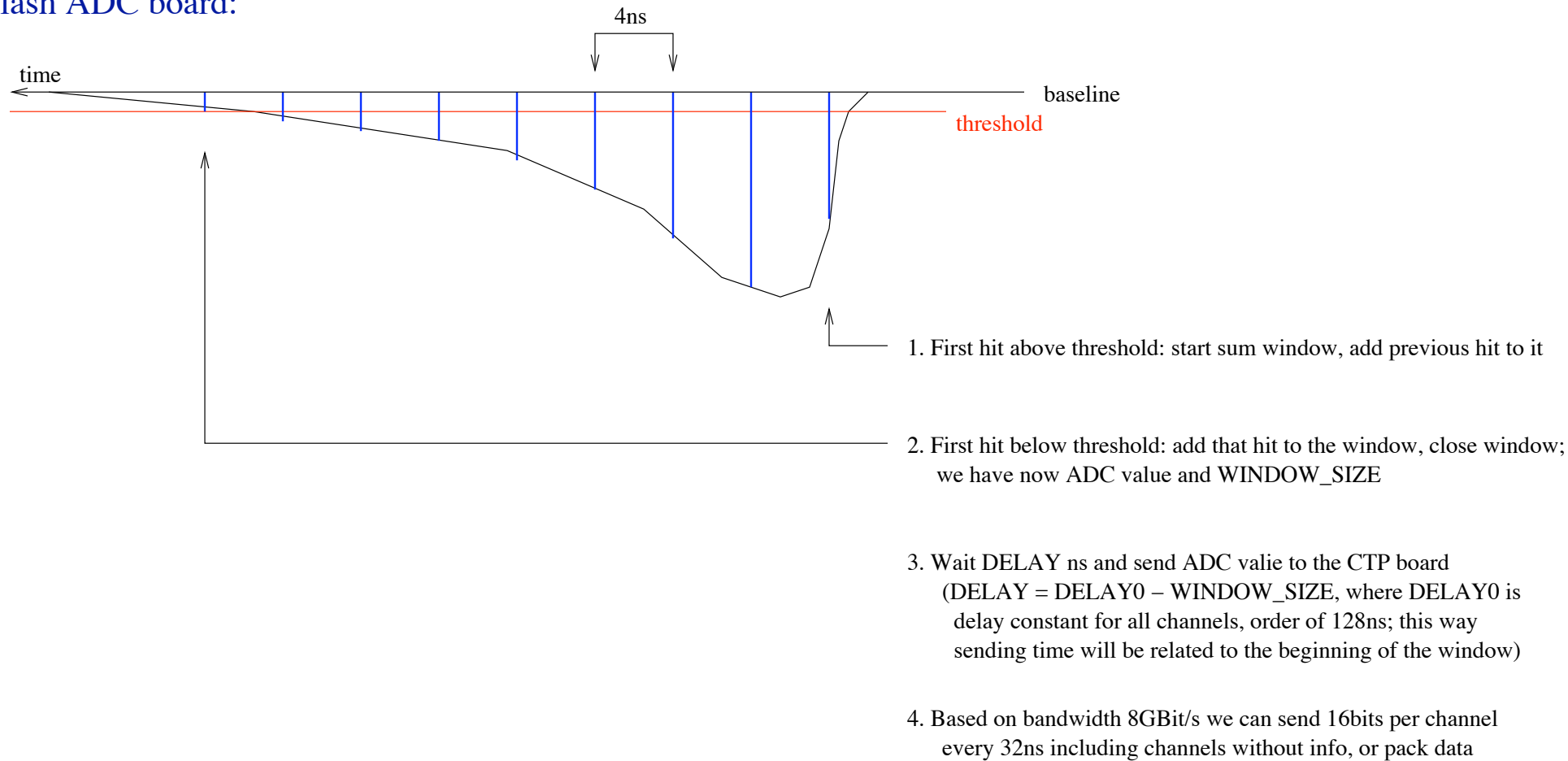
1. Does not have information about original sum window width

2. Expands every window up to the value (programmable) big enough to enforce coincidence between different channels

3. Every channel has programmable delay (4ns step) and readable scaler