# FPGA Program Specifications for the LED Pulsing Application for GlueX Calorimeters Using CAEN V1495 Board

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This application is designed to use CAEN V1495 VME board as a pulser using all ports on the C, D, E, F connectors for Hall D calorimeter monitoring systems. All 24 ports on the D, E, and F connectors are used as individual pulsing outputs. Port 31 (last one) on the C-connector should be configured as the MasterOR of the pulses on all other ports on C, D, E, F connectors. This is specified for DAQ triggering purposes, and for the user is somewhat similar to what G port is for in V1495 Reference Design. The other first 31 ports of the C-connector are used as individual pulse outputs. Therefore, we will have 55 individual pulses and one MasterOR pulse per V1495 board.

The pulser shall start pulsing with default frequency, width and MasterOR delay as soon as it is placed and powered in a VME crate if the dedicated DIP-switch for auto-running is ON. If the dedicated DIP-switch is OFF, there are no pulses on the outputs until pulsing is initiated from the VME controller. The pulser needs to be controllable from the VME controller to set the frequency, the pulse width, the MasterOR delay, as well as to launch and stop the pulse trains when the dedicated DIP-switch is OFF. We will need three identical boards for FCAL and BCAL monitoring system, so G0 and G1 ports can be used for the purposes of synchronization of the boards, if needed. If G0 and/or G1 ports are used for synchronization additional DIP-switches may be needed for clock selection.

Connector/Ports configuration:

* A and B connectors are not used in this application.
* Ports on the C-connector are used as independent 31 LVDS pulse outputs, and the last port (port 31) is programmed as the MasterOR pulse output. MasterOR output pulses every time any of the 55 individual ports pulse.
* G0 and G1 ports are configured for synchronization of the boards. G0 and G1 direction will be set as INPUT, but G1 will be used for OUTPUT, similar to how the ports on the A395D mezzanine board in Reference Design for V1495 are used (?) .
* D, E, F ports are assumed to be provided by A395D daughter boards and shall be configured as 24 independent TTL pulse outputs .
* The correctness of the three mezzanine board configuration shall be checked by the software, therefore the firmware assumes that the right daughter boards are installed.

Registers to be defined:

1. Set frequency of the pulsing for individual 55 outputs (RW) :

* 55x 32 bits, 1 Hz – 1.0 MHz, with 1Hz increment, 0 - continues true level (?), default value is 100Hz.

Implemented with a 32bit counter at 100MHz.

Frequency range is ~1/43Hz to 50MHz

1Hz resolution is not achievable throughout this entire range. For 1Hz to 1MHz, the accuracy will be no worse than 1%, but typically much better especially on the lower end. The actual frequency can be calculated by computing the required divisor needed to create the target frequency (by dividing down the 100MHz reference) – only integer divisors are valid and so the fractional portion is the error.

* if the dedicated DIP-switch is ON, the changes to the pulsing parameters are ignored.

Implemented by used of Spare I/O header. Jumper pins 1-2 to write protect default board values.

1. Set maximum number of pulses for individual 55 outputs (RW) :

* 55x 32 bits, 32 bits, 1 – 0xFFFFFFFF, 0 – means pulsing infinitely until stopped, default is infinity.

The implemented definition is slightly different from above: 0 – disables the pulse, 1-0xFFFFFFFE is the finite pulse count, 0xFFFFFFFF – pulser counts forever

* if the dedicated DIP-switch is ON, the changes to the pulsing parameters are ignored.

1. Set pulse width for individual 55 outputs and the MasterOR output (R/W) :

* 56x 32 bits 10ns – 1000ns, 10ns increment, default value is 100ns.

Implemented

* if the dedicated DIP-switch is ON, the changes to the pulsing parameters are ignored.

1. Set MasterOR pulse delay with respect to the original pulse time (RW) :

* 32 bits, 0ns – 10000ns, 10ns increment, default value is 0ns.

Implemented. 0 to 40,950ns delay in 10ns incremented.

* if the dedicated DIP-switch is ON, the changes to the pulsing parameters are ignored.

1. Start enable mask (RW):

Implemented

* 64 bits used as an enable mask to determine for which registers to start pulsing .
* if the mask is inconsistent with the installed boards, still continue as if all are present.
* writing to this register does not start pulsing.
* if the dedicated DIP-switch is ON, the changes to the pulsing parameters are ignored.

1. Stop enable mask (RW):

Implemented

* 64 bits used as an enable mask to determine for which registers to stop pulsing.
* if the mask is inconsistent with the installed boards, still continue as if all are present.
* writing to this register does not stop pulsing.
* if the dedicated DIP-switch is ON, the changes to the pulsing parameters are ignored.

1. Pulsing status of the individual ports (RO):

Implemented

* 64 bits (55 are actually meaningful) to indicate the status of the pulsing of each individual output (1-pulsing/0-not pulsing).

1. Start/Stop pulsing (WO):

Implemented

* only single bit is needed: START transition and STOP transition.
* writing “1” to this register starts pulsing out of the ports enabled by the start enable mask.
* writing “0” to this register stops pulsing out of the ports enabled by the stop enable mask.
* writing any other value to this register is ignored.
* if the dedicated DIP-switch is ON, the board continues pulsing as before.
* if the mask is inconsistent with the installed boards, still continue as if all boards are present.

# VME Registers

All V1495 pulser board registers can be accessed through the VME bus in the following mode:

* A32/A24: single cycle accesses, 32bit aligned, read or write access (register specific)

**Register Summary:**

|  |  |  |
| --- | --- | --- |
| **Register Name** | **Description** | **Address Offset** |
| **Board Information** |  |  |
| **A\_PULSERID** | Board identification | 0x1000 |
| **A\_FIRMWARE\_REV** | Firmware revision | 0x1004 |
| **A\_BOARDID** | A395x Daughter Board IDs | 0x1008 |
| **A\_JUMPERS** | Jumper Configuration | 0x100C |
| **A\_NIMTTL** | NIM/TTL daugherboard mode | 0x1034 |
|  |  |  |
| **Global Pulser Configuration** |  |  |
| **A\_PULSER\_STATUS\_H** | Pulser Active Status | 0x1010 |
| **A\_PULSER\_STATUS\_L** |  | 0x1014 |
| **A\_PULSER\_START\_MASK\_H** | Pulser Start Mask | 0x1018 |
| **A\_PULSER\_START\_MASK\_L** |  | 0x101C |
| **A\_PULSER\_STOP\_MASK\_H** | Pulser Stop Mask | 0x1020 |
| **A\_PULSER\_STOP\_MASK\_L** |  | 0x1024 |
| **A\_PULSER\_GIN\_MASK\_H** | Pulser GIN OR Mask | 0x1028 |
| **A\_PULSER\_GIN\_MASK\_L** |  | 0x102C |
| **A\_PULSER\_START\_STOP** | Pulser Start/Stop | 0x1030 |
| **A\_MASTEROR\_DELAY** | Master OR Output Delay | 0x1100 |
| **A\_MASTEROR\_WIDTH** | Master OR Output Width | 0x1104 |
| **A\_PULSER\_MOR\_MASK\_H** | Master OR output Mask | 0x1038 |
| **A\_PULSER\_MOR\_MASK\_L** |  | 0x103C |
|  |  |  |
| **Pulser Channel Configuration** |  |  |
| **A\_PERIOD** | Pulser Pulse Period | 0x2000+0x10\*ch |
| **A\_WIDTH** | Pulser Pulse Width | 0x2004+0x10\*ch |
| **A\_NPULSES** | Pulser Pulse Count | 0x2008+0x10\*ch |

**Register: A\_PULSERID**

Address Offset: 0x1000

Size: 32bits

Reset State: 0x50554C53

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PULSERID | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PULSERID | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PULSERID | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PULSERID | | | | | | | |

**PULSERID (RO):**

0x50554C53 = “PULS” in ASCII

**Register: A\_FIRMWARE\_REV**

Address Offset: 0x1004

Size: 32bits

Reset State: 0xXXXXXXXX

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FIRMWARE\_REVISION\_MAJOR | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FIRMWARE\_REVISION\_MAJOR | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| FIRMWARE\_REVISION\_MINOR | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FIRMWARE\_REVISION\_MINOR | | | | | | | |

**FIRMWARE\_REVISION\_MAJOR (RO):**

16bit Major Firmware Revision Number

**FIRMWARE\_REVISION\_MINOR (RO):**

16bit Minor Firmware Revision Number

**Notes:**

1. A register value of 0x00010000 would be read as “V1.0”,

A register value of 0x00020003 would be read as “V2.3”, etc.

1. Major revision number will increment when significant changes are made that are not compatible with the previous version
2. Minor revision number will increment on bug fixes or feature additions that preserve compatibility with the previous version

**Register: A\_BOARDID**

Address Offset: 0x1008

Size: 32bits

Reset State: 0xXXXXXXXX

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| - | - | - | - | - | - | - | - |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| - | - | - | - | - | - | - | - |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| - | - | - | - | - | IDF | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | IDE | | | - | IDD | | |

**IDx (RO):**

Mezzanine board X Identifier

**Notes:**

1. “000” = A395A, 32 input ECL/LVDS

“001” = A395B, 32 output LVDS

“010” = A395C, 32 output ECL

“011” = A395D, 8 input/output NIM/TTL

**Register: A\_JUMPERS**

Address Offset: 0x100C

Size: 32bits

Reset State: 0xXXXXXXXX

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | | 25 | | 24 |
| - | - | - | - | - | | - | | - | - |
| 23 | 22 | 21 | 20 | 19 | 18 | | 17 | | 16 |
| - | - | - | - | - | | - | | - | - |
| 15 | 14 | 13 | 12 | 11 | 10 | | 9 | | 8 |
| - | - | - | - | - | | - | | - | - |
| 7 | 6 | 5 | 4 | 3 | 2 | | 1 | | 0 |
| - | - | JMP5 | JMP4 | JMP3 | | JMP2 | | JMP1 | JMP0 |

**JMPx (RO):**

‘1’ – indicates jumper is installed at position X on spare I/O header

‘0’ – indicates no jumper is installed at position X on spare I/O header

**Notes:**

1. JMP0 is the write register write protect enable jumper. If installed no registers are writable.

**Register: A\_PULSER\_STATUS\_H**

Address Offset: 0x1010

Size: 32bits

Reset State: 0xXXXXXXXX

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| - | - | - | - | - | - | - | - |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CH55 | CH54 | CH53 | CH52 | CH51 | CH50 | CH49 | CH48 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CH47 | CH46 | CH45 | CH44 | CH43 | CH42 | CH41 | CH40 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH39 | CH38 | CH37 | CH36 | CH35 | CH34 | CH33 | CH32 |

**CHx (RO):**

‘1’ – indicates pulser channel x is active

‘0’ – indicates pulser channel x is not active

**Notes:**

1. Ch0-30 => port C 0-30
2. Ch31-38 => port D 0-7
3. Ch39-46 => port E 0-7
4. Ch47-54 => port F 0-7
5. Ch55 => port G 1

**Register: A\_PULSER\_STATUS\_L**

Address Offset: 0x1014

Size: 32bits

Reset State: 0xXXXXXXXX

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | | 25 | | 24 |
| CH31 | CH30 | CH29 | CH28 | CH27 | | CH26 | | CH25 | CH24 |
| 23 | 22 | 21 | 20 | 19 | 18 | | 17 | | 16 |
| CH23 | CH22 | CH21 | CH20 | CH19 | | CH18 | | CH17 | CH16 |
| 15 | 14 | 13 | 12 | 11 | 10 | | 9 | | 8 |
| CH15 | CH14 | CH13 | CH12 | CH11 | | CH10 | | CH9 | CH8 |
| 7 | 6 | 5 | 4 | 3 | 2 | | 1 | | 0 |
| CH7 | CH6 | CH5 | CH4 | CH3 | | CH2 | | CH1 | CH0 |

**CHx (RO):**

‘1’ – indicates pulser channel x is active

‘0’ – indicates pulser channel x is not active

**Notes:**

1. Ch0-30 => port C 0-30
2. Ch31-38 => port D 0-7
3. Ch39-46 => port E 0-7
4. Ch47-54 => port F 0-7
5. Ch55 => port G 1

**Register: A\_PULSER\_START\_MASK\_H**

Address Offset: 0x1018

Size: 32bits

Reset State: 0x00FFFFFF

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| - | - | - | - | - | - | - | - |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CH55 | CH54 | CH53 | CH52 | CH51 | CH50 | CH49 | CH48 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CH47 | CH46 | CH45 | CH44 | CH43 | CH42 | CH41 | CH40 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH39 | CH38 | CH37 | CH36 | CH35 | CH34 | CH33 | CH32 |

**CHx (RW):**

‘1’ – channel x will be started when a pulser start condition is set

‘0’ – channel x will not be changed on a pulser start condition

**Notes:**

1. Ch0-30 => port C 0-30
2. Ch31-38 => port D 0-7
3. Ch39-46 => port E 0-7
4. Ch47-54 => port F 0-7
5. Ch55 => port G 1

**Register: A\_PULSER\_START\_MASK\_L**

Address Offset: 0x101C

Size: 32bits

Reset State: 0xFFFFFFFF

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | | 25 | | 24 |
| CH31 | CH30 | CH29 | CH28 | CH27 | | CH26 | | CH25 | CH24 |
| 23 | 22 | 21 | 20 | 19 | 18 | | 17 | | 16 |
| CH23 | CH22 | CH21 | CH20 | CH19 | | CH18 | | CH17 | CH16 |
| 15 | 14 | 13 | 12 | 11 | 10 | | 9 | | 8 |
| CH15 | CH14 | CH13 | CH12 | CH11 | | CH10 | | CH9 | CH8 |
| 7 | 6 | 5 | 4 | 3 | 2 | | 1 | | 0 |
| CH7 | CH6 | CH5 | CH4 | CH3 | | CH2 | | CH1 | CH0 |

**CHx (RW):**

‘1’ – channel x will be started when a pulser start condition is set

‘0’ – channel x will not be changed on a pulser start condition

**Notes:**

1. Ch0-30 => port C 0-30
2. Ch31-38 => port D 0-7
3. Ch39-46 => port E 0-7
4. Ch47-54 => port F 0-7
5. Ch55 => port G 1

**Register: A\_PULSER\_STOP\_MASK\_H**

Address Offset: 0x1020

Size: 32bits

Reset State: 0x00FFFFFF

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| - | - | - | - | - | - | - | - |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CH55 | CH54 | CH53 | CH52 | CH51 | CH50 | CH49 | CH48 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CH47 | CH46 | CH45 | CH44 | CH43 | CH42 | CH41 | CH40 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH39 | CH38 | CH37 | CH36 | CH35 | CH34 | CH33 | CH32 |

**CHx (RW):**

‘1’ – channel x will be started when a pulser stop condition is set

‘0’ – channel x will not be changed on a pulser stop condition

**Notes:**

1. Ch0-30 => port C 0-30
2. Ch31-38 => port D 0-7
3. Ch39-46 => port E 0-7
4. Ch47-54 => port F 0-7
5. Ch55 => port G 1

**Register: A\_PULSER\_STOP\_MASK\_L**

Address Offset: 0x1024

Size: 32bits

Reset State: 0xFFFFFFFF

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | | 25 | | 24 |
| CH31 | CH30 | CH29 | CH28 | CH27 | | CH26 | | CH25 | CH24 |
| 23 | 22 | 21 | 20 | 19 | 18 | | 17 | | 16 |
| CH23 | CH22 | CH21 | CH20 | CH19 | | CH18 | | CH17 | CH16 |
| 15 | 14 | 13 | 12 | 11 | 10 | | 9 | | 8 |
| CH15 | CH14 | CH13 | CH12 | CH11 | | CH10 | | CH9 | CH8 |
| 7 | 6 | 5 | 4 | 3 | 2 | | 1 | | 0 |
| CH7 | CH6 | CH5 | CH4 | CH3 | | CH2 | | CH1 | CH0 |

**CHx (RW):**

‘1’ – channel x will be started when a pulser stop condition is set

‘0’ – channel x will not be changed on a pulser stop condition

**Notes:**

1. Ch0-30 => port C 0-30
2. Ch31-38 => port D 0-7
3. Ch39-46 => port E 0-7
4. Ch47-54 => port F 0-7
5. Ch55 => port G 1

**Register: A\_PULSER\_GIN\_MASK\_H**

Address Offset: 0x1028

Size: 32bits

Reset State: 0x00000000

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| - | - | - | - | - | - | - | - |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CH55 | CH54 | CH53 | CH52 | CH51 | CH50 | CH49 | CH48 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CH47 | CH46 | CH45 | CH44 | CH43 | CH42 | CH41 | CH40 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH39 | CH38 | CH37 | CH36 | CH35 | CH34 | CH33 | CH32 |

**CHx (RW):**

‘1’ – GIN(0) will be OR’d with channel x output

‘0’ – GIN(0) will not be OR’d with channel x output

**Notes:**

1. This allows a master/slave option to support a fanning out more than can be done on a single V1495. Normally the master board will set the G1 port pulser to feed the G0 of a slave board. The slave board can then enable the G0 to OR to the selected outputs.
2. Ch0-30 => port C 0-30
3. Ch31-38 => port D 0-7
4. Ch39-46 => port E 0-7
5. Ch47-54 => port F 0-7
6. Ch55 => port G 1

**Register: A\_PULSER\_GIN\_MASK\_L**

Address Offset: 0x102C

Size: 32bits

Reset State: 0x00000000

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | | 25 | | 24 |
| CH31 | CH30 | CH29 | CH28 | CH27 | | CH26 | | CH25 | CH24 |
| 23 | 22 | 21 | 20 | 19 | 18 | | 17 | | 16 |
| CH23 | CH22 | CH21 | CH20 | CH19 | | CH18 | | CH17 | CH16 |
| 15 | 14 | 13 | 12 | 11 | 10 | | 9 | | 8 |
| CH15 | CH14 | CH13 | CH12 | CH11 | | CH10 | | CH9 | CH8 |
| 7 | 6 | 5 | 4 | 3 | 2 | | 1 | | 0 |
| CH7 | CH6 | CH5 | CH4 | CH3 | | CH2 | | CH1 | CH0 |

**CHx (RW):**

‘1’ – GIN(0) will be OR’d with channel x output

‘0’ – GIN(0) will not be OR’d with channel x output

**Notes:**

1. This allows a master/slave option to support a fanning out more than can be done on a single V1495. Normally the master board will set the G1 port pulser to feed the G0 of a slave board. The slave board can then enable the G0 to OR to the selected outputs.
2. Ch0-30 => port C 0-30
3. Ch31-38 => port D 0-7
4. Ch39-46 => port E 0-7
5. Ch47-54 => port F 0-7
6. Ch55 => port G 1

**Register: A\_PULSER\_MOR\_MASK\_H**

Address Offset: 0x1038

Size: 32bits

Reset State: 0x00000000

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| - | - | - | - | - | - | - | - |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CH55 | CH54 | CH53 | CH52 | CH51 | CH50 | CH49 | CH48 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CH47 | CH46 | CH45 | CH44 | CH43 | CH42 | CH41 | CH40 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH39 | CH38 | CH37 | CH36 | CH35 | CH34 | CH33 | CH32 |

**CHx (RW):**

‘1’ – Master OR will be OR’d with channel x output

‘0’ – Master OR will not be OR’d with channel x output

**Notes:**

1. This allows the Master OR signal (which has a programmable delay) to be sent out on any of the normal pulser output channels.
2. Ch0-30 => port C 0-30
3. Ch31-38 => port D 0-7
4. Ch39-46 => port E 0-7
5. Ch47-54 => port F 0-7
6. Ch55 => port G 1

**Register: A\_PULSER\_MOR\_MASK\_L**

Address Offset: 0x103C

Size: 32bits

Reset State: 0x00000000

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | | 25 | | 24 |
| CH31 | CH30 | CH29 | CH28 | CH27 | | CH26 | | CH25 | CH24 |
| 23 | 22 | 21 | 20 | 19 | 18 | | 17 | | 16 |
| CH23 | CH22 | CH21 | CH20 | CH19 | | CH18 | | CH17 | CH16 |
| 15 | 14 | 13 | 12 | 11 | 10 | | 9 | | 8 |
| CH15 | CH14 | CH13 | CH12 | CH11 | | CH10 | | CH9 | CH8 |
| 7 | 6 | 5 | 4 | 3 | 2 | | 1 | | 0 |
| CH7 | CH6 | CH5 | CH4 | CH3 | | CH2 | | CH1 | CH0 |

**CHx (RW):**

‘1’ – Master OR will be OR’d with channel x output

‘0’ – Master OR will not be OR’d with channel x output

**Notes:**

1. This allows the Master OR signal (which has a programmable delay) to be sent out on any of the normal pulser output channels.
2. Ch0-30 => port C 0-30
3. Ch31-38 => port D 0-7
4. Ch39-46 => port E 0-7
5. Ch47-54 => port F 0-7
6. Ch55 => port G 1

**Register: A\_PULSER\_START\_STOP**

Address Offset: 0x1030

Size: 32bits

Reset State: 0xXXXXXXXX

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| - | - | - | - | - | - | - | - |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| - | - | - | - | - | - | - | - |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| - | - | - | - | - | - | - | - |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | - | START |

**START (WO):**

‘1’ – Writing this value starts all pulsers defined by PULSER\_START\_MASK

‘0’ – Write this value stops all pulsers defined by PULSER\_STOP\_MASK

**Notes:**

1. Set the PULSER\_START\_MASK/PULSER\_STOP\_MASK mask registers before writing START
2. This provides the mechanism to synchronously start/stop a set of pulsers

**Register: A\_MASTEROR\_DELAY**

Address Offset: 0x1100

Size: 32bits

Reset State: 0x00000000

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | | 25 | | 24 |
|  |  |  |  |  | |  | |  |  |
| 23 | 22 | 21 | 20 | 19 | 18 | | 17 | | 16 |
|  |  |  |  |  | |  | |  |  |
| 15 | 14 | 13 | 12 | 11 | 10 | | 9 | | 8 |
|  |  |  |  | DELAY | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | | 1 | | 0 |
| DELAY | | | | | | | | | |

**DELAY (RW):**

0 – 4095: Sets Master OR (Port C, bit 31) output delay in 10ns ticks. A delay value of 0 will give roughly no delay with respect to the other pulse outputs

**Register: A\_MASTEROR\_WIDTH**

Address Offset: 0x1104

Size: 32bits

Reset State: 0x0000000A

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | | 25 | | 24 |
| - | - | - | - | - | | - | | - | - |
| 23 | 22 | 21 | 20 | 19 | 18 | | 17 | | 16 |
| - | - | - | - | - | | - | | - | - |
| 15 | 14 | 13 | 12 | 11 | 10 | | 9 | | 8 |
| - | - | - | - | - | | - | | - | - |
| 7 | 6 | 5 | 4 | 3 | 2 | | 1 | | 0 |
| WIDTH | | | | | | | | | |

**WIDTH (RW):**

0 – 255: Sets Master OR (Port C, bit 31) output width in 10ns ticks. If a rising edge to the MasterOR input happens while the MasterOR output is high then the input will be ignored (i.e. the MasterOR pulse width runs in non-updating mode).

**Register: A\_PERIOD**

Address Offset: 0x2000 + 0x10\*CH

Size: 32bits

Reset State: 0x000F423F

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PERIOD | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PERIOD | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PERIOD | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PERIOD | | | | | | | |

**PERIOD (RW):**

0 – 0xFFFFFFFF: Pulser period = (PERIOD+1)\*10ns.

**Notes:**

1. The actual period of the pulser is the register PERIOD value plus 1.

**Register: A\_WIDTH**

Address Offset: 0x2004 + 0x10\*CH

Size: 32bits

Reset State: 0x0000000A

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| WIDTH | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WIDTH | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| WIDTH | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| WIDTH | | | | | | | |

**WIDTH (RW):**

0 – 0xFFFFFFFF: Pulser pulse width = WIDTH\*10ns

**Register: A\_NPULSES**

Address Offset: 0x2008 + 0x10\*CH

Size: 32bits

Reset State: 0xFFFFFFFF

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NPULSES | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NPULSES | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| NPULSES | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NPULSES | | | | | | | |

**NPULSES (RW):**

0x00000000: Disables pulser

0x00000001-0xFFFFFFFE: When START is issues, the channel will issue this number of pulses

0xFFFFFFFF: Always enabled pulser output

**Register: A\_NIMTTL**

Address Offset: 0x1034

Size: 32bits

Reset State: 0x00000003

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | | 25 | | 24 | |
| - | - | - | - | - | | - | | - | | - |
| 23 | 22 | 21 | 20 | 19 | 18 | | 17 | | 16 | |
| - | - | - | - | - | | - | | - | | - |
| 15 | 14 | 13 | 12 | 11 | 10 | | 9 | | 8 | |
| - | - | - | - | - | | - | | - | | - |
| 7 | 6 | 5 | 4 | 3 | 2 | | 1 | | 0 | |
| - | - | - | - | - | | SELF | | SELE | | SELD |

**SELx (RW):**

‘0’ – sets NIM/TTL daughter ‘x’ card output mode to NIM

‘1’ – sets NIM/TTL daughter ‘x’ card output mode to TTL