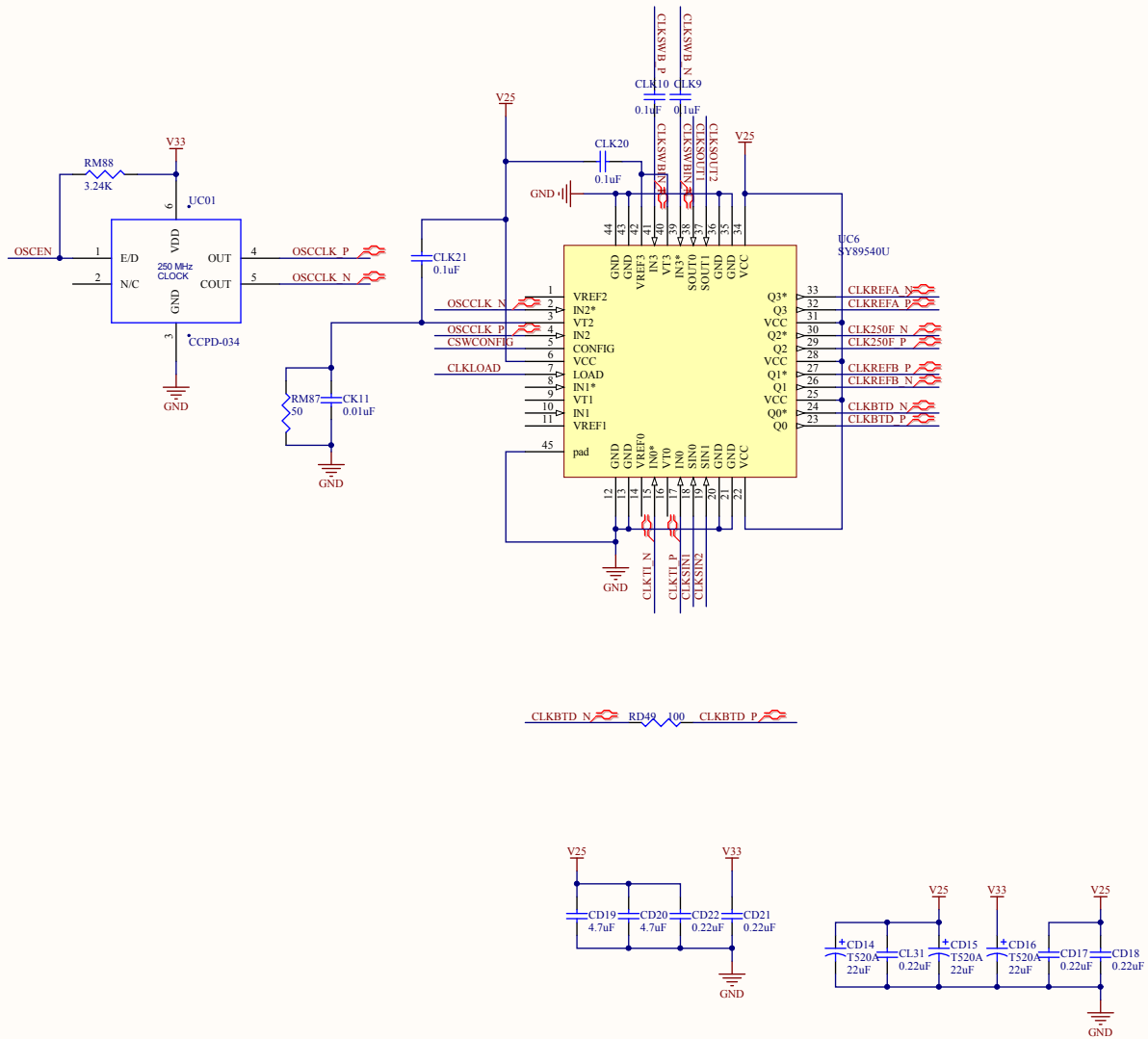
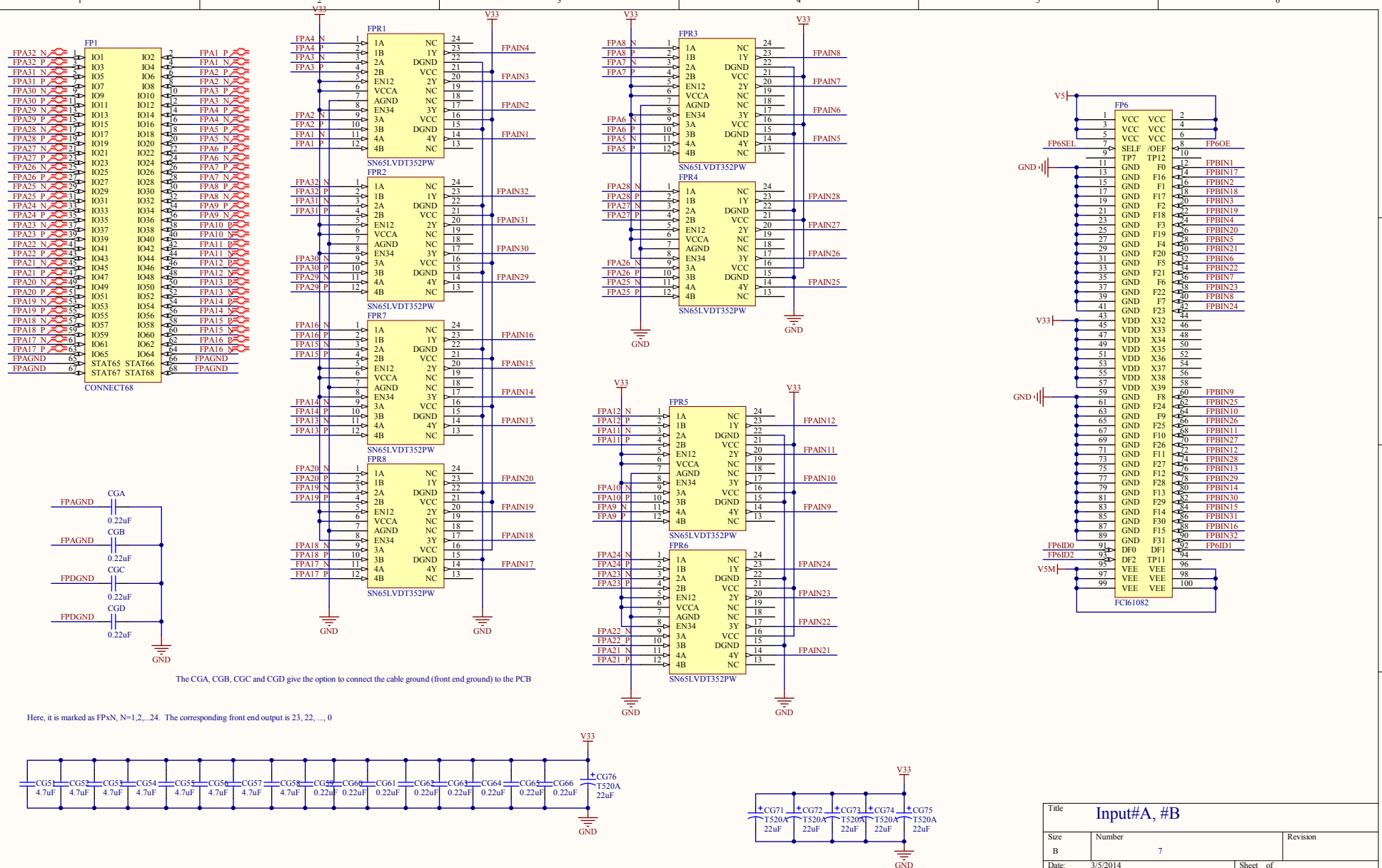
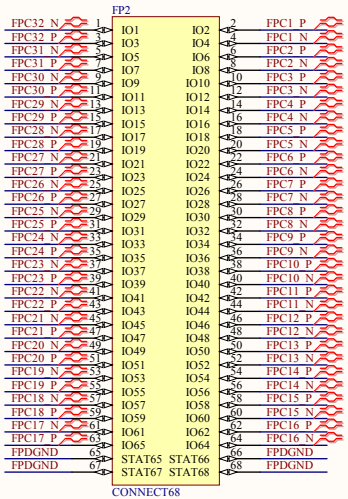
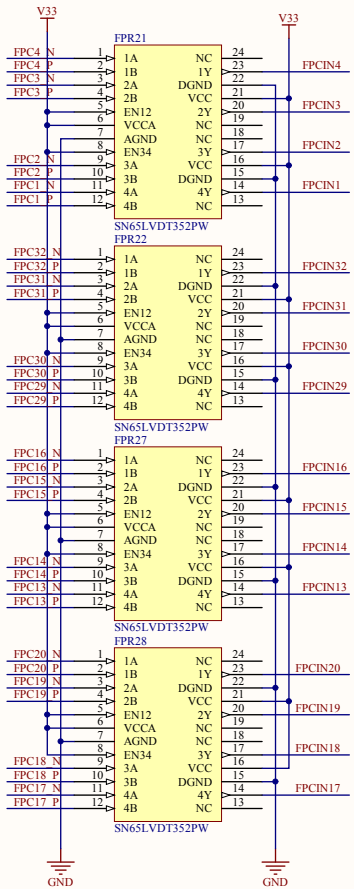


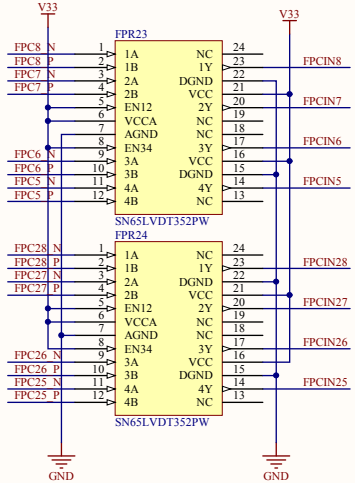
Title	Clock Distribution
Size	B
Number	18
Revision	
Date:	3/5/2014
Sheet	of
File:	C:\pcb\VETROC\ClockDistr.SchDoc
Drawn By:	GU

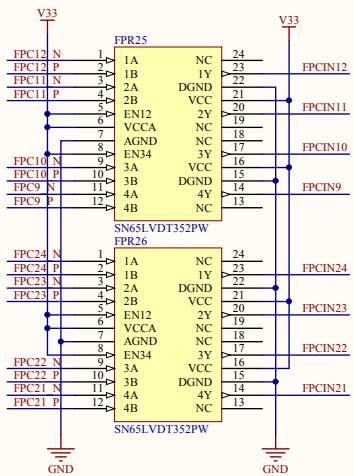


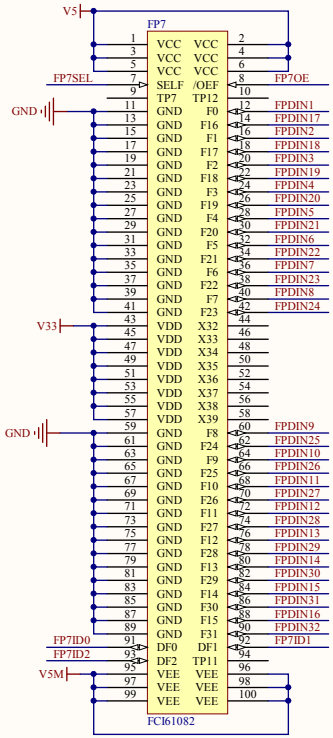
Title	Input#A, #B		
Size	Number		Revision
B	7		
Date:	3/5/2014	Sheet of	
File:	C:\pcb\VETROC\FPinA.SchDoc	Drawn By:	GU



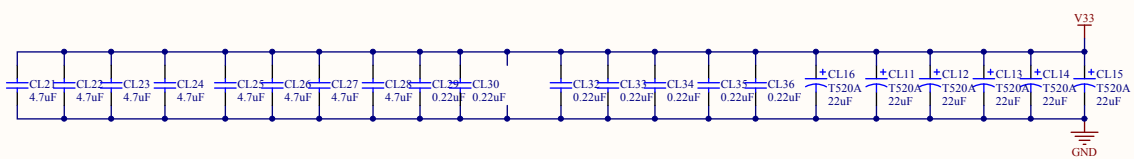




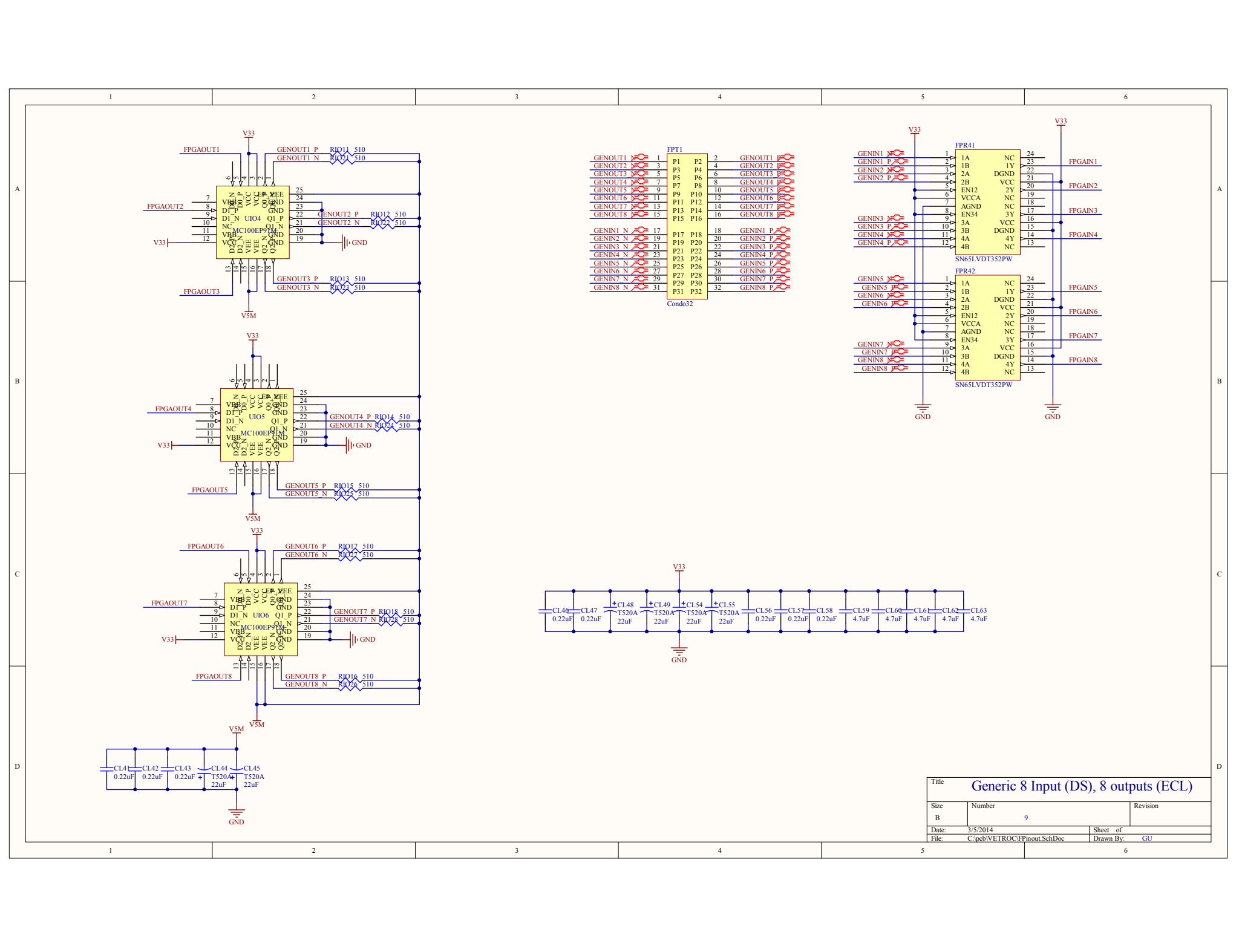




Here, it is marked as FPxN, N=1,2,..24. The corresponding front end output is 23, 22, ..., 0

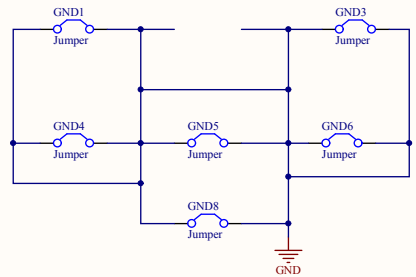


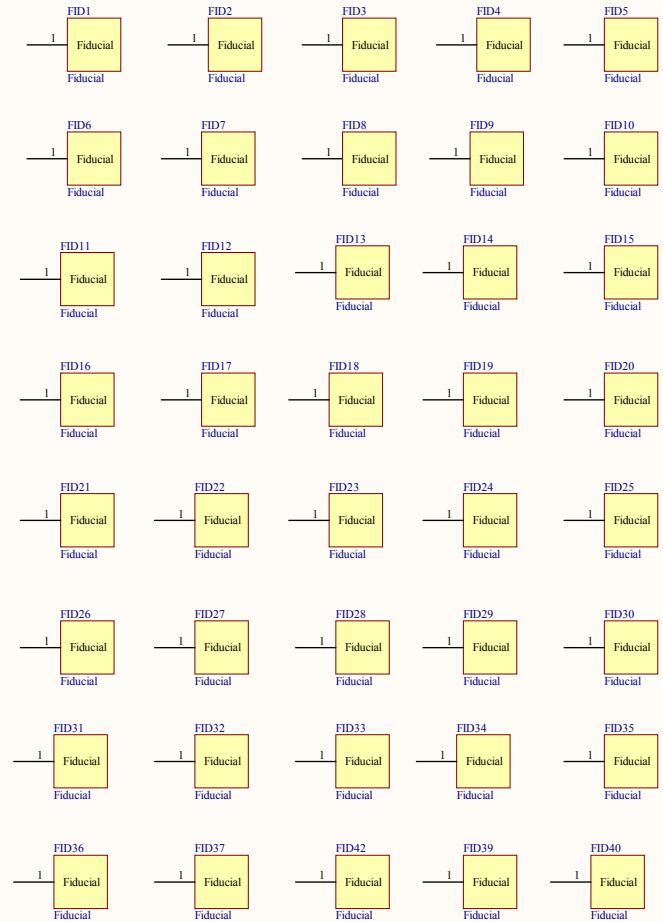
Title	Input#C, #D		
Size: B	Number: 8	Revision:	
Date: 3/5/2014		Sheet of	
File: C:\pcb\VETROC\FPinB.SchDoc		Drawn By: GU	



Title	Generic 8 Input (DS), 8 outputs (ECL)	
Size: B	Number: 9	Revision:
Date: 3/5/2014		Sheet of
File: C:\pcb\VETROC\FPinout.SchDoc		Drawn By: GU

Ground posts





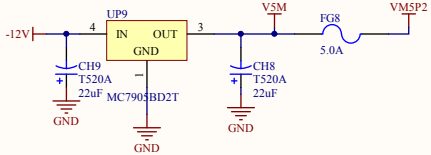
Title: Alignment points and ground points		
Size: B	Number: 19	Revision:
Date: 3/5/2014		Sheet of
File: C:\pcb\VETROC\GndMark.SchDoc		Drawn By: GU

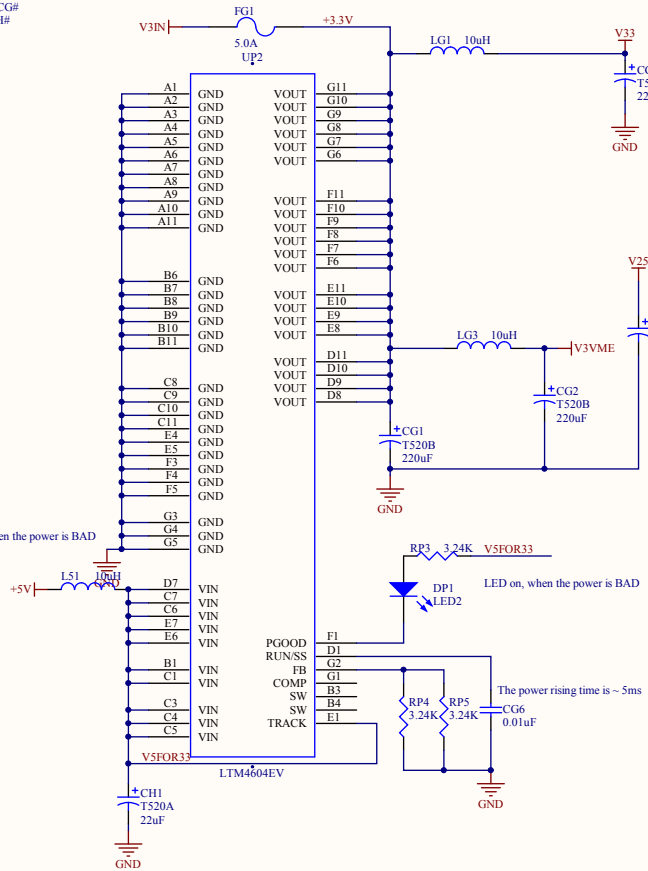
This page: RP# (Resistor for Power Supplies)

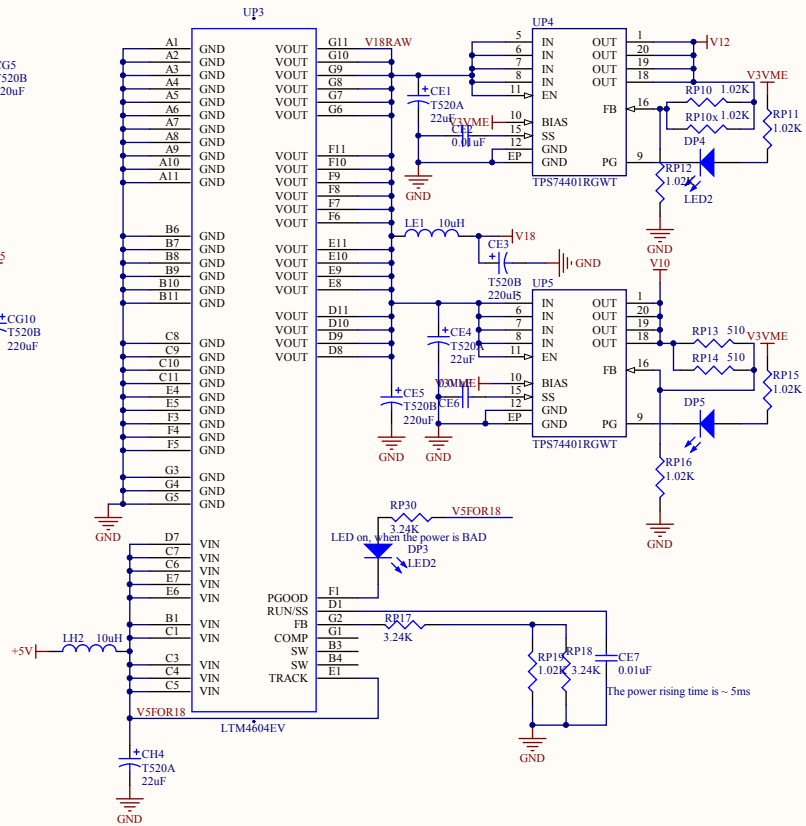
RT#: input termination resistors
RD#, RE#: Pull-down resistors for LVPECL drivers
RB#: backplane (esp. VME) resistors
RC#: resistor/capacitor for input selection

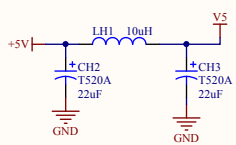
-5V: CA#
+1.0V: CB#
+1.2V: CC#
+3.3V: CD#
Others: CK#

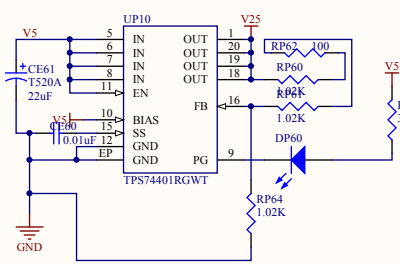
+1.8V: CE#
+2.5V: CF#
+3.3V: CG#
+5V: CH#

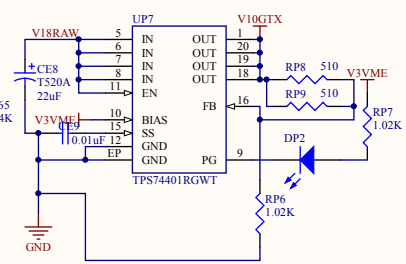










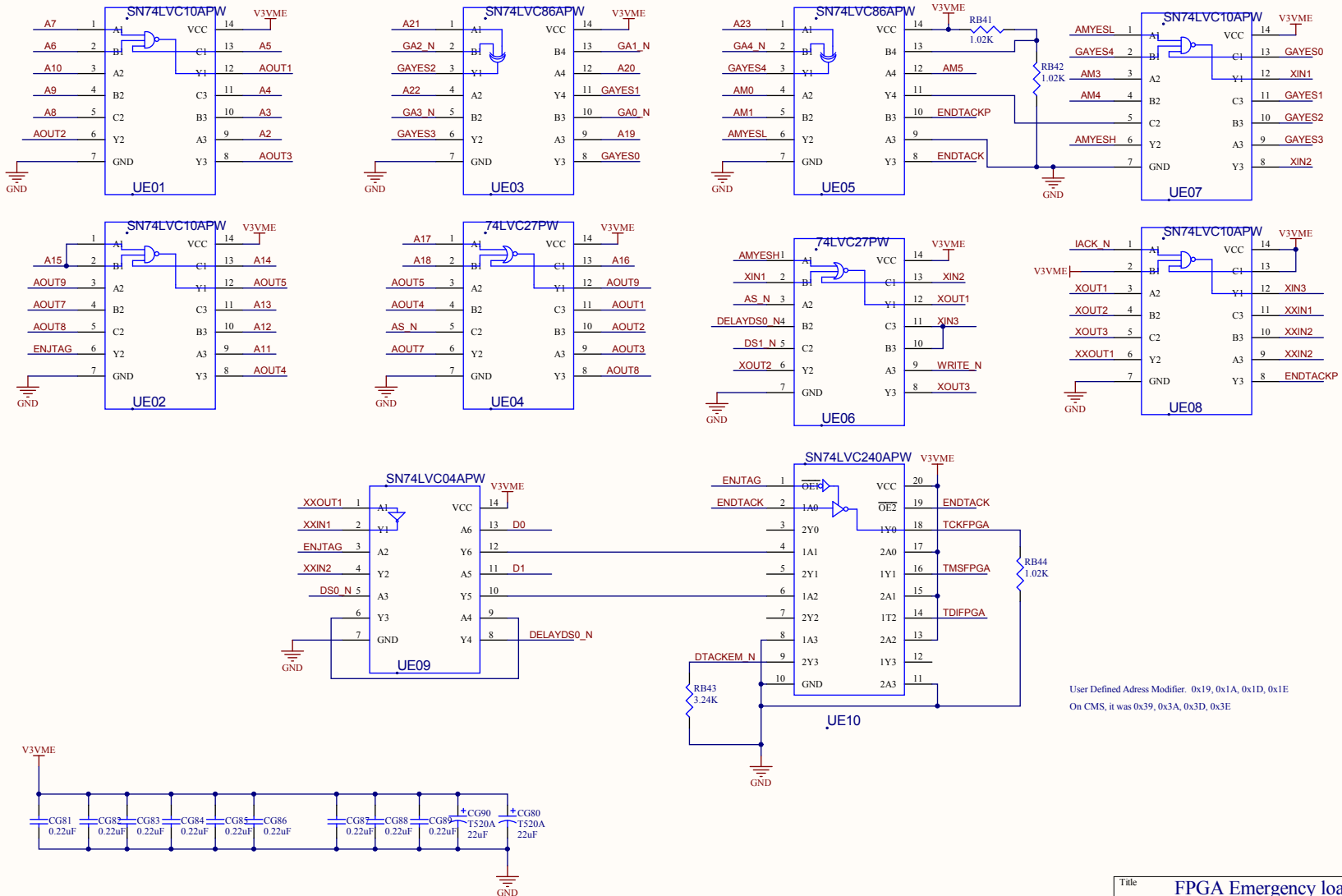


Power on connector: +5VME, +12VME, -12VME, V3IN

Used on board: V5, V33, V3VME, VM5ECL, V25, V25PECL, V18, V12, V10, V10GTX

Title	Power source	
Size: B	Number: 1	Revision:
Date: 3/5/2014	Sheet of	
File: C:\pcb\VETROC\PowerSource.SchDoc	Drawn By: GU	

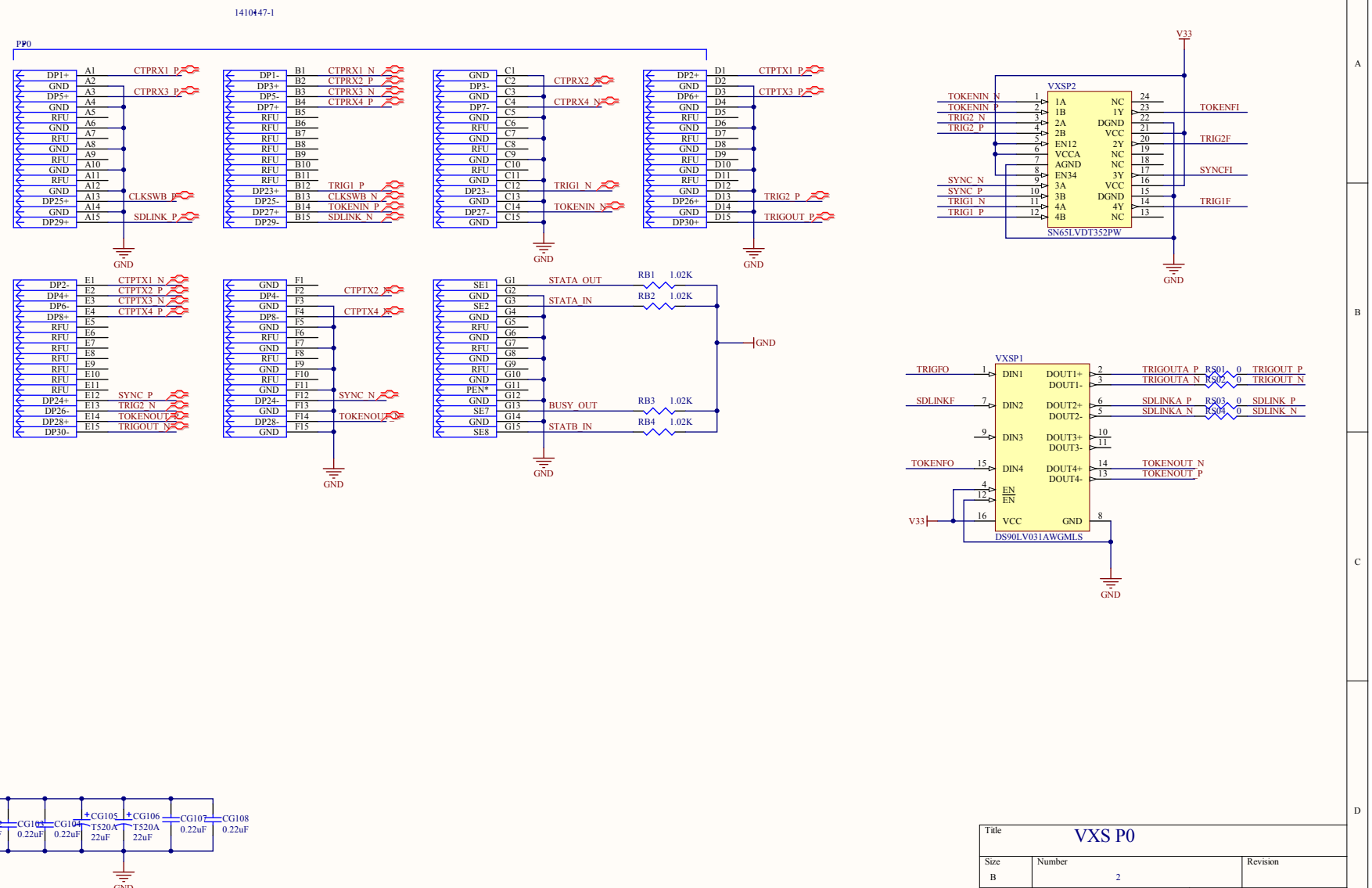
Discrete logic to load the VPROM in emergency



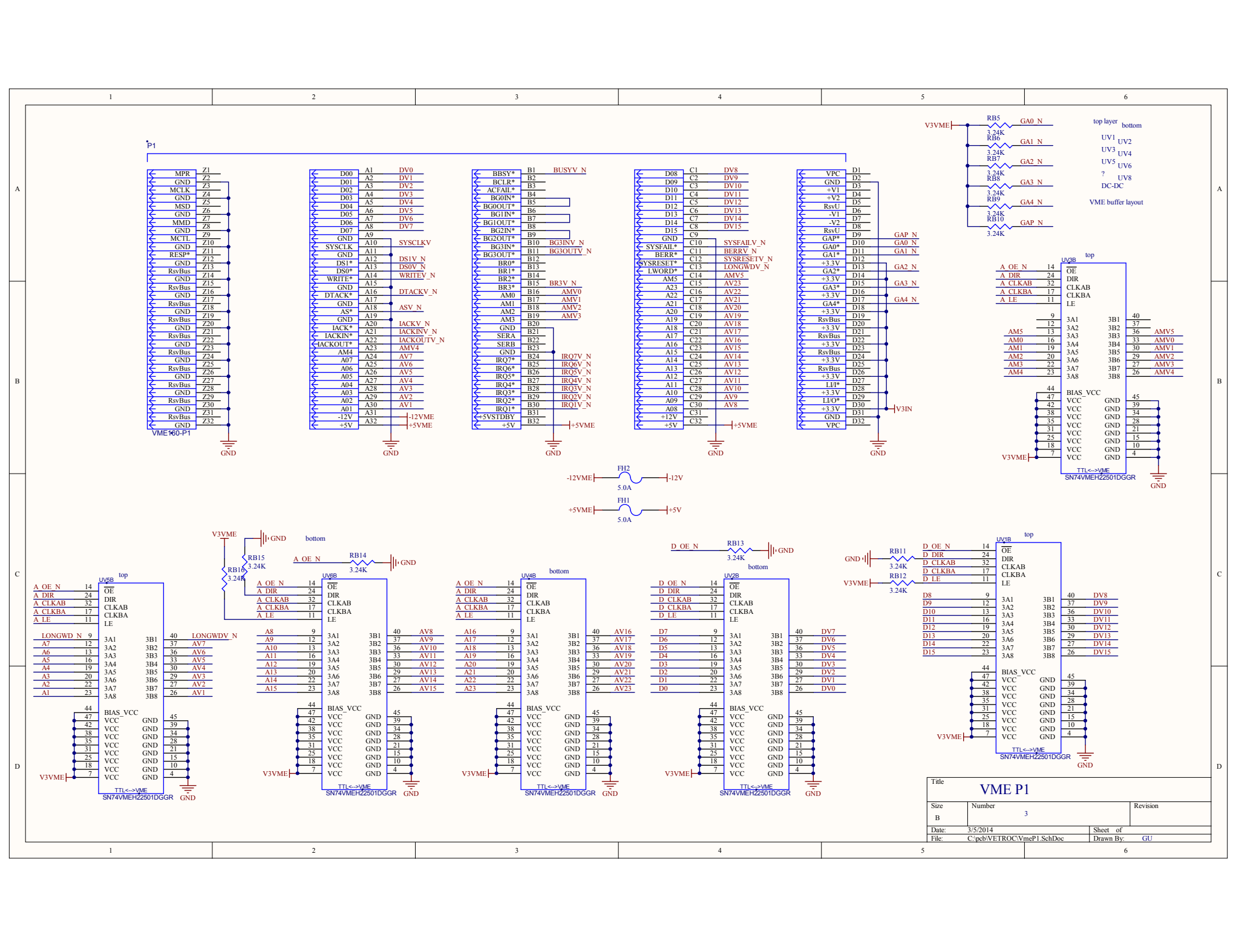
User Defined Adress Modifier. 0x19, 0x1A, 0x1D, 0x1E

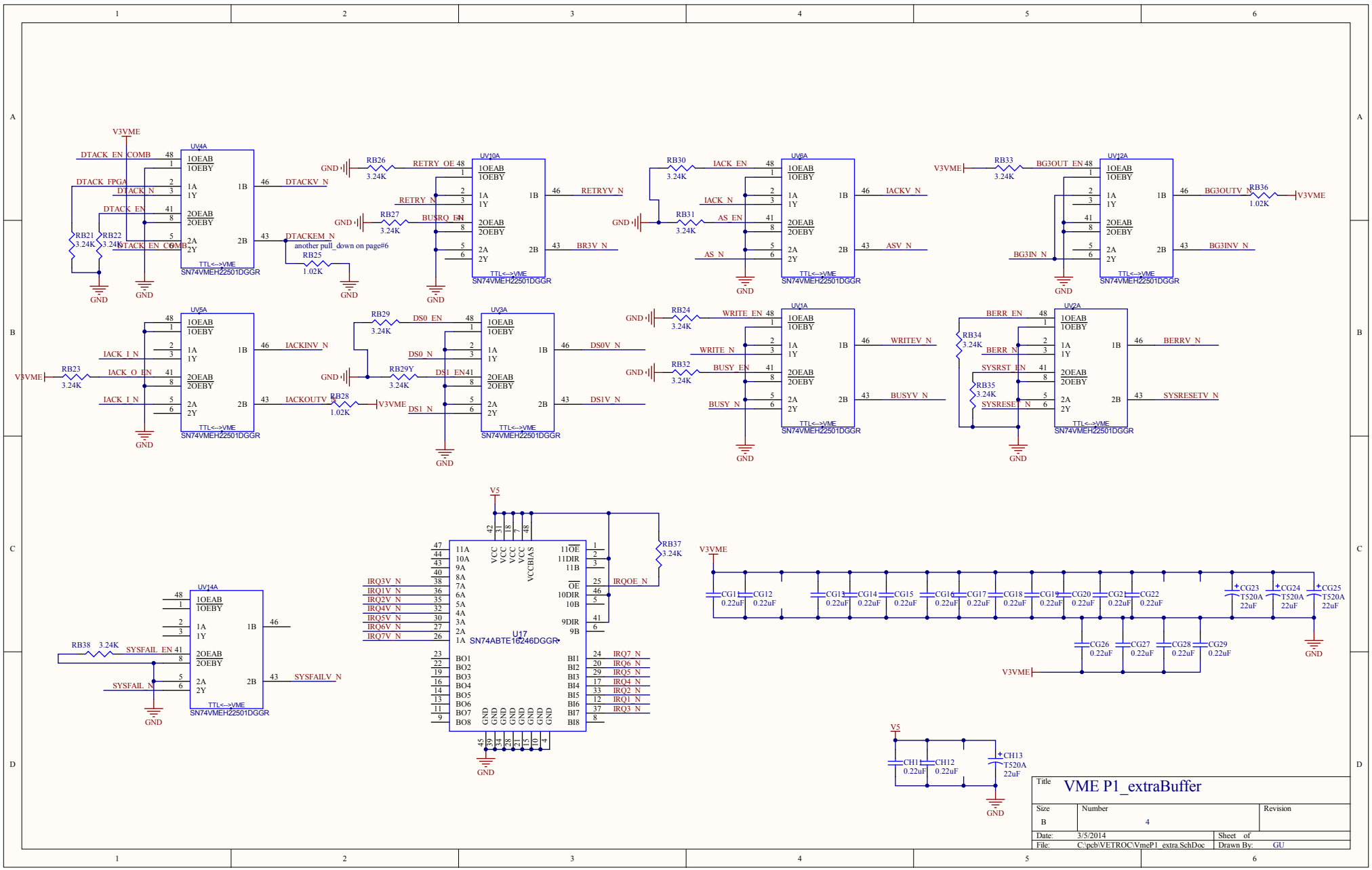
On CMS, it was 0x39, 0x3A, 0x3D, 0x3E

Title	FPGA Emergency loading	
Size: B	Number: 6	Revision:
Date: 3/5/2014	Sheet of	
File: C:\pcb\VETROC\VMEemergency.SchDoc	Drawn By: GU	

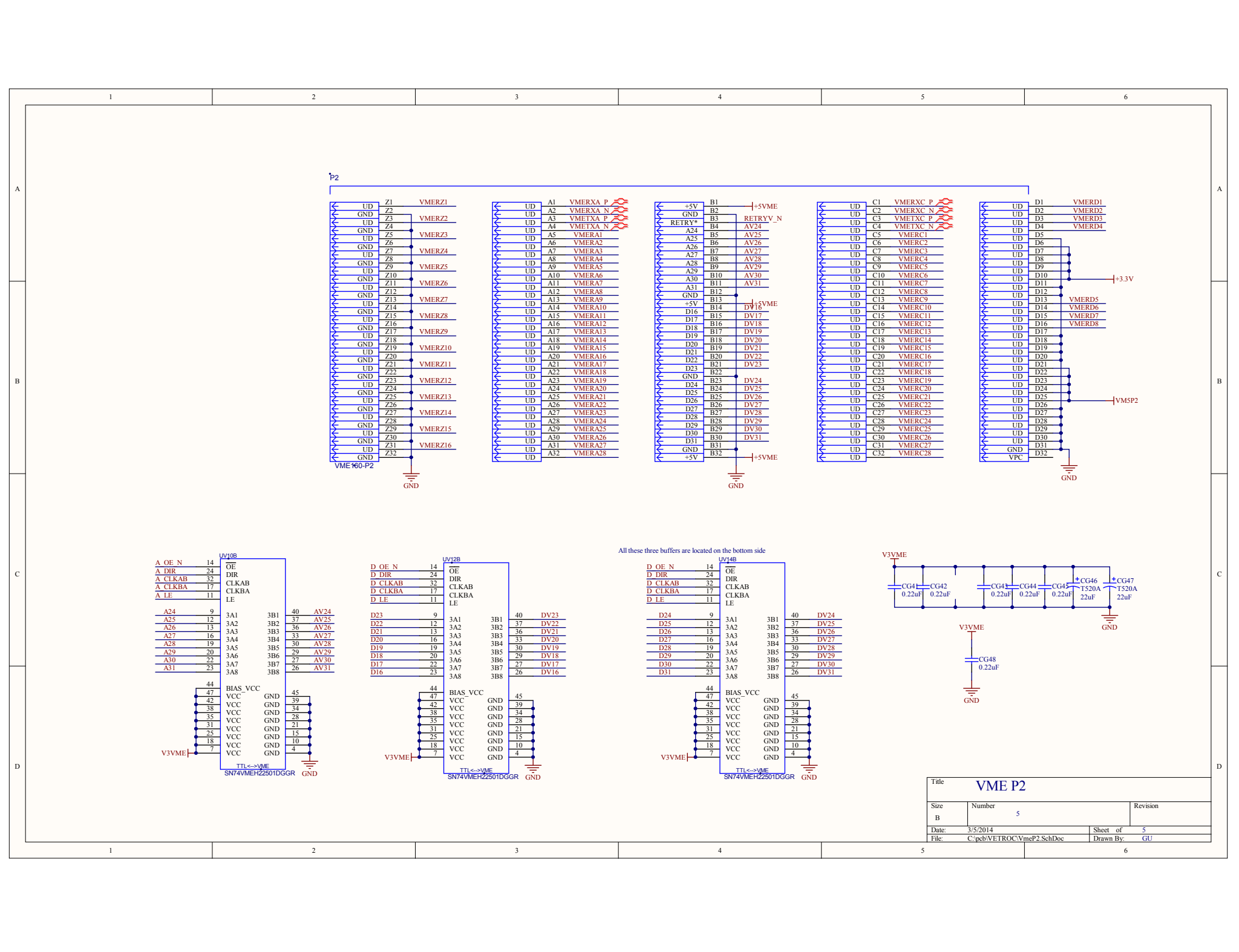


Title	VXS P0		
Size: B	Number: 2	Revision:	
Date: 3/5/2014		Sheet of	
File: C:\pcb\VETROC\VmeP0.SchDoc		Drawn By: GU	

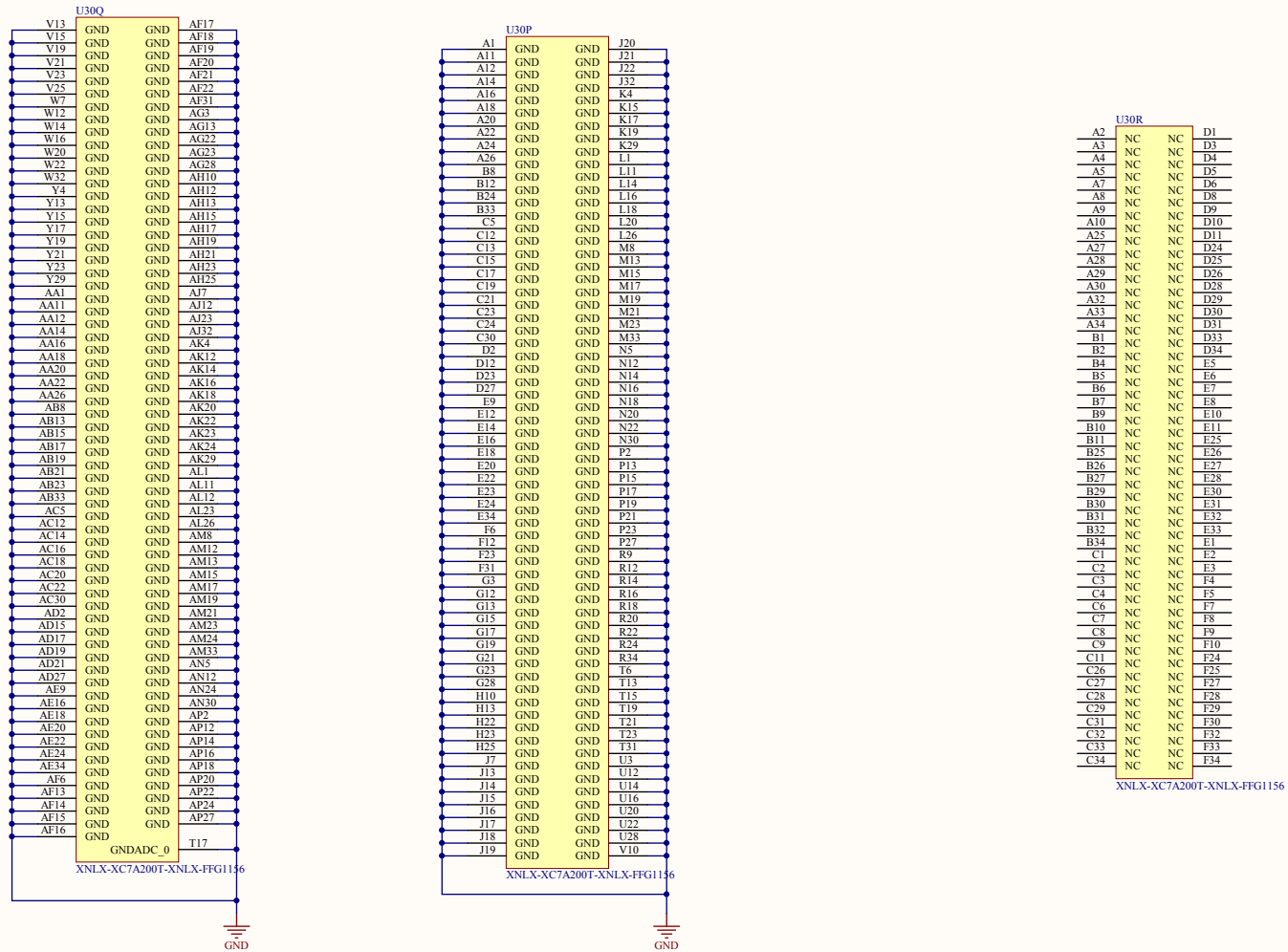

P1
VME160-P1
MPR GND MCLK GND MSD GND MMD GND MCTL GND RESP* GND RsvBus GND RsvBus GND RsvBus GND RsvBus GND RsvBus GND RsvBus GND RsvBus GND
Z1 Z2 Z3 Z4 Z5 Z6 Z7 Z8 Z9 Z10 Z11 Z12 Z13 Z14 Z15 Z16 Z17 Z18 Z19 Z20 Z21 Z22 Z23 Z24 Z25 Z26 Z27 Z28 Z29 Z30 Z31 Z32
D00 D01 D02 D03 D04 D05 D06 D07 GND SYSCLK GND DS1* DS0* WRITE* GND DTACK* GND AS* GND IACK* IACKIN* IACKOUT* AM4 A07 A06 A05 A04 A03 A02 A01 -12V +5V
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A24 A25 A26 A27 A28 A29 A30 A31 A32
DV0 DV1 DV2 DV3 DV4 DV5 DV6 DV7 SYSCLKV DS1V_N DS0V_N WRITEV_N DTACKV_N ASV_N IACKV_N IACKINV_N IACKOUTV_N AMV4 AV7 AV6 AV5 AV4 AV3 AV2 AV1 -12VME +5VME
BBSY* BCLR* ACFAIL* BG0IN* BG0OUT* BG1IN* BG1OUT* BG2IN* BG2OUT* BG3IN* BG3OUT* BR0* BR1* BR2* BR3* AM0 AM1 AM2 AM3 GND SERA SERB GND IRQ7* IRQ6* IRQ5* IRQ4* IRQ3* IRQ2* IRQ1* -5VSTDBY +5V
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 B21 B22 B23 B24 B25 B26 B27 B28 B29 B30 B31 B32
BUSYV_N BG3INV_N BG3OUTV_N BR3V_N AMV0 AMV1 AMV2 AMV3 IRQ7V_N IRQ6V_N IRQ5V_N IRQ4V_N IRQ3V_N IRQ2V_N IRQ1V_N +5VME
D08 D09 D10 D11 D12 D13 D14 D15 GND SYSFAIL* BERR* SYSRESET* LWORD* AM5 A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A09 A08 +12V +5V
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32
DV8 DV9 DV10 DV11 DV12 DV13 DV14 DV15 SYSFAILV_N BERRV_N SYSRESETV_N LONGWDV_N AMV5 AV23 AV22 AV21 AV20 AV19 AV18 AV17 AV16 AV15 AV14 AV13 AV12 AV11 AV10 AV9 AV8 +5VME
VPC GND +V1 +V2 RsvU -V1 -V2 RsvU GAP* GA0* GA1* +3.3V GA2* +3.3V GA3* +3.3V GA4* +3.3V RsvBus +3.3V RsvBus +3.3V RsvBus +3.3V RsvBus +3.3V LI/I* +3.3V LI/O* +3.3V GND VPC
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 D31 D32
GAP_N GA0_N GA1_N GA2_N GA3_N GA4_N V3IN
GND
V3VME
RB5 RB6 RB7 RB8 RB9 RB10 3.24K
GA0_N GA1_N GA2_N GA3_N GA4_N GAP_N
top layer bottom
UV1 UV2 UV3 UV4 UV5 UV6 ? UV8 DC-DC
VME buffer layout
UV3B top
A_OE_N A_DIR A_CLKAB A_CLKBA A_LE
OE DIR CLKAB CLKBA LE
AM5 AM0 AM1 AM2 AM3 AM4
AMV5 AMV0 AMV1 AMV2 AMV3 AMV4
BIAS_VCC VCC GND
TTL<->VME SN74VMEH22501DGGR
FH2 -12VME -12V 5.0A
FH1 +5VME +5V 5.0A
V3VME GND RB15 RB16 3.24K RB14 A_OE_N
UV5B top
UV6B bottom
UV4B bottom
UV2B bottom
LONGWD_N A7 A6 A5 A4 A3 A2 A1
LONGWDV_N AV7 AV6 AV5 AV4 AV3 AV2 AV1
A8 A9 A10 A11 A12 A13 A14 A15
AV8 AV9 AV10 AV11 AV12 AV13 AV14 AV15
A16 A17 A18 A19 A20 A21 A22 A23
AV16 AV17 AV18 AV19 AV20 AV21 AV22 AV23
D_OE_N D_DIR D_CLKAB D_CLKBA D_LE
D7 D6 D5 D4 D3 D2 D1 D0
DV7 DV6 DV5 DV4 DV3 DV2 DV1 DV0
RB13 RB11 RB12
UV1B top
D8 D9 D10 D11 D12 D13 D14 D15
DV8 DV9 DV10 DV11 DV12 DV13 DV14 DV15
Title
VME P1
Size B
Number 3
Revision
Date: 3/5/2014
Sheet of
File: C:\pcb\VETROC\VmeP1.SchDoc
Drawn By: GU



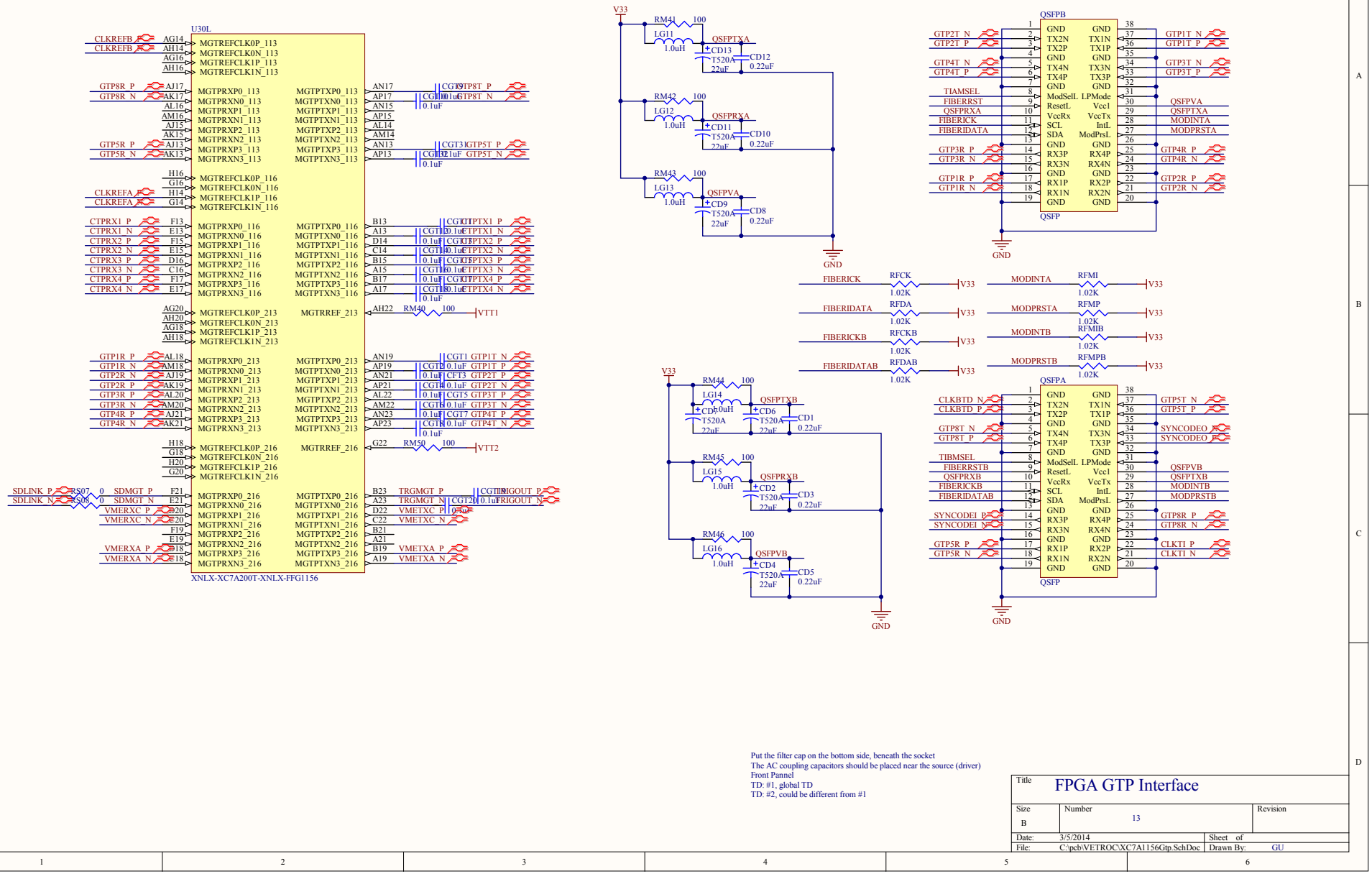
Title	VME P1_extraBuffer
Size	B
Number	4
Revision	
Date:	3/5/2014
Sheet	of
File:	C:\pcb\VETROC\VmeP1_extra.SchDoc
Drawn By:	GU



Title	VME P2	
Size: B	Number: 5	Revision:
Date: 3/5/2014		Sheet of 5
File: C:\pcb\VETROC\VmeP2.SchDoc		Drawn By: GU

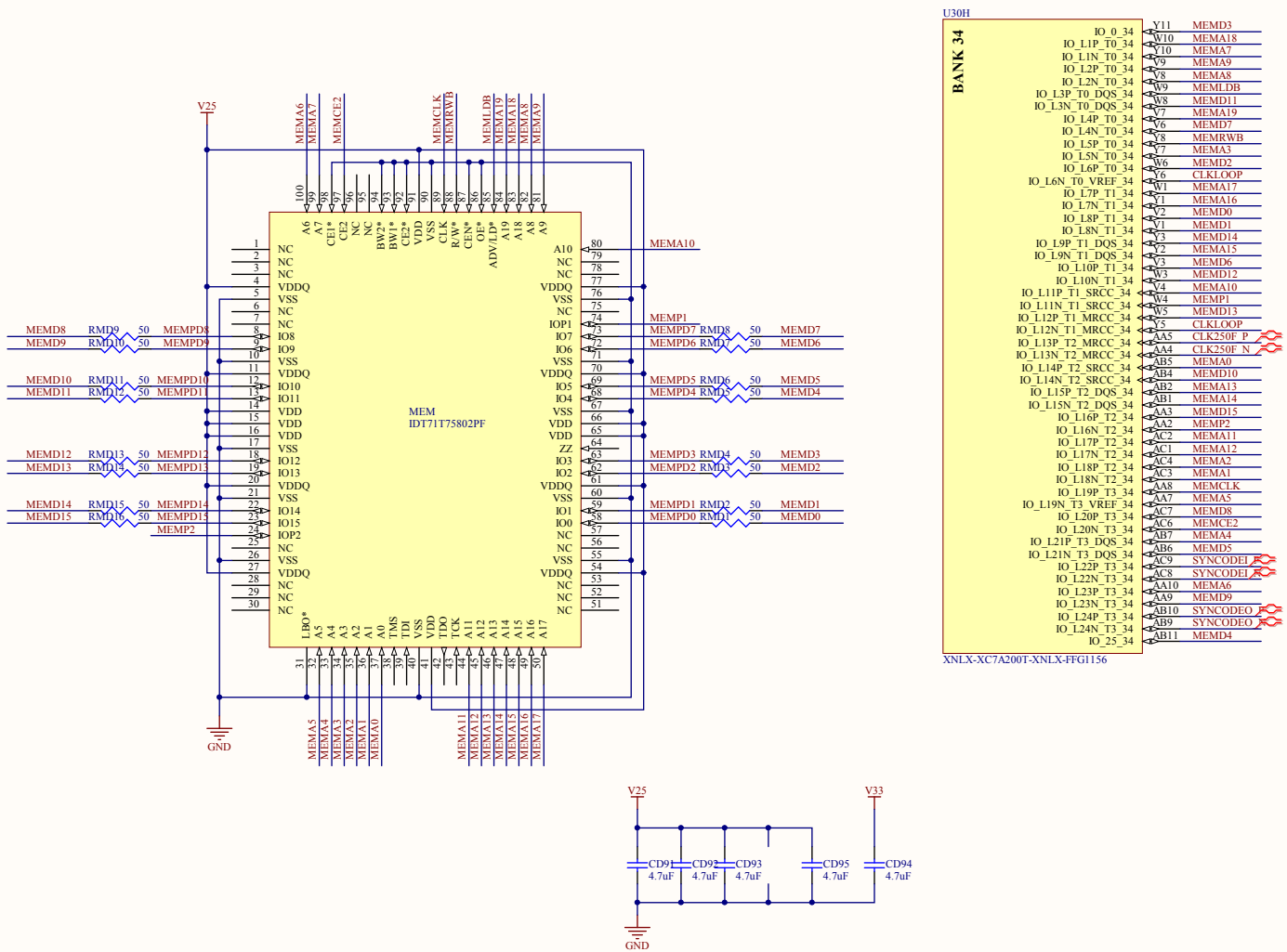


Title	FPGA Ground		
Size: B	Number: 10		Revision:
Date: 3/5/2014		Sheet of	
File: C:\pcb\VETROC\XC7A1156Gnd.SchDoc		Drawn By: GU	


U30L
MGTREFCLK0P_113
MGTREFCLK0N_113
MGTREFCLK1P_113
MGTREFCLK1N_113
MGTPRXP0_113
MGTPRXN0_113
MGTPRXP1_113
MGTPRXN1_113
MGTPRXP2_113
MGTPRXN2_113
MGTPRXP3_113
MGTPRXN3_113
MGTPTXP0_113
MGTPTXN0_113
MGTPTXP1_113
MGTPTXN1_113
MGTPTXP2_113
MGTPTXN2_113
MGTPTXP3_113
MGTPTXN3_113
MGTREFCLK0P_116
MGTREFCLK0N_116
MGTREFCLK1P_116
MGTREFCLK1N_116
MGTPRXP0_116
MGTPRXN0_116
MGTPRXP1_116
MGTPRXN1_116
MGTPRXP2_116
MGTPRXN2_116
MGTPRXP3_116
MGTPRXN3_116
MGTPTXP0_116
MGTPTXN0_116
MGTPTXP1_116
MGTPTXN1_116
MGTPTXP2_116
MGTPTXN2_116
MGTPTXP3_116
MGTPTXN3_116
MGTREFCLK0P_213
MGTREFCLK0N_213
MGTREFCLK1P_213
MGTREFCLK1N_213
MGTRREF_213
MGTPRXP0_213
MGTPRXN0_213
MGTPRXP1_213
MGTPRXN1_213
MGTPRXP2_213
MGTPRXN2_213
MGTPRXP3_213
MGTPRXN3_213
MGTPTXP0_213
MGTPTXN0_213
MGTPTXP1_213
MGTPTXN1_213
MGTPTXP2_213
MGTPTXN2_213
MGTPTXP3_213
MGTPTXN3_213
MGTREFCLK0P_216
MGTREFCLK0N_216
MGTREFCLK1P_216
MGTREFCLK1N_216
MGTRREF_216
MGTPRXP0_216
MGTPRXN0_216
MGTPRXP1_216
MGTPRXN1_216
MGTPRXP2_216
MGTPRXN2_216
MGTPRXP3_216
MGTPRXN3_216
MGTPTXP0_216
MGTPTXN0_216
MGTPTXP1_216
MGTPTXN1_216
MGTPTXP2_216
MGTPTXN2_216
MGTPTXP3_216
MGTPTXN3_216
XNLX-XC7A200T-XNLX-FFG1156
V33
RM41 100
LG11 1.0uH
QSFPTXA
CD13 T520A 22uF
CD12 0.22uF
RM42 100
LG12 1.0uH
QSFPRXA
CD11 T520A 22uF
CD10 0.22uF
RM43 100
LG13 1.0uH
QSFPVA
CD9 T520A 22uF
CD8 0.22uF
GND
QSFPB
GND
TX2N
TX2P
GND
TX4N
TX4P
GND
ModSelL
ResetL
VccRx
SCL
SDA
GND
RX3P
RX3N
GND
RX1P
RX1N
GND
TX1N
TX1P
GND
TX3N
TX3P
GND
LPMode
Vcc1
VccTx
IntL
ModPrsL
GND
RX4P
RX4N
GND
RX2P
RX2N
GND
QSFP
FIBERICK
FIBERIDATA
FIBERICKB
FIBERIDATAB
RFCK 1.02K
RFDA 1.02K
RFCKB 1.02K
RFDAB 1.02K
MODINTA
MODPRSTA
MODINTB
MODPRSTB
RFMI 1.02K
RFMP 1.02K
RFMIB 1.02K
RFMPB 1.02K
QSFPTXB
QSFPRXB
QSFPVB
QSFPA
TIAMSEL
TIBMSEL
SYNCODEO
SYNCODEI
Put the filter cap on the bottom side, beneath the socket
The AC coupling capacitors should be placed near the source (driver)
Front Pannel
TD: #1, global TD
TD: #2, could be different from #1
Title
FPGA GTP Interface
Size
B
Number
13
Revision
Date: 3/5/2014
Sheet of
File: C:\pcb\VETROC\XC7A1156Gtp.SchDoc
Drawn By: GU

Title	FPGA #A #B inputs and generic inputs	
Size: B	Number: 15	Revision:
Date: 3/5/2014	Sheet of	
File: C:\pcb\VETROC\XC7A1156InAB.SchDoc	Drawn By: GU	

Title	FPGA #C #D inputs, and generic outputs		
Size: B	Number: 16		Revision:
Date: 3/5/2014		Sheet of	
File: C:\pcb\VETROC\XC7A1156InCD.SchDoc		Drawn By: GU	

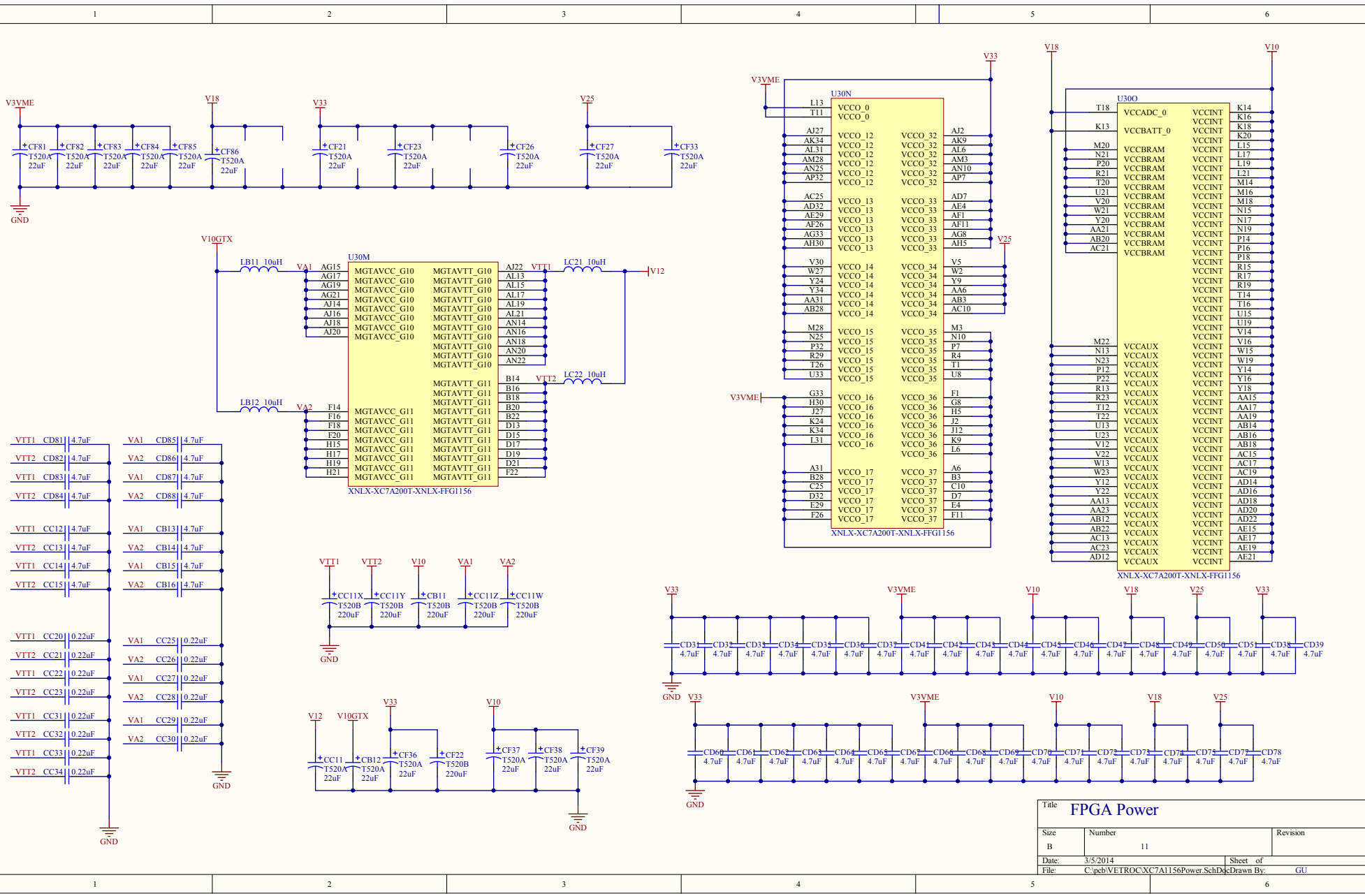


Title: FPGA LVDS input/output bank, including clock

Size	Number	Revision
B	17	

Date: 3/5/2014 Sheet of

File: C:\pcb\VETROC\XC7A1156InOut.SchDoc Drawn By: GU


V3VME
V18
V33
V25
GND
CF81 T520A 22uF
CF82 T520A 22uF
CF83 T520A 22uF
CF84 T520A 22uF
CF85 T520A 22uF
CF86 T520A 22uF
CF21 T520A 22uF
CF23 T520A 22uF
CF26 T520A 22uF
CF27 T520A 22uF
CF33 T520A 22uF
V10GTX
V12
LB11 10uH
LB12 10uH
LC21 10uH
LC22 10uH
VA1
VA2
VTT1
VTT2
U30M
XNLX-XC7A200T-XNLX-FFG1156
U30N
U30O
V10
CD81 4.7uF
CD82 4.7uF
CD83 4.7uF
CD84 4.7uF
CD85 4.7uF
CD86 4.7uF
CD87 4.7uF
CD88 4.7uF
CB13 4.7uF
CB14 4.7uF
CB15 4.7uF
CB16 4.7uF
CC12 4.7uF
CC13 4.7uF
CC14 4.7uF
CC15 4.7uF
CC20 0.22uF
CC21 0.22uF
CC22 0.22uF
CC23 0.22uF
CC25 0.22uF
CC26 0.22uF
CC27 0.22uF
CC28 0.22uF
CC29 0.22uF
CC30 0.22uF
CC31 0.22uF
CC32 0.22uF
CC33 0.22uF
CC34 0.22uF
CC11X 220uF
CC11Y 220uF
CB11 220uF
CC11Z 220uF
CC11W 220uF
CC11 22uF
CB12 22uF
CF36 22uF
CF22 220uF
CF37 22uF
CF38 22uF
CF39 22uF
CD31 4.7uF
CD32 4.7uF
CD33 4.7uF
CD34 4.7uF
CD35 4.7uF
CD36 4.7uF
CD37 4.7uF
CD41 4.7uF
CD42 4.7uF
CD43 4.7uF
CD44 4.7uF
CD45 4.7uF
CD46 4.7uF
CD47 4.7uF
CD48 4.7uF
CD49 4.7uF
CD50 4.7uF
CD51 4.7uF
CD38 4.7uF
CD39 4.7uF
CD60 4.7uF
CD61 4.7uF
CD62 4.7uF
CD63 4.7uF
CD64 4.7uF
CD65 4.7uF
CD67 4.7uF
CD66 4.7uF
CD68 4.7uF
CD69 4.7uF
CD70 4.7uF
CD71 4.7uF
CD72 4.7uF
CD73 4.7uF
CD74 4.7uF
CD75 4.7uF
CD77 4.7uF
CD78 4.7uF
Title FPGA Power
Size B
Number 11
Revision
Date: 3/5/2014
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Drawn By: GU

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Size: B	Number: 14	Revision:
Date: 3/5/2014	Sheet of	
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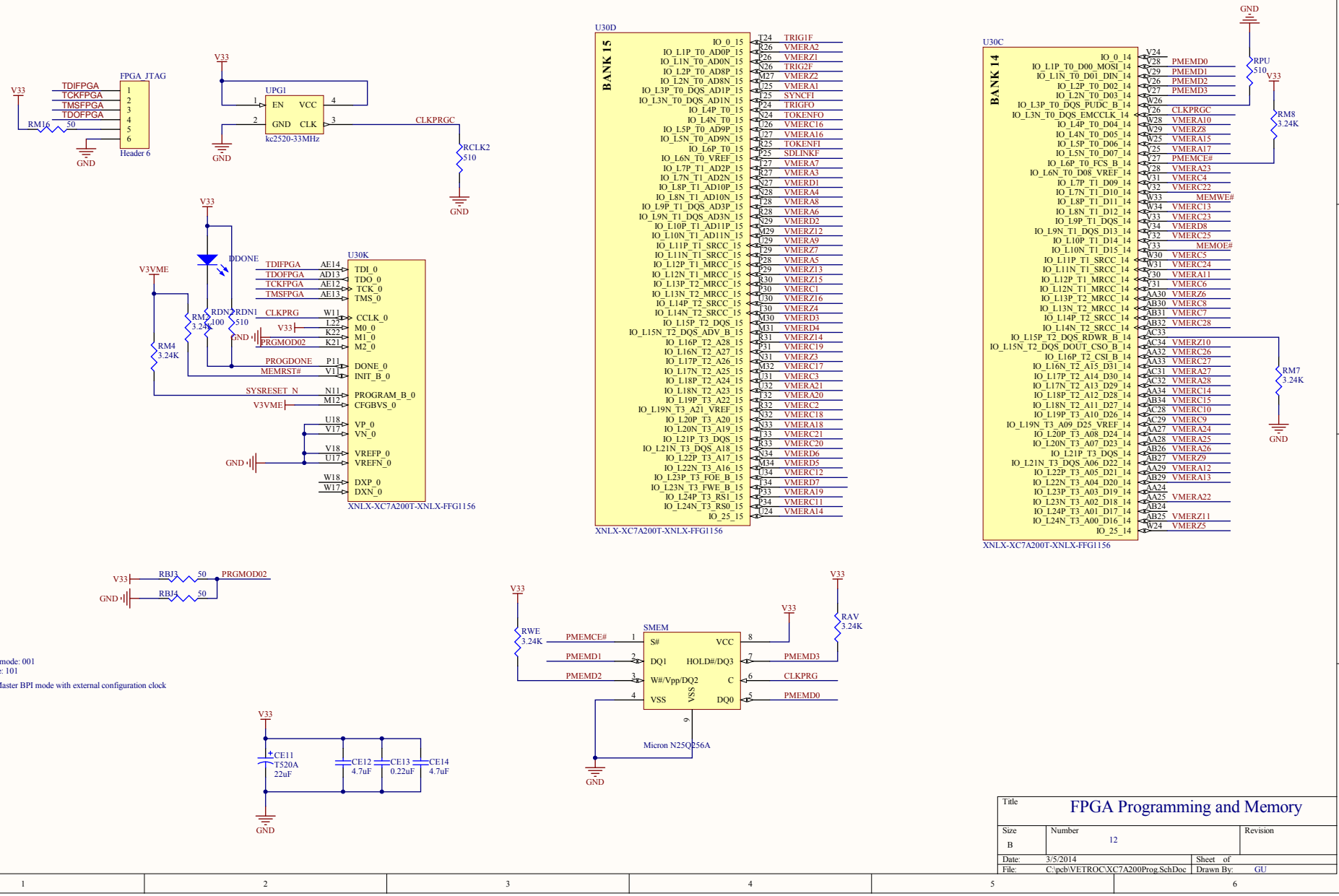
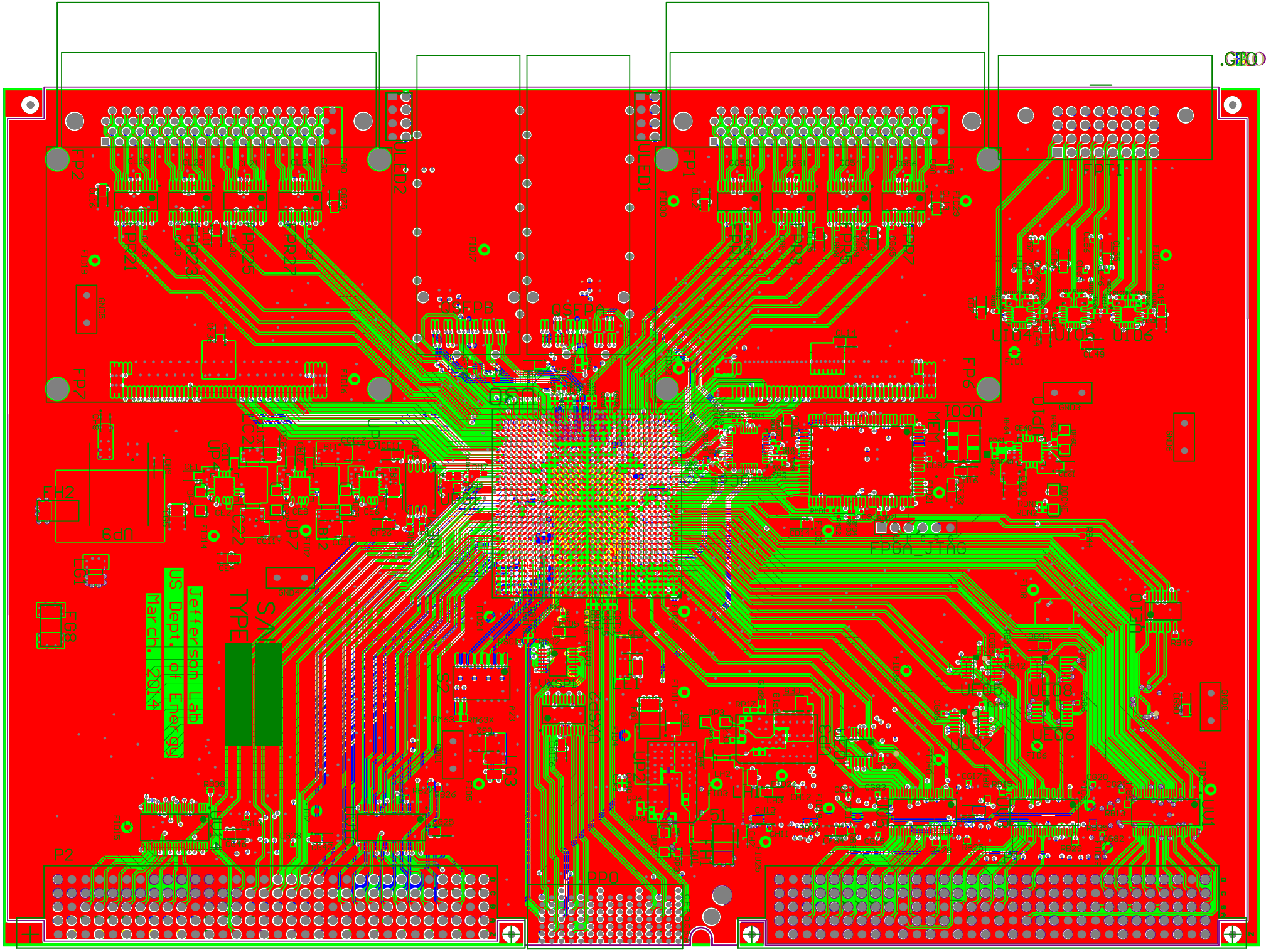

FPGA_JTAG
TDIFPGA
TCKFPGA
TMSFPGA
TDOFPGA
RM16 50
Header 6
UPG1
kc2520-33MHz
CLKPRGC
RCLK2 510
U30K
DONE
RM2 3.24K
RDN2 100
RDN1 510
RM4 3.24K
PROGDONE
MEMRST#
SYSRESET_N
PRGMOD02
XNLX-XC7A200T-XNLX-FFG1156
RBJ3 50
RBJ4 50
Master SPI mode: 001
JTAG mode: 101
FPGA uses Master BPI mode with external configuration clock
CE11 T520A 22uF
CE12 4.7uF
CE13 0.22uF
CE14 4.7uF
U30D
BANK 15
XNLX-XC7A200T-XNLX-FFG1156
U30C
BANK 14
RPU 510
RM8 3.24K
RM7 3.24K
XNLX-XC7A200T-XNLX-FFG1156
RWE 3.24K
SMEM
Micron N25Q256A
RAV 3.24K
Title
FPGA Programming and Memory
Size
B
Number
12
Revision
Date: 3/5/2014
File: C:\pcb\VETROC\XC7A200Prog.SchDoc
Sheet of
Drawn By: GU


Jefferson Lab
US Dept. of Energy
March 2012
SYN
TYPE
FPGA_JTAG
QSFPB
QSFPA
P2
P1