**Compton eTrig Readout – General Comments**

**Section III: Anticipated Data**

**Channel Map:**

Is a ~768x768 matrix map needed/desired? Or is this just a remapping of discriminated signals that are more local?

If mapping is this arbitrary, then essentially no logic can be performed on the individual VXS/VME cards and must be done where all of the detector hits are visible in a single unit (in CTP or SSP). While this is probably doable additional checking would be need to confirm the CTP would have the necessary resources for this massive remapping. You have an existing detector channel-to-cable mapping – will this no longer be used? Having a simple mapping scheme up front makes everything easier in the long run. This general issue would be a good point to discuss in further detail.

**Section IV: Definition of Triggers and Prescaling**

**Trigger Prescalers:**

24bit prescaler per trigger is no problem

**Triggers 1-5:**

No problem in general. The FADC250 has a maximum trigger latency of 8µs (this is the longest time it can wait to receive a trigger after a signal comes into its ADC input before it will lose that data); therefore, C (the coincidence time window parameter) should be constrained to: 0 < C < 8µs in steps of 4ns (~213 steps).

**Section V: Readout and Noise Suppression**

**Time resolution:**

For triggering the time resolution of 32ns (potentially 16ns if CTP has margin) would fit nicely (allows the 4Gbps link from the VXS card to send a 128 channel pattern every 32ns – even though only a 96 channel pattern would be used 32ns is much more convenient than 24ns).

For readout a time resolution of 4ns would be easily doable (and likely down to 1ns possible) – this depends on how the readout data should be formatted.

**Section VI: Additional Logic Input**

**Additional Logic Inputs**

Additional logic inputs will be no problem on the VXS cards. The number will be determined by the available front-panel space. A proposed front-panel layout will indicate an option of what can be done.

**Section VII: Helicity Recording and Onboard Scalers**

**Helicity, T-Settle, Pair Sync**

Recoding this signals shouldn’t be a problem, but further information will be needed to implement the desired functionality.

**Scalers**

5 Scalers – one for each trigger

96 Scalers – one for each channel. Support for triggered event building of these values and tagging with helicity state.

**Proposed Data Structures**

“Time tag”: There will be a global 250MHz clock feeding all VXS modules that is synchronized so they will all count this value together. Each event readout will contain this 250MHz timestamp for all boards and they will provide the same value if they are all synchronized properly.

Data structures: The way the FADC250 (also a new VXS readout board) builds events will force the data structures to look a bit different when they are actually readout of the boards, but they can be reformatted after they are readout to match what you desire. It won’t be any problem to support the “Fixed Data Structure” and “Variable Data Structure”. We should probably discuss this in more detail to make sure we’re all on the same page.

**Section VIII: Compatibility with Previous Detector**

**Reuse Connector 3M 50pin**

Great plan to reuse this format. I would plan to use the dual stacked mate of this on the VXS card side so that 4x 50pin connectors per VXS card will be possible and still have room left for additional I/O (10 to 16 additional I/O differential pairs could be provided on dual stacked headers).

**General Specifications for VETROC (VXS Electron Trigger Read Out Card)**

|  |  |
| --- | --- |
|  | **Form Factor**   * 6U VXS VITA 41 Payload Module   **Front Panel Indicators**   * Power Ok LED * VME DTACK LED * Status/Trigger LED   **Detector Inputs**   * 96 channel LVDS detector inputs * 4x 50pin dual row 0.1” headers (compatible with existing ETROC cables)     **General Purpose Inputs/Output**   * 8x differential ECL inputs (16pin dual row 0.1” spaced header) * 8x differential ECL outputs (16pin dual row 0.1” spaced header)   **High Speed Serial P0 Inputs/Ouptuts**   * 250MHz LVPECL Clock Input * Trig 1, Trig 2, Sync Inputs * Status, Busy Outputs * 4x 2.5-5Gbps Lanes to/from CTP   **Event Builder**   * 2MByte Event Buffer * >>100kHz Trigger Acceptance Rate (@ >99% live time, assuming 100% occupancy or fixed data structure) * >1kHz Scaler Trigger Acceptance Rate (@ >99% live time)   **Readout Interface**   * VME64x backplane interface * 2eSST (200MB/s) transfer rate support * 32bit register access   **Programming**   * Onboard Jtag port * VME firmware update   **Power Requirements**   * +5.0v @ TBD Amps * -12.0v @ TBD Amps |

**General Comments**

**Readout Performance**

1. The trigger rate an individual VETROC module can accept will be very high (in the MHz range)
2. There is no specific limit on the individual strip rate the VETROC can handle (1MHz+ is ok)
3. For this isolated system the general limiting factor of the DAQ system will be the Gigabit Ethernet of the CPU, not the VXS front-end cards or trigger system. This limit is on the order of 115MB/s, but in reality this number should be reduced to perhaps 80MB/s to account for various network traffic delays that may occur.
4. It is expected that the crate will be equipped with a modern Intel based Core i7 CPU or better.

**Scalability**

1. The Jlab VXS based crates can be equipped with up to 16 front-end readout boards. For the Hall A Compton setup 1 slot is given to the FADC and the remaining 15 readout slots would be available to VETROC modules. If each VETROC supports 96 detector channels this system would be scalable to 1,440 channels.

It is likely that further scaling by a factor of 8 is achievable with no loss of trigger performance if a reasonable channel map exists by using an SSP to accept trigger information from 8 crates (though this would take additional firmware development to support).

**Triggers**

1. The VXS TI operating in master mode can support up to 6 inputs. It is my understanding that Hall A is planning to use a TI in master mode as its “TS”, but I did want to point out that the standard VXS TS would support 32+ trigger inputs that may be of interest.

The CTP basically has no support for event-by-event readout data. If you have multiple trigger sources enabled you likely will want to have the type as part of the event data. In this case the CTP could send 5 trigger bits to the TS. Then the TS will record this pattern (trigger type and input state) as part of the event when the system is triggered. It also seems to me that the helicity flip and possibly related bits would be a nice fit to go into the TS. As you add these up you can quickly use up the few (6) trigger inputs on a TI acting like the TS. Perhaps it will be worthwhile to plan on investing in a TS (perhaps not if this is really a standalone DAQ)?

1. The “strip matching” logic timing coincidence is expected to be formed by generating a digital pulse width equal to the coincidence time for each strip each time the strip channel sees a logic ‘0’->’1’ transition.

**Readout Data**

1. When the VETROC receives a readout trigger, it will use the programmable width digital pulse outputs from each strip (the same one used to form time coincidence for the trigger logic) and capture this pattern to form the event data structure (this is important to keep the trigger decision consistent with the readout data). It would be possible to have the VETROC act like a TDC for the readout data and report an accurate time measurement (in the neighborhood of 1 to 4ns resolution) which could be advantageous for offline analysis in removing noise hits. This would certainly be more information to readout, but maybe worth it.

**VETROC Assembly Pricing Estimates**

The following pricing is reasonably conservative and is expected to be an upper limit and also give some wiggle room for various component selections.

**Components (QTY per component, Ext Cost for 10 boards):**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Part Number** | **QTY** | **Description** | **Cost** | **Ext. Cost** | **Note** |
| 3433-D302 | 2 | Dual Stacked 50pin Headers | $18.61 | $1860.35 | Min. 100 |
| PCB | 1 | Multilayer VXS PCB | $600.00 | $6000.00 |  |
| Front Panel | 1 | VXS Machined/Silkscreen Panel | $100.00 | $1000.00 |  |
| FPGA | 1 | Xilinx Spartan 6 or Kintex 7 | $250.00 | $2500.00 |  |
| VXS-P0 | 1 | VITA 41 VXS Plug | $83.00 | $830.00 |  |
| VXS-KEY | 1 | VITA 41 VXS Key | $30.00 | $300.00 |  |
| MISC POWER | 1 | Misc Power supply components | $50.00 | $500.00 |  |
| MISC CON | 1 | Misc connectors | $50.00 | $500.00 |  |
| MISC IC | 1 | Misc chips/buffers/passives | $200.00 | $2000.00 |  |
| ASSEMBLY | 1 | PCB Assembly/NRE | $600.00 | $6000.00 |  |

**Prototyping 1 Board Cost:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Part Number** | **QTY** | **Description** | **Cost** | **Ext. Cost** | **Note** |
| 3433-D302 | 2 | Dual Stacked 50pin Headers | $18.61 | $1860.35 | Min. 100 |
| PCB | 1 | Multilayer VXS PCB | $2000.00 | $2000.00 |  |
| FPGA | 1 | Spartan 6/Kintex 7 | $250.00 | $250.00 |  |
| VXS-P0 | 1 | VITA 41 VXS Plug | $83.00 | $83.00 |  |
| VXS-KEY | 1 | VITA 41 VXS Key | $30.00 | $30.00 |  |
| MISC POWER | 1 | Misc Power supply components | $100.00 | $100.00 |  |
| MISC CON | 1 | Misc connectors | $100.00 | $100.00 |  |
| MISC IC | 1 | Misc chips/buffers/passives | $400.00 | $400.00 |  |
| ASSEMBLY | 1 | PCB Assembly/NRE | $2000.00 | $2000.00 |  |

**Material Costs for 1 Prototype + 10 Production Boards**

Prototype: $6823.35

Production: $19,630

**Total: $26453.35**

**VETROC Development Schedule**

**Prototype Schematics/PCB Design**

Schematic: 2 weeks

PCB Layout: 2 weeks

* Schematic/PCB design time would be spread of several weeks due to interleaving projects…
* Prototype turn-around time would depend on potential long-lead components, but probably could be around 4-6 weeks.

**Prototype Firmware Design**

VETROC Firmware: 4 weeks

CTP Firmware: 4 weeks

* Firmware development time would be spread of several weeks due to interleaving projects…
* There is a significant degree of uncertainty here based on potential bugs and feature requests that develop

**Production Schematics/PCB Design**

Schematic+ PCB Layout: 1 week

* Time reserved to fix prototype issues before small production run

**Production Firmware Design**

Firmware: 1 week

* Time reserved to fix prototype issues for production modules