Verilog Club - Assignment 3

This assignment involves building a state machine that implements a traffic light controller. This is a “dumb” state machine. It doesn’t handle left turns, it only handles north-south and east-west traffic flow control. It doesn’t handle inputs from buried sensors that detect if vehicles are present.

It does however, have strict requirements on the timing of the light on and off times.

As you can see from the timing diagram, 7 states are defined. The states are:

SAFE	In this state both directions are red. This state provides time for the intersection to clear of traffic and those pesky drivers that like to “run” red lights just after turning red from yellow.
NS_GREEN	In this state, the north-south lights are green
NS_YELLOW	In this state, the north-south lights are yellow
NS_RED	In this state, the north-south lights are red
EW_GREEN	In this state, the east-west lights are green
EW_YELLOW	In this state, the east-west lights are yellow
EW_RED	In this state, the east-west lights are red

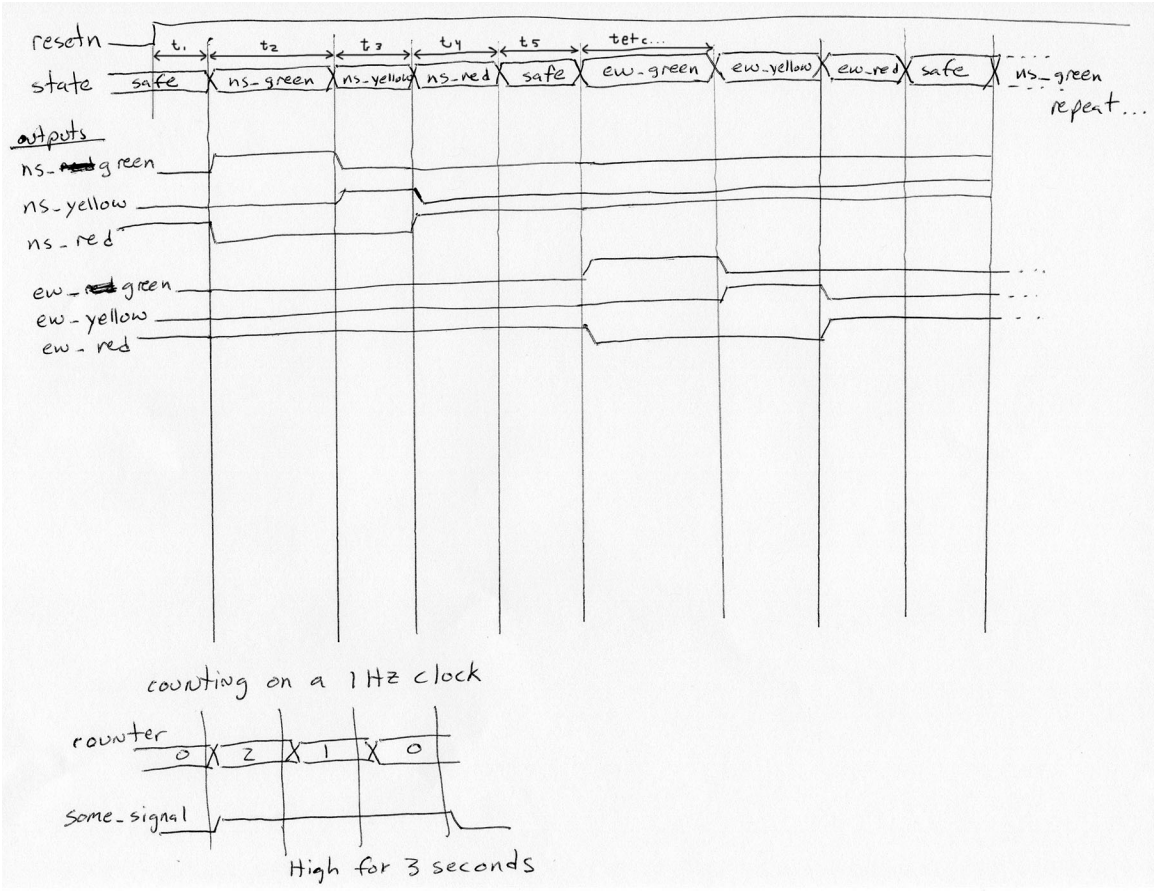
The **durations** that the state machine are in a particular state are:

SAFE after exiting reset	= 15 seconds (t1 in the diagram)
SAFE all other times	= 3 seconds (t5 in the diagram)
GREEN states	= 60 seconds
YELLOW states	= 4 seconds
RED states	= 3 seconds

The input clock to the state machine runs at 1 Hz, ie 1 cycle per second, convenient for counting seconds eh? The output of the state machine should come from flip-flops. These flops will drive the high-current controllers that illuminate the traffic lights.

The state machine can be (should be) built using a counter that defines how long the state machine remains in each state. An example is shown at the bottom of the diagram. The combination of a **state machine** and a **counter** is an incredibly useful combination, as the counter can be loaded with various values that can change over time depending on conditions. In this example, there are fixed times for the GREEN, YELLOW and RED states, but 2 conditions for the SAFE state.

Your assignment is to code up a SystemVerilog solution that implements this traffic controller.


resetn
t1
t2
t3
t4
t5
tetc...
state
safe
ns_green
ns_yellow
ns_red
safe
ew_green
ew_yellow
ew_red
safe
ns_green
repeat...
outputs
ns_green
ns_yellow
ns_red
ew_green
ew_yellow
ew_red
counting on a 1Hz clock
counter
0
2
1
0
some_signal
High for 3 seconds