Initials: _____

CprE 381 Computer Organization and Assembly Level Programming
Spring 2015
Exam 1

Last Name (printed) _____

First Name (printed) _____

Lab Section _____

Instructions:

- **Do not open this exam booklet until told to do so.**
- The exam is open book, open notes.
- Calculator is allowed.
- E-reader is allowed for reading electronic textbook, but it has to be put in the airplane mode.
- Do all work in the space provided. **You must show your work to receive credit.**
- Clearly indicate the answer you want counted.
- Make assumptions if necessary and state your assumption.
- Be sure to complete the three lines above.
- Cheating will not be tolerated by the instructor or your classmates and will result in a severe penalty.
- This is a 50-minute exam.

Score:

Q1	Q2	Q3	Q4	Total
10	**12**	**8**	**10**	**40**

1. Answer the following short questions:

   a. [5] A design team is trying to make a program run faster on an embedded processor. They find that a new compiler optimization can reduce the instruction count by 30% (70% of the original) but increase the CPI by 10% (110% of the original). They also find that they may tune up the processor frequency by 20% (120% of the original) by increasing the voltage level. What is the speedup after both improvements?

   b. [5] A processor runs at 1.5V and 1000MHz in the default setting. The OS can use DVFS (dynamic voltage and frequency scaling) to make the processor run at 1.2V and 500MHz. What is the ratio of power reduction?

Do not use any MIPS pseudo instructions in the following questions.

2. [12 pts] Translate the following C statements into MIPS code. The variables and function are declared as follows. The questions are independent.

```
int m;
int i;
int Y[100];
double data[100];
int count_above(double X[], double threshold);
```

Also assume the following:

- m is a global variable and assigned to memory locations 0($gp).
- i is a local variable and assigned to register $s0.
- The starting address of Y[] is 1000($gp).
- The starting address of data[] is 2000($gp).
- All temporary registers are free.

a. [2 pts] `m = 0xF0FFFF0F;`

b. [5 pts] `Y[i+1] = Y[i];`

c. [5 pts] `m = count_above(data, data[0]);`

Note: In the floating-point part of the call convention, the first floating-point parameter is in $f12 (for `float`) or $f12:$f13 (for `double`), and the second parameter is in $14 or $f14:$15. The return value is in $f0 (for `float`) or $f0:$f1 (for `double`).

3. [8] Translate the following C function into MIPS. Do not use any MIPS pseudo instructions in the following questions.

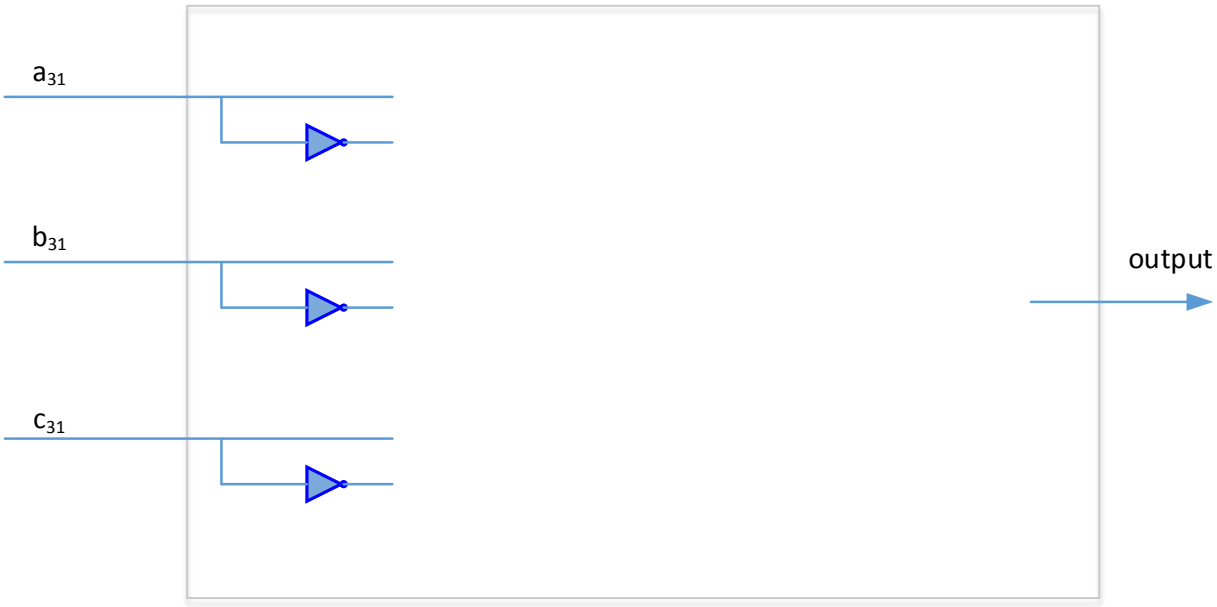
```
// count the number of 1s in a 32-bit binary
unsigned int count_bit_one(unsigned int n)
{
   int count = 0;

   do {
      count += (n & 0x0001);
      n = (n >> 1);
   } while (n != 0);

   return count;
}
```

4. The following questions are regarding arithmetic unit design.

   a. [5 pts] Complete the following schematic diagram for overflow detection logic. The logic is used with an adder that performs c = a + b, where a, b, c are 32-bit 2's complement integers. The inputs to the logic are the sign bits of a, b and c, namely a_{31}, b_{31}, and c_{31}. The 1-bit output is 1 if overflow occurs, 0 otherwise.

   You may only use the following logic gates: AND, OR, NOT (you may not need all of them). The AND gates and OR gates may have up to three inputs.

   Hints:
   - For an adder, overflow occurs if and only if 1) adding two positives yields a negative, or 2) adding two negatives yields a positive.



b. [5] What floating point number does the following 32-bit binary represent? You must show the procedure of conversion to get the full credit.

Note: 32-bit single-precision FP uses 8-bit exponent with a bias of 127 and 23-bit fraction.

```
1011 1111 1000 0000 0000 0000 0000 0000
```