EE552 Project Proposal

Yu-Ting Chiu 2717896258 ychiu078@usc.edu
Beila Zhao 9821347549 beilazha@usc.edu
Chenjie Weng 4599107598 cweng701@usc.edu
Jiahui Wang 2436803430 jwang246@usc.edu

1. Baseline Details

- Topology: 4x4 mesh
- Routing scheme: oblivious deterministic x-y routing
- Switching technique: packet switching
- Gate level implementation: Multiply-and-Accumulate (MAC)

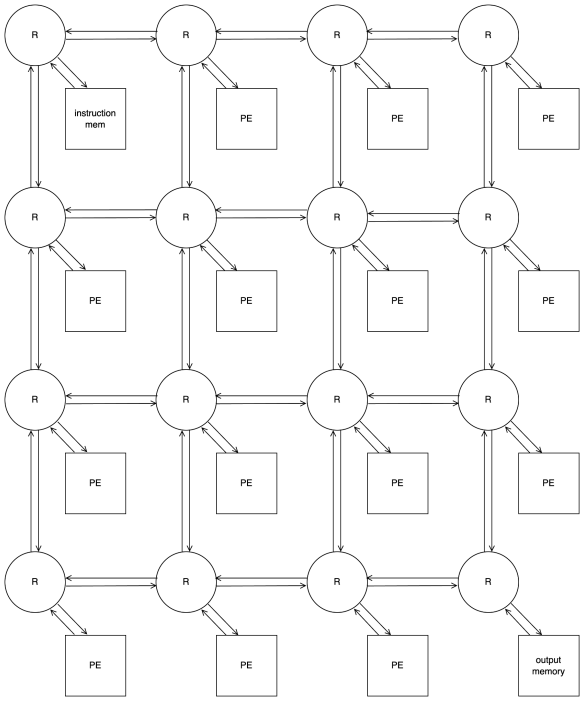

Figure 1. NoC Architecture

2. Enhancement

- Instr mem: develop control system that supports configurable kernel size
- NoC: two sets of NoC, one for control flow(command transfer), one for data flow
- Topology: use a greater mesh to allow kernel size up to 5x5
- PE: to enhance data transfer efficiency, we introduced a filter reuse mechanism whereby each filter weight is transmitted a single time and then reused locally. This optimization minimizes memory bandwidth usage and reduces communication overhead, resulting in improved system performance.

3. Task partitioning

NoC Architecture: Beila Zhao
PE Architecture: Chenjie Weng
Functional Verification: Jiahui Wang
Control System Design: Yu-Ting Chiu