Group 19
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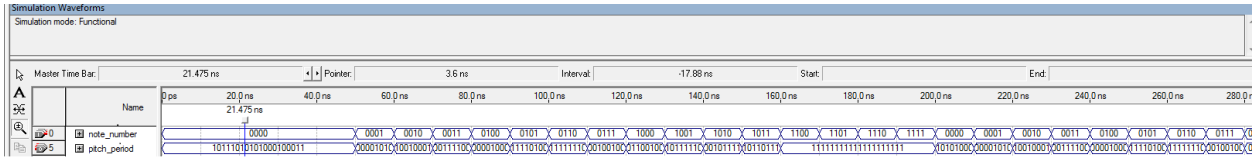
In this lab, we were asked to create a circuit via VHDL for a music box and for a sine decoder. Within the VHDL code for the music box, we have one 4-bit std_vector input and a 20-bit std_vector output.

Variable Name	Type	Bit
note_number	in std logic_vector(3 downto 0)	4
pitch_period	out std logic_vector(19 downto 0)	20

We used the selector method to implement different notes. For example, when we input “0000” the output will be “10111010101000100011” which is a representation of the note C. Thought in an octave, there are only 12 different notes(12 valided inputs) hence there will be 4 invalid inputs. We handle those 4 invalid input by giving the output all 1s as the specification asked.

The following (Figure 1) is the simulation result of the above VHDL code. It demonstrated the code is functioning properly by showing when the input is 0000 the output is 10111010101000100011 etc

Figure 1



G19_sine

A circuit for a sine function is built to calculate a range of values from 0 to 90 degrees. The equation of a sine function is known as

$$s = sin(x)$$

Where x is the input and s is the output. (See table 1) The input is a 7-bit binary number value that represents the values between 0 and 128. On the other hand, the output is a 16-bit binary numbers that represents the fractional part of the number. (See table 2)

Table 1: List of inputs/outputs

Variable	Name
Input	Input[6..0]
Output	Sine[15..0]
Clock Signal	clk

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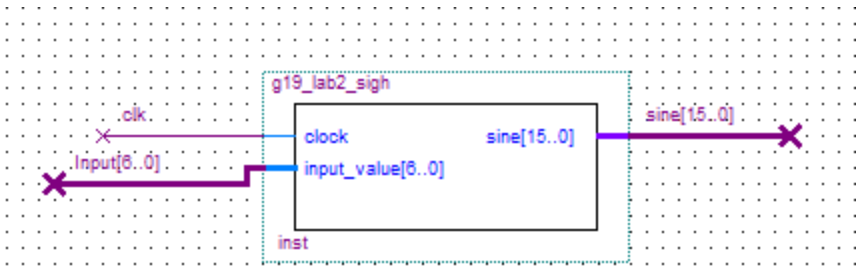
Table 2: Example of fractional part

Variable	x	s
Value	48	0.743144825
Binary Representation	0110001	1011111000111111

A LUT is generated to store all the inputs by creating a Memory Initialization File. A MIF contains the initial values for each address in the memory. Sine shaped waveforms are then generated from the compiled VHDL description. (See Fig. 2)
To write the VHDL, our team used LPM ROM module, which must be supplied with ROM data in an external file known as the MIF.

Figure 2: Sine Circuit



The circuit of the sine function has one 7-bit input, one clock signal and one 16-bit output. This circuit is designed to put the 7-bit input into the schematic symbol of a sine function and give a 16-bit result as its output.

Figure 3

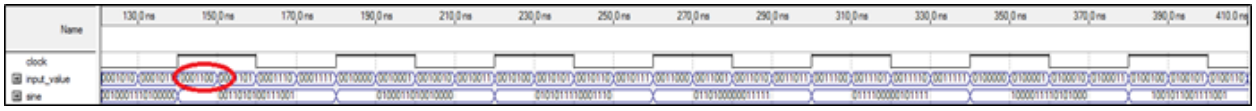


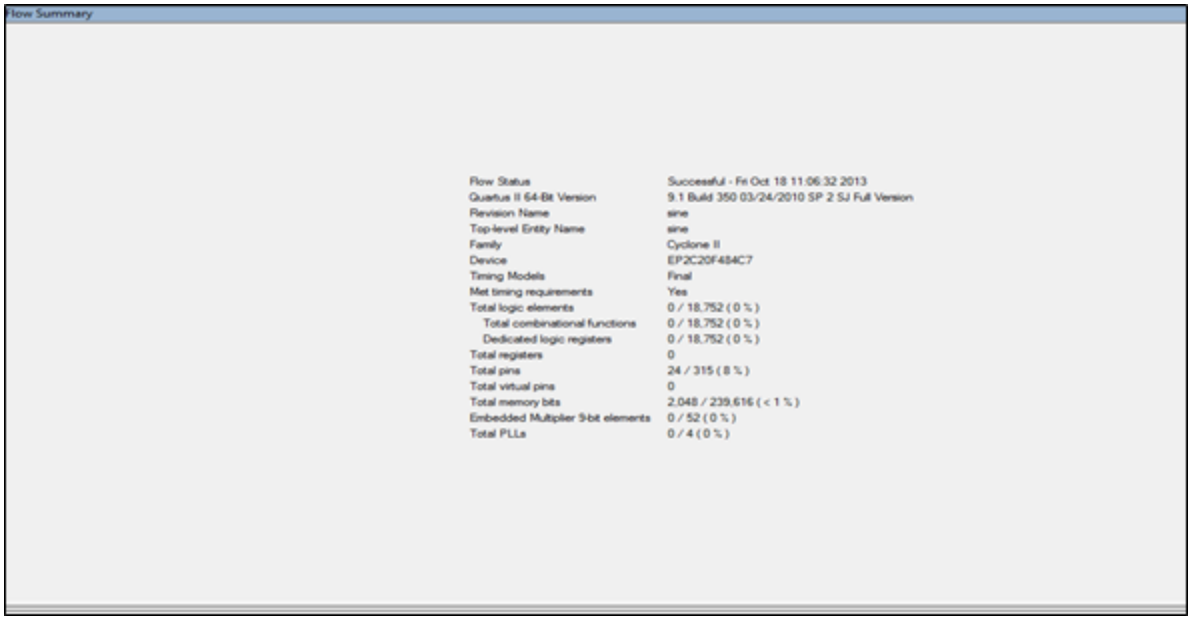
Table 3: MIF (Memory Initialization File)

Addr	+0	+1	+2	+3	+4	+5	+6	+7
0	0000000000000000	0000010001110111	0000100011101111	0000110101100101	0001000111011011	0001011001001111	0001101011000010	0001111100110010
8	0010001110100000	0010100000001100	0010110001110100	0011000011011000	0011010100111001	0011100110010110	0011110111101110	0100001001000001
16	0100011010010000	0100101011011000	0100111100011011	0101001101011000	0101011110001110	0101101110111110	0101111111100110	0110010000000110
24	0110100000011111	0110110000110000	0111000000111001	0111010000111000	0111100000101111	0111110000011100	0111111111111111	1000001111011001
32	1000011110101000	1000101101101101	1000111100100111	1001001011010101	1001011001111001	1001101000010000	1001110110011011	1010000100011011
40	1010010010001101	1010011111110011	1010101101001100	1010111010010111	1011000111010101	1011010100000100	1011100000100110	1011101100111001
48	1011111000111110	1100000100110100	1100010000011011	1100011011110011	1100100110111011	1100110001110011	1100111100011011	1101000110100011
56	1101010000111011	1101011010110011	1101100100011001	1101101101101111	1101110110110011	1101111111100111	1110000000001000	1110010000011001
64	1110011000010111	1110100000000011	1110101011011110	1110101110100110	1110110101011011	1110111011111111	1111000010001111	1111001000001101
72	1111001101111000	1111010011010000	1111011000010101	1111011101000110	1111100001100101	1111100101110000	1111101001100111	1111101101001011
80	1111110000011100	1111110011011001	1111111011000010	1111111000010111	1111111010011000	1111111100000110	1111111101100000	1111111110100110
88	1111111111011000	1111111111110110	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111
96	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111
104	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111
112	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111
120	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111	1111111111111111

In the Flow Summary, it indicates that we used 702 transistors for the simulation of the sine function. (See Fig. 4) The functional simulation also demonstrates that the outputs match with their respective inputs in one clock cycle. Our value can be checked by comparing the input value with its output on the MIF block. For instance, when the input is 0001100, we can see that

its corresponding output is 0011010100111001. Therefore, our input value matches with the sine output. (See Fig. 3)

Figure 4: Number of logic gates



The largest propagation delay of the circuit from the rising edge of the clock signal to the time when the output is stabilized is about 12.22 ns. For example, the rising edge is 60ns and the time the stabilized output is approximately 72.22ns. (See Fig.4) Also, this can be confirmed by looking at the Timing Analyzer Summary, where the worst propagation delay is 12.754ns. (See Fig.5)

Figure 5: Timing Simulation

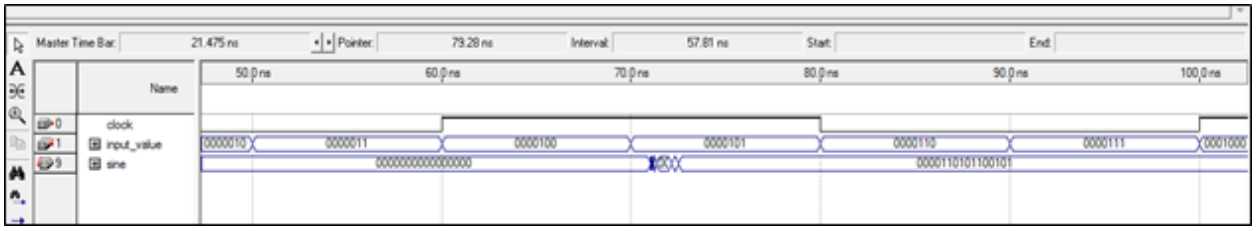


Figure 6: Timing Analyzer

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To
1	Worst-case tsu	N/A	None	4.574 ns	input_value[1]	lpm_rom:crc_table|altron
2	Worst-case tco	N/A	None	12.754 ns	lpm_rom:crc_table|altrom:srom|altsyncram:rom_block|altsyncram_a001:auto_generated|ram_block1a0~porta_address_reg6	sine[2]
3	Worst-case th	N/A	None	-3.496 ns	input_value[2]	lpm_rom:crc_table|altron
4	Total number of failed paths					

The timing simulation takes the various delays in the circuit into account. The propagation delay can be found. Four different input values (0000000, 1111111, 1010101, 0101010) are used to simulate a timing waveform, and we can see that the output match with their input. (See Fig. 6) For the first care, since the rising time of the clock signal is 540ns and the time the output is stabilized is around 552.575ns, the propagation delay is also about 12.575 ns and it is relatively

close to the largest propagation delay, which is 12.754ns. Also, the settling times are approximately the same for the other 3 cases.

Figure 7: Timing Simulation with 4 different inputs