Group 19
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G19_note_number

A 16-bit note information words are stored in a song memory and they are played by our music box. The 16-bit word contains the following information:

Figure 1: Note Information

1. (bits 0-3) Note Number
2. (bits 4-6) Octave Number
3. (bits 7-9) Note Duration
4. (bit 10) Triplet
5. (bits 11-14) Loudness
6. (bit 15) End of Song marker

Each note number represents a specific note in the musical notes whereas the octave number shows which octave the note is to be played at.

Table 1: List of Inputs/Outputs

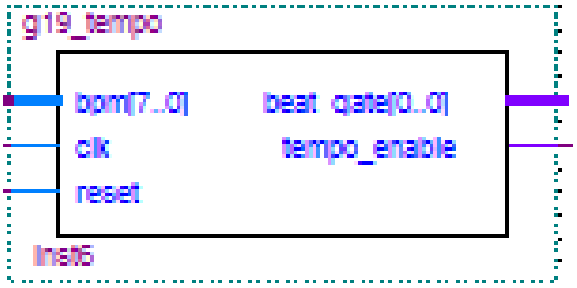
Inputs		Outputs	
Variable Names	Specifications	Variable Names	Specifications
note_duration (3bits)	Indicates how long the note will be played	Gate (1-bit)	Output signal
Triplet (1-bit)	Indicates that the note is 2/3 the duration of regular length note		
tempo_enable (1-bit)	Input signal from g19_tempo (done in previous lab)		
clk	Clock of the circuit		
reset	Asynchronous reset		

The note_duration and the triplet information are used to generate an appropriate note GATE signal (correct high and low period) which match the transition table within the lab slide. The circuit is implemented by using a single process block counter. The circuit takes in a signal called tempo_enable which is generated from the g19_tempo where g19_tempo is acting as a frequency divider. Whenever tempo_enable is high, the value of count is incremented on every clock cycle. Within the note_timer clock, we use process block to implement different operation of the circuit. The gate is set to zero when

the count reaches half of the number of tempo pulses per note. If the count value reaches the number of tempo pulses minus 1, then the GATE is set to 1 again and the count is set to 0.

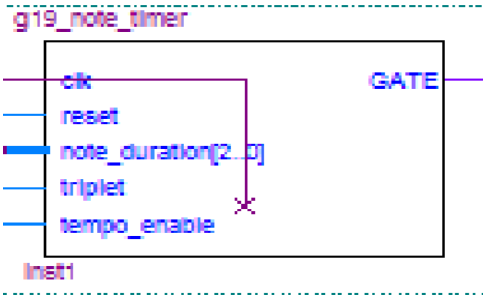
In the circuit, a basic tempo, which is also known as the timing of the notes for the music, is used from the previous laboratory #3. The tempo is measured in Beats per Minute (bpm) and it is 8-bit value. The tempo_enable of the tempo circuit is connected to the tempo_enable input of note_timer block diagram. (See Figure 3) Furthermore, the tempo input is set to a constant value of 120 bpm for stimulation purpose.

Figure 2: Block Diagram of Tempo



The GATE output signal of the note timer block is connected to the GATE input signal of the envelope module our team created in laboratory #3. Both RISE_RATE and FALL_RATE are set to a constant value of 120 for testing purpose.

Figure 3: Block Diagram of the Note Timer



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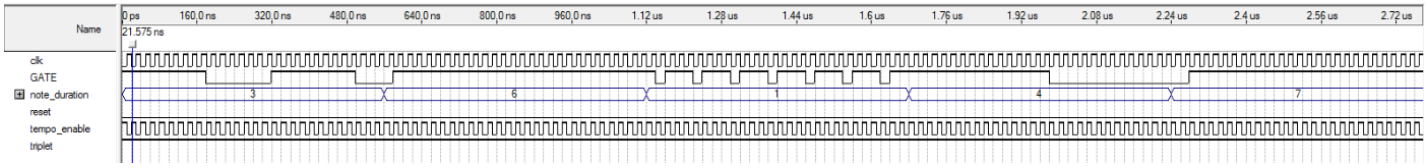
In the simulation, our team tested the circuit with several input values with triplet set to high and keep the note_duration constantly changing after certain amount of time. However since our note_duration values keep on changing, some of the duration is not long enough for the circuit to react or finish a complete cycle on the GATE signal. Hence we check with note duration that has a complete cycle of GATE signal. In the simulation shown in figure 4, we can see that when note_duration is 1, there should be 3 tempo_enable pulse when the GATE signal is high and one pulse when it is low (note the triplet is high) and for note_duration equal to 3, there should be 9 tempo_enable pulse when the GATE signal is high and 7 when it is low (all this are reference to p 17 of the lab lecture slide). Our stimulation shows the same result hence our circuit is functioning correctly.

Figure 4: Simulation of the Note Timer



Finally, the circuit is tested on the DE1 board after our team assigned all the appropriate pins. The note_duration and triplet inputs of the g49_note_timer module and the enable and reset bits are all connected to the switches on the DE1 board. (See Figure 5) And this circuit produce the right LED signal we want as the stimulation show. The time between flashes of the envelope is 2 times longer for every increment in the note duration. Also, if we set the triplet to 1, the duration of the flash is 2/3 as long as when the triplet is set to 0.

Figure 5: Schematic of the whole circuit

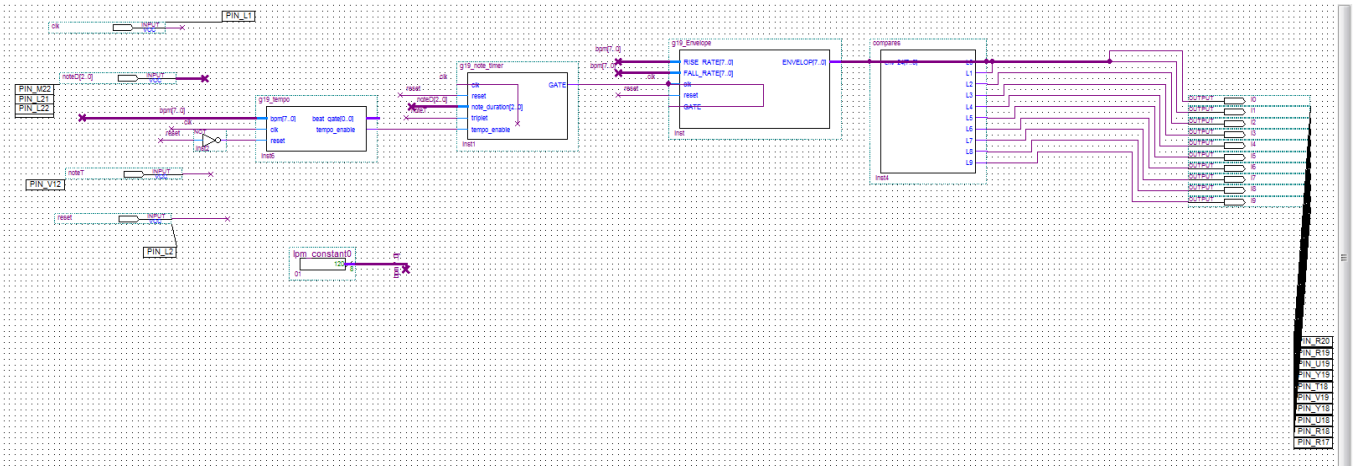


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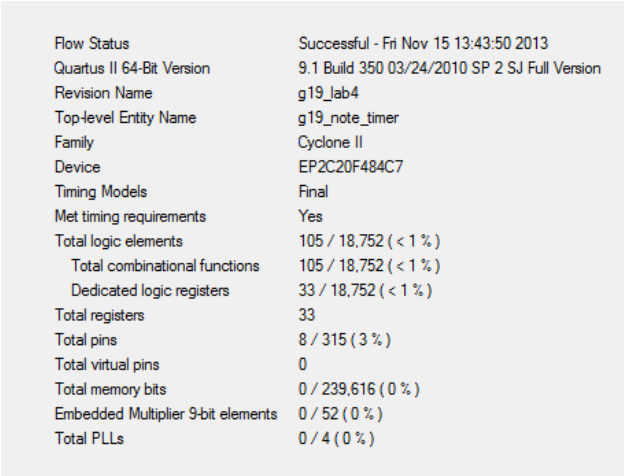
Figure 6: Flow summary



Flow Status	Successful - Fri Nov 15 13:43:50 2013
Quartus II 64-Bit Version	9.1 Build 350 03/24/2010 SP 2 SJ Full Version
Revision Name	g19_lab4
Top-level Entity Name	g19_note_timer
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	105 / 18,752 (< 1 %)
Total combinational functions	105 / 18,752 (< 1 %)
Dedicated logic registers	33 / 18,752 (< 1 %)
Total registers	33
Total pins	8 / 315 (3 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Figure 7: Timing Analyzer

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tsu	N/A	None	16.592 ns	note_duration[1]	n[17]	--	clk	0
2	Worst-case tco	N/A	None	8.604 ns	GATE~reg0	GATE	clk	--	0
3	Worst-case th	N/A	None	-4.419 ns	tempo_enable	n[0]	--	clk	0
4	Clock Setup: 'clk'	N/A	None	131.56 MHz (period = 7.601 ns)	n[0]	n[17]	clk	clk	0
5	Total number of failed paths								0