

BG96 Hardware Design

LTE Module Series

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atlantik
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About the Document

History

Revision	Date	Author	Description
1.0	2017-01-05	Lyndon LIU/ Daryl DU/ Allen WANG	Initial
1.1	2017-03-16	Allen WANG	<ol style="list-style-type: none"> Updated operating frequencies of the module in Table 1. Added GSM features in Table 2.
1.2	2017-03-28	Allen WANG/ Lyndon LIU	<ol style="list-style-type: none"> Updated function diagram in Figure 1. Updated pin assignment (top view) in Figure 2. Added the description of SPI interface in Chapter 3.12.
1.3	2017-04-11	Allen WANG	<ol style="list-style-type: none"> Updated model and frequency band of the module in Table 1. Updated download and upload rates of the module in Table 2. Added the description of NEMA UART interface in Table 4 and Table 13.
1.4	2017-04-28	Allen WANG	<ol style="list-style-type: none"> Updated the function diagram in Figure 1. Updated the pin assignment (top view) in Figure 2. Added the reference circuit of I2S application with audio codec (Figure 20). Added the description of power saving mode (PSM) and the note in Chapter 3.3. Updated the timing of resetting module in Figure 14.

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1 Introduction

This document defines BG96 module and describes its air interface and hardware interfaces which are connected with customers' applications.

This document can help customers quickly understand the interface specifications, electrical and mechanical details, as well as other related information of BG96. To facilitate its application in different fields, reference design is also provided for customers' reference. Associated with application note and user guide, customers can use the module to design and set up mobile applications easily.

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1.1. Safety Information

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating BG96. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for the customers' failure to comply with these precautions.



Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. You must comply with laws and regulations restricting the use of wireless devices while driving.



Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden, so as to prevent interference with communication systems. Consult the airline staff about the use of wireless devices on boarding the aircraft, if your device offers an Airplane Mode which must be enabled prior to boarding an aircraft.



Switch off your wireless device when in hospitals, clinics or other health care facilities. These requests are designed to prevent possible interference with sensitive medical equipment.



Cellular terminals or mobiles operating over radio frequency signal and cellular network cannot be guaranteed to connect in all conditions, for example no mobile fee or with an invalid (U)SIM card. While you are in this condition and need emergent help, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.



Your cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency energy. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.



In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

BG96 is an embedded IoT (LTE Cat M1 and LTE Cat NB1) wireless communication module without receive diversity. It supports LTE-TDD and Half-Duplex LTE-FDD wireless communication, which provides data connectivity on LTE-TDD/FDD networks. It also provides GNSS¹⁾ function and voice²⁾ interface to meet customers' specific application demands. The following table shows the frequency bands of BG96 module.

Table 1: Frequency Bands of BG96 Module

Module	LTE Bands	GSM	Rx-diversity	GNSS ¹⁾
BG96	Cat M1 & NB1:			
	LTE-FDD:			
	B1/B2/B3/B4/B5/B8/B12/ B13/B18/B19/B20/B26/B28 LTE-TDD: B39 (for Cat M1 only)	GSM850/GSM900/ DCS1800/PCS1900	Not Supported	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS

NOTES

- ¹⁾ GNSS function is optional.
- ²⁾ BG96 does not support VoLTE (Voice over LTE) function temporarily.

With a compact profile of 22.5mm × 26.5mm × 2.3mm, BG96 can meet almost all requirements for M2M applications such as automotive, smart metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

BG96 is an SMD type module which can be embedded into applications through its 102 LGA pads. BG96 supports internet service protocols like TCP, UDP and PPP. Extended AT commands have been developed for customers to use these internet service protocols easily.

2.2. Key Features

The following table describes the detailed features of BG96.

Table 2: Key Features of BG96

Features	Details
Power Supply	Supply voltage: 3.3V~4.3V Typical supply voltage: 3.8V
Transmitting Power	Class 3 (23dBm±2.7dB) for LTE-FDD bands Class 3 (23dBm±2.7dB) for LTE-TDD bands Class 4 (33dBm±2dB) for GSM850 Class 4 (33dBm±2dB) for GSM900 Class 1 (30dBm±2dB) for DCS1800 Class 1 (30dBm±2dB) for PCS1900 Class E2 (27dBm±3dB) for GSM850 8-PSK Class E2 (27dBm±3dB) for GSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class E2 (26dBm±3dB) for PCS1900 8-PSK
LTE Features	Support up to LTE Cat M1 and LTE Cat NB1 Support 1.08MHz RF bandwidth Support SISO in DL direction Cat M1: Max. 375kbps (DL)/375kbps (UL) Cat NB1: Max. 32kbps (DL)/70kbps (UL)
GSM Features	GPRS: Support GPRS multi-slot class 12 (12 by default) Coding schemes: CS-1, CS-2, CS-3 and CS-4 Maximum of four Rx time slots per frame GPRS: Max. 85.6kbps (DL)/85.6kbps (UL) EDGE: Support EDGE multi-slot class 12 (12 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 EDGE: Max. 236.8kbps (DL)/236.8kbps (UL)
Internet Protocol Features*	Support TCP/UDP/PPP protocols Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which are usually used for PPP connections
SMS*	Text and PDU mode

	Point to point MO and MT SMS cell broadcast SMS storage: ME by default
(U)SIM Card Interface	Support (U)SIM card: 1.8V, 3.0V
Audio Feature*	Support one digital audio interface: I2S interface
USB Interface	Compliant with USB 2.0 specification (slave only) and the data transfer rate can reach up to 480Mbps Used for AT command communication, data transmission, GNSS NEMA output, software debugging and firmware upgrade Support USB drivers for Windows XP, Windows Vista, Windows 7, Windows 8/8.1, Window 10, Linux 2.6 or later, Android 4.0/4.2/4.4/5.0/5.1/6.0
UART Interfaces	UART1: Used for data transmission and AT command communication Baud rate reach up to 3000000bps; 115200bps by default Support RTS and CTS hardware flow control UART2: Used for module debugging and log output 115200bps baud rate UART3/SPI*: UART3 is the default configuration when the module is used as a modem. In this case, it is used for outputting GNSS data or NEMA sentences. When the module is used as the core board, the port can be multiplexed into SPI* interface for data transferring.
AT Commands	3GPP TS 27.007 and 3GPP TS 27.005 AT commands, as well as Quectel enhanced AT commands
Network Indication	One NETLIGHT pin for network connectivity status indication
Antenna Interfaces	Including main antenna (ANT_MAIN) and GNSS antenna (ANT_GNSS) interfaces
Physical Characteristics	Size: 22.5mm × 26.5mm × 2.3mm Weight: approx. 3.1g
Temperature Range	Operation temperature range: -35°C ~ +75°C ¹⁾ Extended temperature range: -40°C ~ +85°C ²⁾
Firmware Upgrade	USB interface and DFOTA*
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. “*” means under development.
2. ¹⁾ Within operation temperature range, the module is 3GPP compliant.

3. ²⁾ Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

2.3. Functional Diagram

The following figure shows a block diagram of BG96 and illustrates the major functional parts.

- Power management
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interfaces

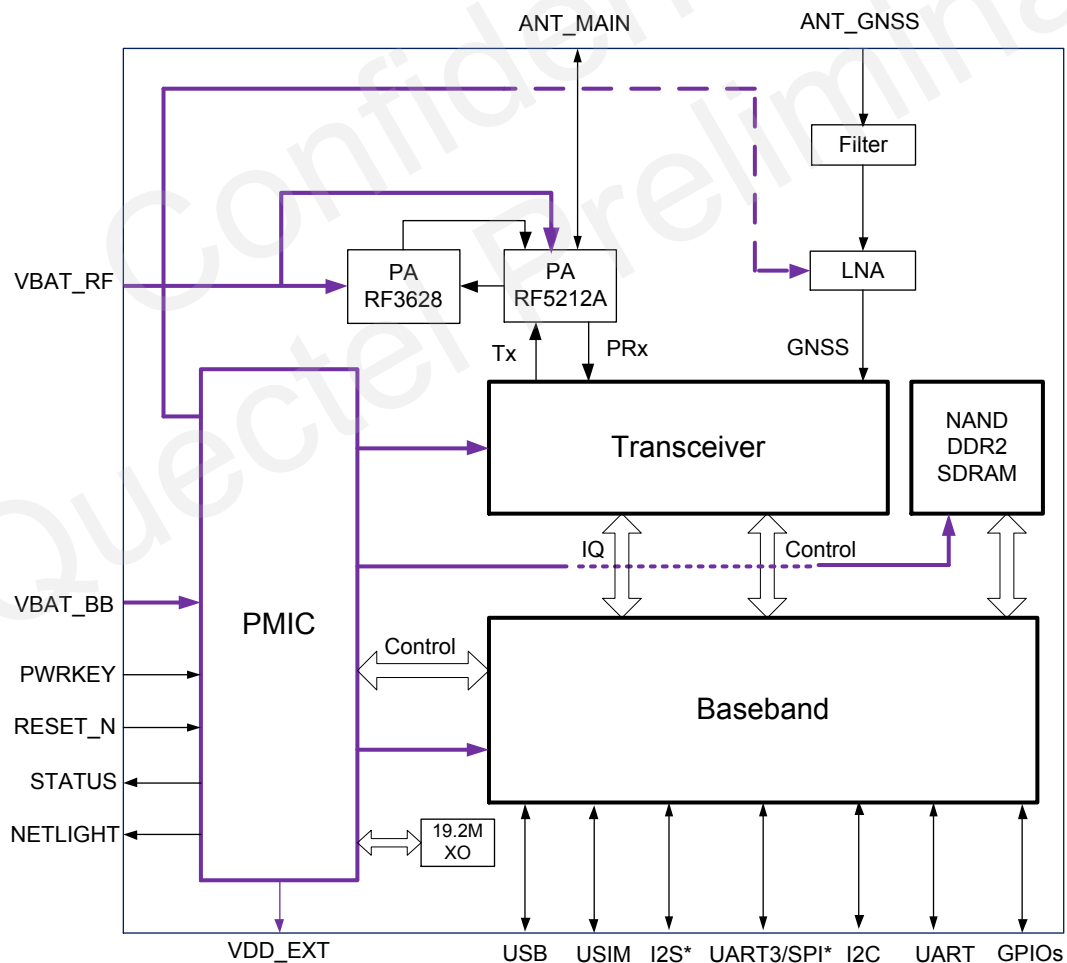


Figure 1: Functional Diagram

NOTE

“*” means under development.

2.4. Evaluation Board

In order to help customers develop applications conveniently with BG96, Quectel supplies the evaluation board (EVB), USB data cable, earphone, antenna and other peripherals to control or test the module.

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3 Application Interfaces

BG96 is equipped with 62-pin 1.1mm pitch SMT pads and 40-pin ground/reserved pads that can be connected to customers' cellular application platforms. The following sub-chapters will provide detailed description of interfaces listed below:

- Power supply
- (U)SIM card interface
- USB interface
- UART interfaces
- I2S* interface
- UART3/SPI* interface
- Status indication
- USB_BOOT interface

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3.1. Pin Assignment

The following figure shows the pin assignment of BG96.

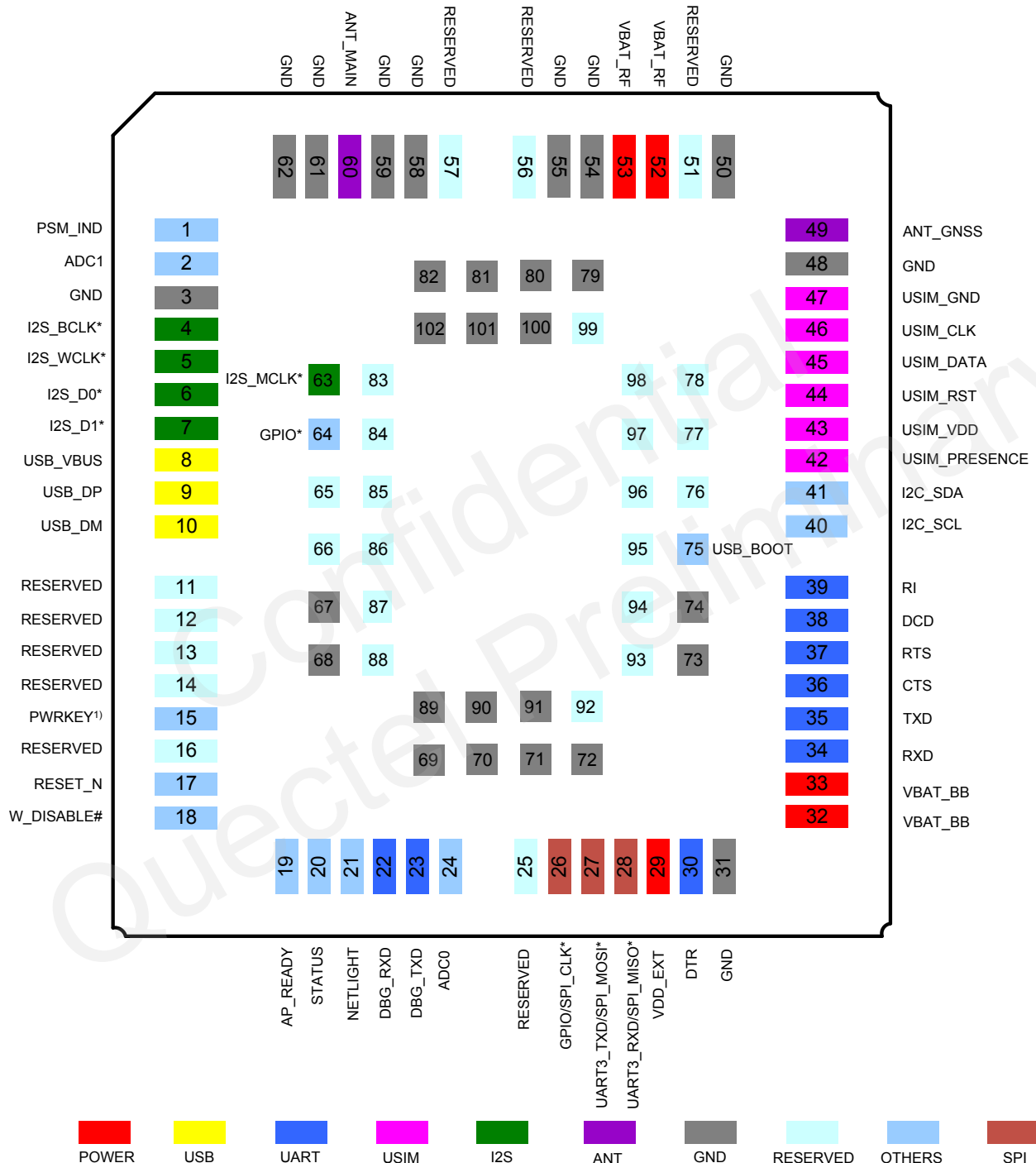


Figure 2: Pin Assignment (Top View)

NOTES

1. Keep all RESERVED pins and unused pins unconnected.
2. GND pads should be connected to ground in the design.
3. ¹⁾ PWRKEY output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
4. "*" means under development.

3.2. Pin Description

The following tables show the pin definition and description of BG96.

Table 3: Definition of I/O Parameters

Type	Description
IO	Bidirectional
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

Table 4: Pin Description

Power Supply					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT_BB	32, 33	PI	Power supply for module baseband part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	
VBAT_RF	52, 53	PI	Power supply for module RF	Vmax=4.3V Vmin=3.3V	

			part	Vnorm=3.8V	
VDD_EXT	29	PO	Provide 1.8V for external circuit	Vnorm=1.8V I _O max=50mA	Power supply for external GPIO's pull up circuits.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67~74, 79~82, 89~91, 100~102		Ground		

Turn on/off

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	15	DI	Turn on/off the module	V _{IH} max=2.1V V _{IH} min=1.3V V _{IL} max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
RESET_N	17	DI	Reset signal of the module	V _{IH} max=2.1V V _{IH} min=1.3V V _{IL} max=0.5V	If unused, keep this pin open.

Status Indication

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
STATUS	20	OD	Indicate the module's operation status	V _{OH} min=1.35V V _{OL} max=0.45V	1.8V power domain. If unused, keep this pin open.
NETLIGHT	21	DO	Indicate the module's network activity status	V _{OH} min=1.35V V _{OL} max=0.45V	1.8V power domain. If unused, keep it open.

USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	8	PI	USB detection	Vmax=5.25V Vmin=3.0V Vnorm=5.0V	
USB_DP	9	IO	USB differential data bus (+)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω.

USB_DM	10	IO	USB differential data bus (-)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω.
(U)SIM Card Interface					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM_GND	47		Specified ground for (U)SIM card		
USIM_VDD	43	PO	Power supply for (U)SIM card	For 1.8V (U)SIM: V _{max} =1.9V V _{min} =1.7V For 3.0V (U)SIM: V _{max} =3.05V V _{min} =2.7V I _{Omax} =50mA	Either 1.8V or 3V is supported by the module automatically.
USIM_DATA	45	IO	Data signal of (U)SIM card	For 1.8V (U)SIM: V _{ILmax} =0.6V V _{IHmin} =1.2V V _{OLmax} =0.45V V _{OHmin} =1.35V For 3.0V (U)SIM: V _{ILmax} =1.0V V _{IHmin} =1.95V V _{OLmax} =0.45V V _{OHmin} =2.55V	
USIM_CLK	46	DO	Clock signal of (U)SIM card	For 1.8V (U)SIM: V _{OLmax} =0.45V V _{OHmin} =1.35V For 3.0V (U)SIM: V _{OLmax} =0.45V V _{OHmin} =2.55V	
USIM_RST	44	DO	Reset signal of (U)SIM card	For 1.8V (U)SIM: V _{OLmax} =0.45V V _{OHmin} =1.35V For 3.0V (U)SIM: V _{OLmax} =0.45V V _{OHmin} =2.55V	

USIM_			(U)SIM card	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.
PRESENCE	42	DI	insertion detection		

UART1 Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RI	39	DO	Ring indicator	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
DCD	38	DO	Data carrier detection	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
RTS	37	DI	Request to send	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.
CTS	36	DO	Clear to send	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
TXD	35	DO	Transmit data	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
RXD	34	DI	Receive data	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.
DTR	30	DI	Data terminal ready. Sleep mode control.	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. Pull-up by default. Low level wakes up the module. If unused, keep it open.

UART2 Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DBG_TXD	23	DO	Transmit data	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
DBG_RXD	22	DI	Receive data	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.

UART3/SPI* Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
----------	---------	-----	-------------	--------------------	---------

GPIO/ SPI_CLK*	26	DO	GPIO/SPI master clock	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
UART3_TXD/ SPI_MOSI*	27	DO	Transmit data/ Master Out Slave In of SPI interface	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
UART3_RXD/ SPI_MISO*	28	DI	Receive data/ Master In Slave Out of SPI interface	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.

I2S* Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
I2S_MCLK*	63	DO	I2S master clock	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
I2S_BCLK*	4	DO	I2S bit clock	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
I2S_WCLK*	5	DO	I2S data frame clock	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
I2S_D0*	6	IO	I2S data 0	$V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{OLmax}=0.45V$ $V_{IHmin}=1.35V$	1.8V power domain. If unused, keep it open.
I2S_D1*	7	IO	I2S data 1	$V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{OLmax}=0.45V$ $V_{IHmin}=1.35V$	1.8V power domain. If unused, keep it open.

I2C Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
I2C_SCL	40	OD	I2C serial clock. Used for external codec.		External pull-up resistor is required. 1.8V only. If unused, keep it open.
I2C_SDA	41	OD	I2C serial data. Used for external codec.		External pull-up resistor is required. 1.8V only. If unused, keep it open.

Antenna Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
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ANT_MAIN	60	IO	Main antenna interface	50Ω impedance	
ANT_GNSS	49	AI	GNSS antenna interface	50Ω impedance	If unused, keep it open.

Other Pins

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PSM_IND*	1	DO	Power saving mode indicator	V _{IL} min=-0.3V V _{IL} max=0.6V V _{IH} min=1.2V V _{IH} max=2.0V	1.8V power domain. If unused, keep it open.
W_DISABLE#	18	DI	Airplane mode control	V _{IL} min=-0.3V V _{IL} max=0.6V V _{IH} min=1.2V V _{IH} max=2.0V	1.8V power domain. Pull-up by default. In low voltage level, the module can enter into airplane mode. If unused, keep it open.
AP_READY*	19	DI	Application processor sleep state detection	V _{IL} min=-0.3V V _{IL} max=0.6V V _{IH} min=1.2V V _{IH} max=2.0V	1.8V power domain. If unused, keep it open.
USB_BOOT	75	DI	Force the module to boot from USB port	V _{IL} min=-0.3V V _{IL} max=0.6V V _{IH} min=1.2V V _{IH} max=2.0V	1.8V power domain. If unused, keep it open.
GPIO*	64	IO	General-purpose input/output	V _{IL} min=-0.3V V _{IL} max=0.6V V _{IH} min=1.2V V _{IH} max=2.0V	1.8V power domain. If unused, keep it open.

ADC Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC1	2	AI	General purpose analog to digital converter interface	Voltage range: 0.3V to VBAT_BB	If unused, keep it open.
ADC0	24	AI	General purpose analog to digital converter interface	Voltage range: 0.3V to VBAT_BB	If unused, keep it open.

RESERVED Pins

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RESERVED	11~14, 16, 25, 51, 56, 57, 65, 66, 76~78, 83~88, 92~99		Reserved		Keep these pins unconnected.

NOTES

1. Keep all RESERVED pins and unused pins unconnected.
2. “*” means under development.

3.3. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 5: Overview of Operating Modes

Mode	Details
Normal Operation	Idle Software is active. The module has registered on network, and it is ready to send and receive data.
	Talk/Data Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	AT+CFUN command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.
Airplane Mode	AT+CFUN command or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.
PSM*	A UE may adopt the PSM (Power Saving Mode) for reducing its power consumption. PSM is similar to power-off, but the UE remains registered on the network and there is no need to re-attach or re-establish PDN connections. When the module is successfully entered into the PSM, PSM_IND* outputs a low level.

Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.
-----------------	--

NOTES

1. In PSM or sleep mode, it is recommended to use UART interface for module connection. USB connection is NOT recommended as it will cause increase in power consumption.
2. "*" means under development.

3.4. Power Saving

3.4.1. Sleep Mode

BG96 is able to reduce its current consumption to a minimum value during sleep mode. The following describes the power saving procedure of BG96 module.

3.4.1.1. UART Application

If the host communicates with module via UART interface, the following preconditions can let the module enter into sleep mode.

- Execute **AT+QSCCLK=1** command to enable sleep mode.
- Drive DTR to high level.

The following figure shows the connection between the module and the host.

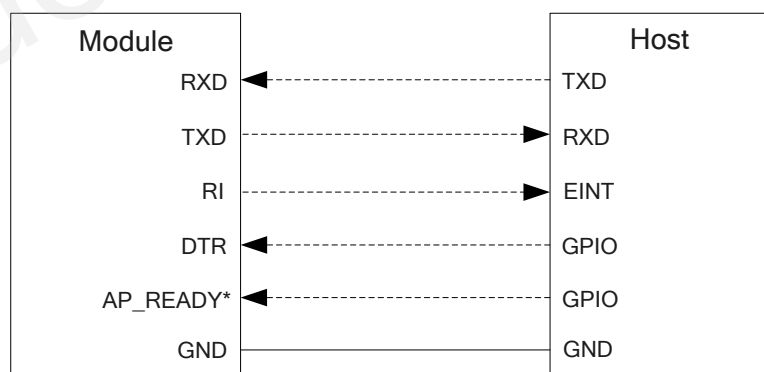


Figure 3: Sleep Mode Application via UART

- Driving the host DTR to low level will wake up the module.
- When BG96 has URC to report, RI signal will wake up the host. Refer to **Chapter 3.15** for details about RI behaviors.
- AP_READY* will detect the sleep state of the host (can be configured to high level or low level detection). Please refer to **AT+QCFG="apready"** command for details.

3.4.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup functions, the following three preconditions must be met to let the module enter into sleep mode.

- Execute **AT+QSClk=1** command to enable the sleep mode.
- Ensure the DTR is held in high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

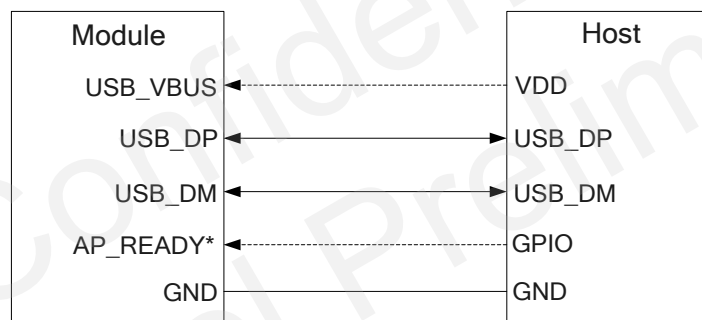


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to BG96 through USB will wake up the module.
- When BG96 has URC to report, the module will send remote wake-up signals via USB bus so as to wake up the host.

3.4.1.3. USB Application with USB Suspend/Resume and RI Function

If the host supports USB suspend/resume, but does not support remote wake-up function, the RI signal is needed to wake up the host. There are three preconditions to let the module enter into sleep mode.

- Execute **AT+QSClk=1** command to enable sleep mode.
- Ensure the DTR is held in high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

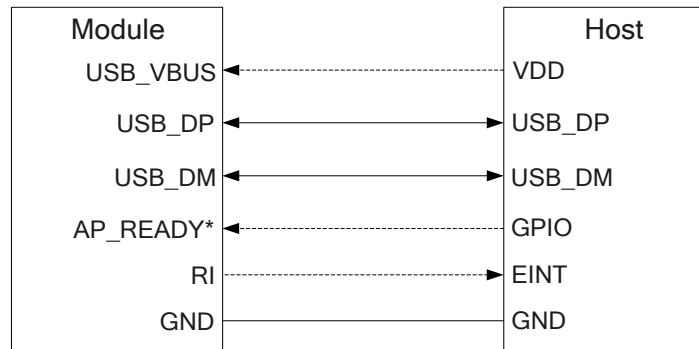


Figure 5: Sleep Mode Application with RI

- Sending data to BG96 through USB will wake up the module.
- When BG96 has a URC to report, RI signal will wake up the host.

3.4.1.4. USB Application without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be disconnected via an additional control circuit to let the module enter into sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Ensure the DTR is held in high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

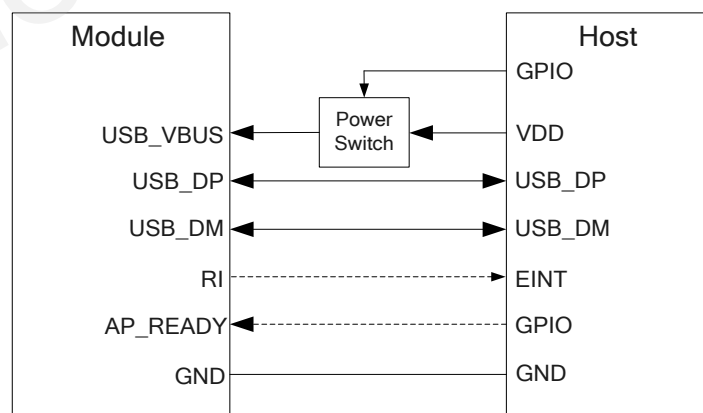


Figure 6: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTES

1. Please pay attention to the level match shown in dotted line between the module and the host. Refer to **document [1]** for more details about BG96 power management application.
2. “*” means under development.

3.4.2. Airplane Mode

When the module enters into airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. This mode can be set via the following ways.

Hardware:

W_DISABLE# is pulled up by default. Driving it to low level will let the module enter into airplane mode.

Software:

AT+CFUN=<fun> command provides choice of the functionality level, through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality mode (by default).
- **AT+CFUN=4**: Airplane mode. RF function is disabled.

NOTES

1. Airplane mode control via W_DISABLE# is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"** command. The command is still under development.
2. The execution of **AT+CFUN** command will not affect GNSS function.

3.5. Power Supply

3.5.1. Power Supply Pins

BG96 provides four VBAT pins for connection with an external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part.
- Two VBAT_BB pins for module's baseband part.

The following table shows the details of VBAT pins and ground pins.

Table 6: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	52, 53	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	32, 33	Power supply for module's baseband part	3.3	3.8	4.3	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67~74, 79~82, 89~91, 100~102	Ground	-	-	-	-

3.5.2. Decrease Voltage Drop

The power supply range of the module is from 3.3V to 4.3V. Please make sure that the input voltage will never drop below 3.3V.

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be used to provide the low ESR. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1mm, and the width of VBAT_RF trace should be no less than 2mm. In principle, the longer the VBAT trace is, the wider it will be.

Three ceramic capacitors (100nF, 33pF, 10pF) are recommended to be applied to the VBAT pins. These capacitors should be placed close to the VBAT pins. In addition, in order to get a stable power source, it is suggested that you should use a zener diode of which reverse zener voltage is 5.1V and dissipation power is more than 0.5W. The following figure shows the star structure of the power supply.

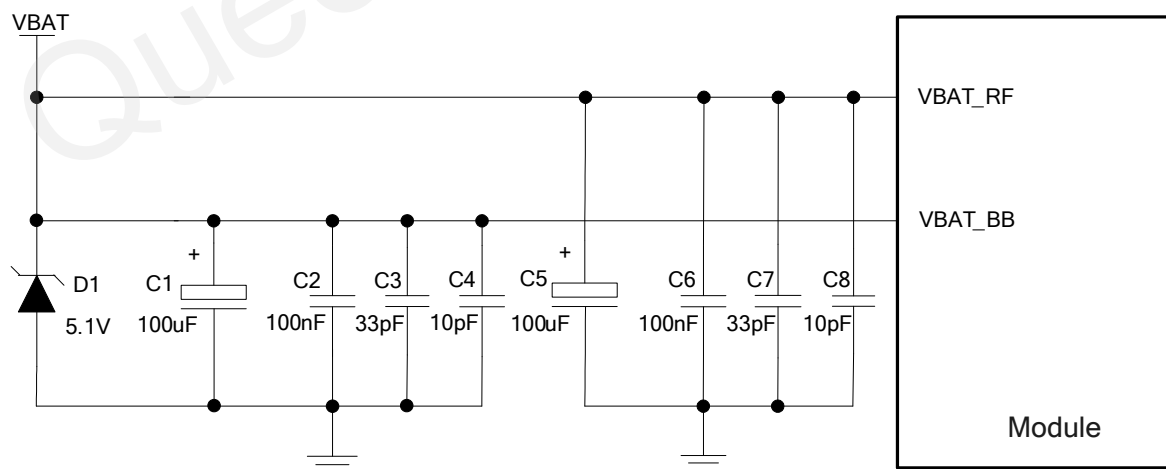


Figure 7: Star Structure of the Power Supply

3.5.3. Monitor the Power Supply

AT+CBC command can be used to monitor the VBAT_BB voltage value. For more details, please refer to *document [2]*.

3.6. Turn on and off Scenarios

3.6.1. Turn on Module Using the PWRKEY Pin

The following table shows the pin definition of PWRKEY.

Table 7: Pin Definition of PWRKEY

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	15	Turn on/off the module	$V_{IHmax}=2.1V$ $V_{IHmin}=1.3V$ $V_{ILmax}=0.5V$	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.

When BG96 is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 100ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin (require external pull-up) outputting a low level, PWRKEY pin can be released. A simple reference circuit is illustrated in the following figure.

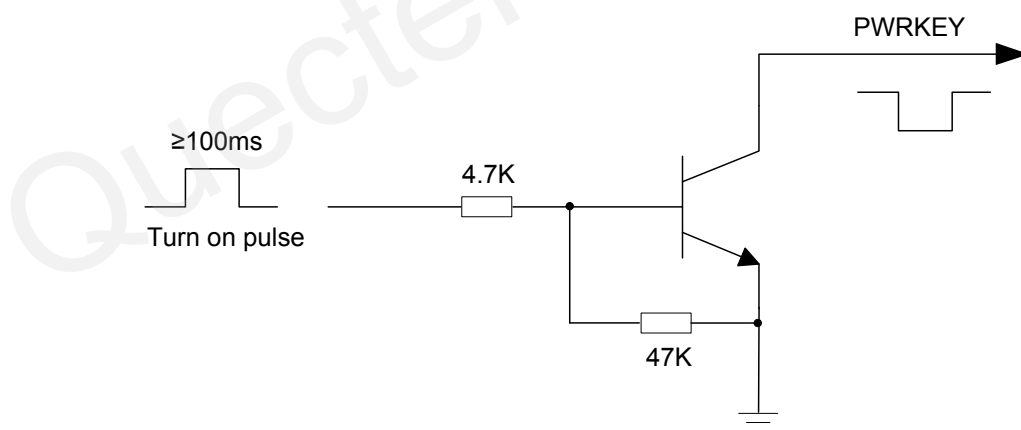


Figure 8: Turn on the Module Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

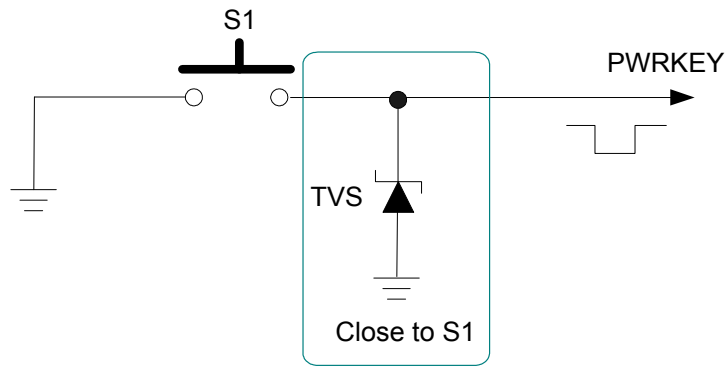


Figure 9: Turn on the Module Using Keystroke

The turn on scenario is illustrated in the following figure.

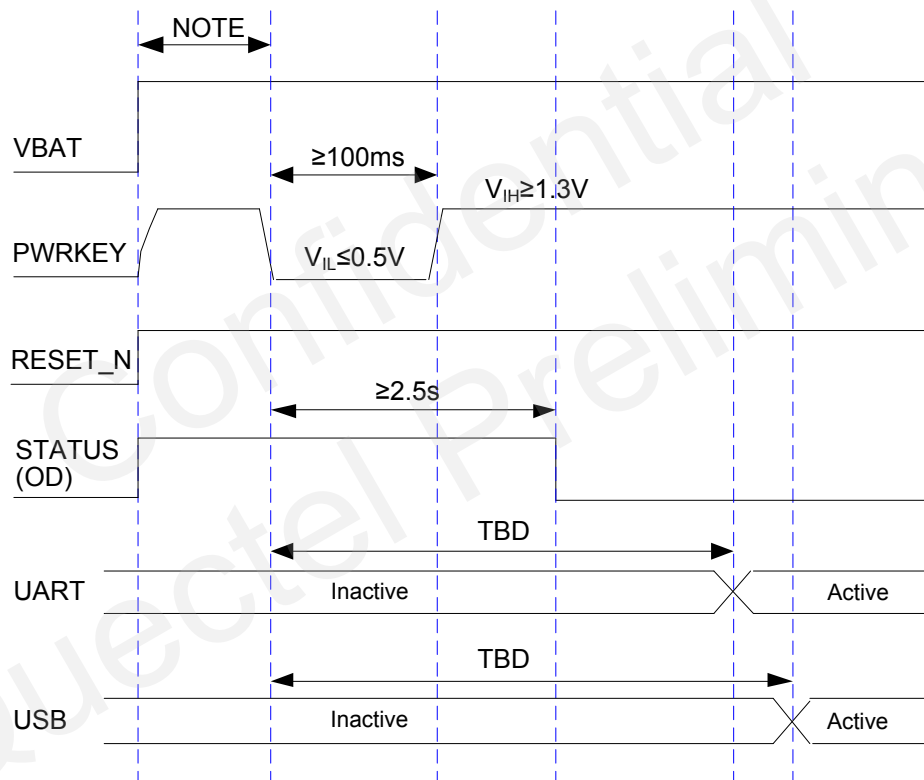


Figure 10: Timing of Turning on Module

NOTE

Make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30ms.

3.6.2. Turn off Module

The following procedures can be used to turn off the module:

- Normal power down procedure: Turn off the module using the PWRKEY pin.
- Normal power down procedure: Turn off the module using **AT+QPOWD** command.

3.6.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage (the specific time is TBD), the module will execute power-down procedure after the PWRKEY is released. The power-down scenario is illustrated in the following figure.

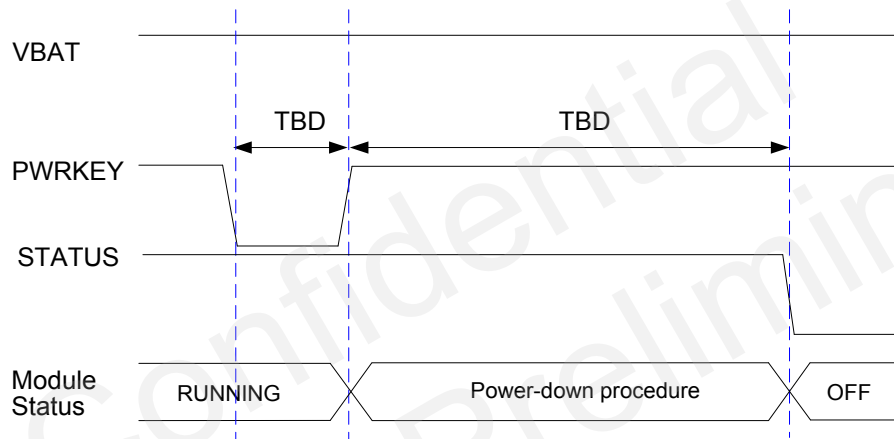


Figure 11: Timing of Turning off Module

3.6.2.2. Turn off Module Using AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to turning off the module via PWRKEY pin.

Please refer to **document [2]** for details about **AT+QPOWD** command.

3.7. Reset the Module

The RESET_N pin can be used to reset the module. The module can be reset by driving RESET_N to a low level voltage for time between Treset_min and Treset_max.

Table 8: RESET_N Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	17	Reset signal of the module	V _{IH} max=2.1V V _{IH} min=1.3V V _{IL} max=0.5V	

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

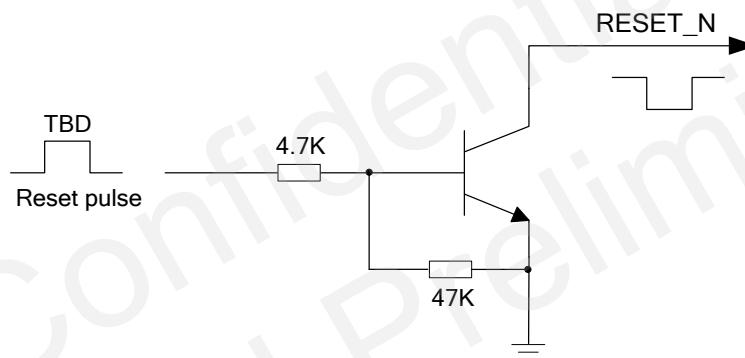


Figure 12: Reference Circuit of RESET_N by Using Driving Circuit

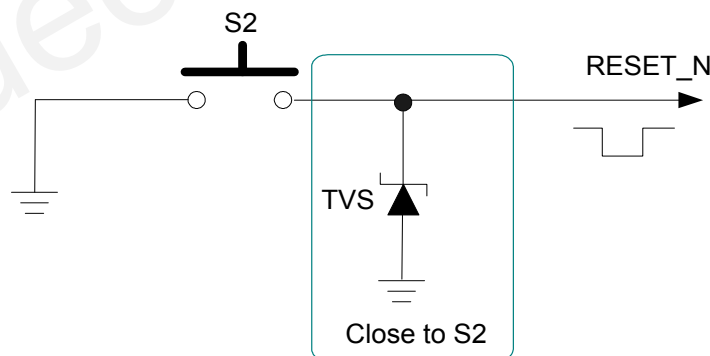


Figure 13: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

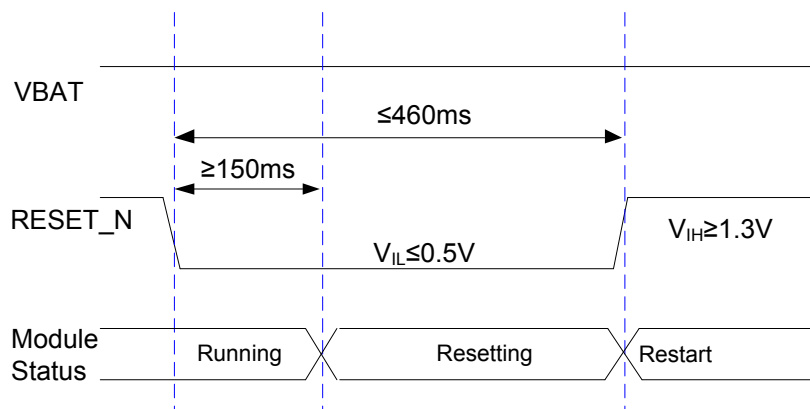


Figure 14: Timing of Resetting Module

NOTES

1. Use RESET_N only when turning off the module by **AT+QPOWD** command and PWRKEY pin both failed.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.8. (U)SIM Card Interface

The (U)SIM card interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8V and 3.0V (U)SIM cards are supported.

Table 9: Pin Definition of (U)SIM Card Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	43	PO	Power supply for (U)SIM card	Either 1.8V or 3.0V is supported by the module automatically.
USIM_DATA	45	IO	Data signal of (U)SIM card	
USIM_CLK	46	DO	Clock signal of (U)SIM card	
USIM_RST	44	DO	Reset signal of (U)SIM card	
USIM_PRESENCE	42	DI	(U)SIM card insertion detection	
USIM_GND	47		Specified ground for (U)SIM card	

BG96 supports (U)SIM card hot-plug via the USIM_PRESENCE pin. The function supports low level and high level detections, and is disabled by default. Please refer to **document [2]** about **AT+QSIMDET** command for details.

The following figure shows a reference design of (U)SIM card interface with an 8-pin (U)SIM card connector.

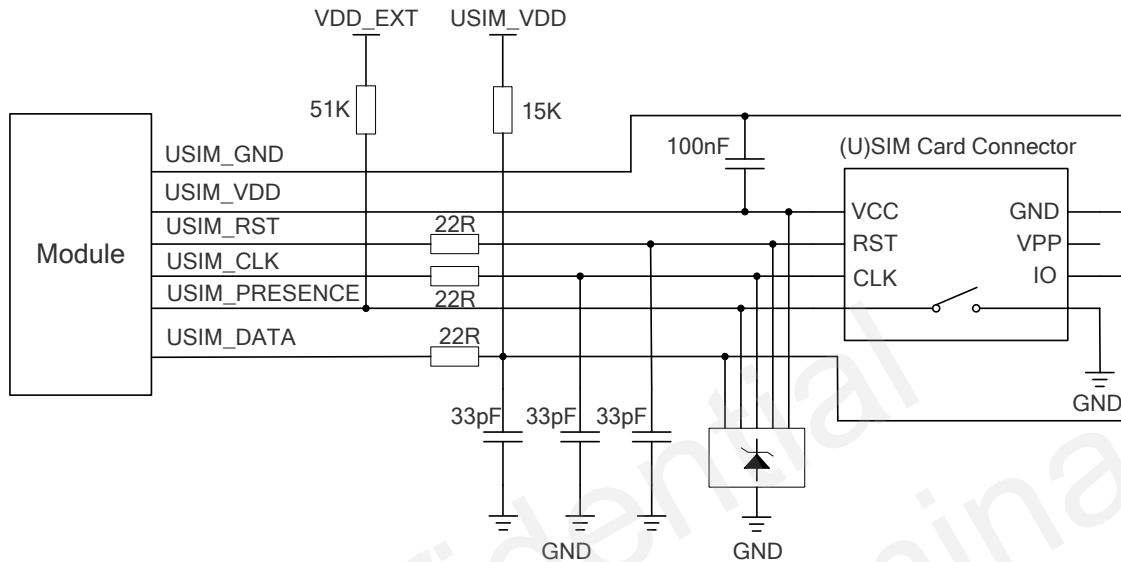


Figure 15: Reference Circuit of (U)SIM Card Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_PRESENCE unconnected. A reference circuit for (U)SIM card interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

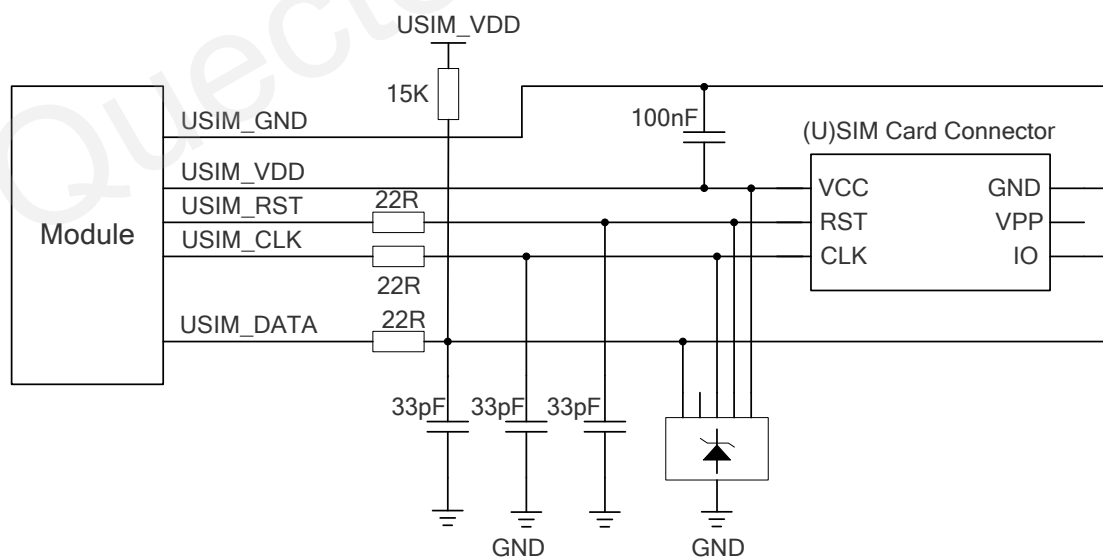


Figure 16: Reference Circuit of (U)SIM Card Interface with a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design:

- Keep layout of (U)SIM card as close to the module as possible. Keep the trace length as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 50pF. The 22Ω resistors should be added in series between the module and the (U)SIM card so as to suppress EMI spurious transmission and enhance ESD protection. The 33pF capacitors are used for filtering interference of GSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.9. USB Interface

BG96 contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480Mbps) and full-speed (12Mbps) modes. The USB interface is used for AT command communication, data transmission, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 10: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	PI	USB connection detection	Typically 5.0V
USB_DP	9	IO	USB differential data bus (+)	Require differential impedance of 90Ω
USB_DM	10	IO	USB differential data bus (-)	Require differential impedance of 90Ω
GND	3		Ground	

For more details about USB 2.0 specification, please visit <http://www.usb.org/home>.

The USB interface is recommended to be reserved for firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

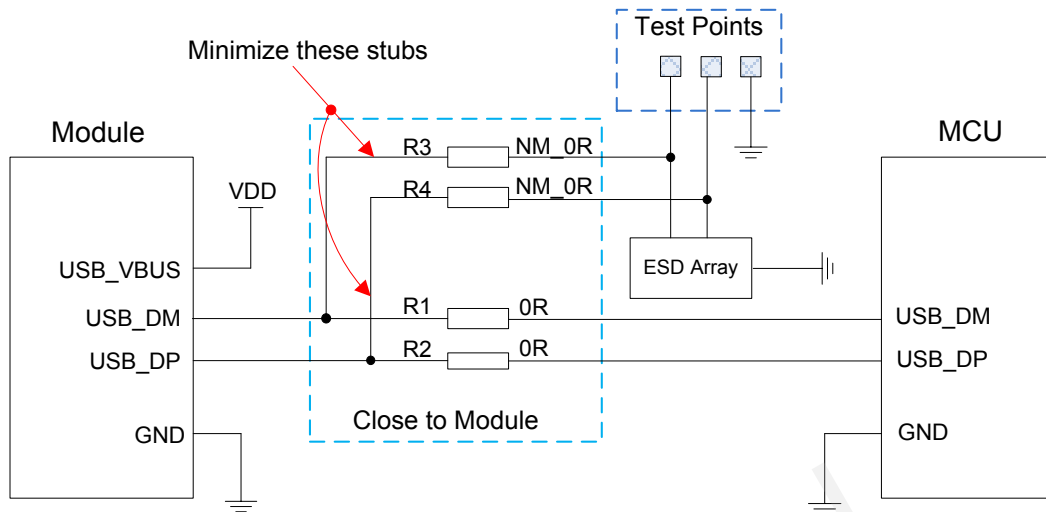


Figure 17: Reference Circuit of USB Application

In order to ensure signal integrity of USB data lines, components R1, R2, R3 and R4 must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω .
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2pF.
- Keep the ESD protection components to the USB connector as close as possible.

NOTE

BG96 module can only be used as a slave device.

3.10. UART Interfaces

The module provides three UART interfaces: UART1, UART2 and UART3 interfaces. The following are their features.

- UART1 interface supports 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 3000000bps baud rates, and the default is 115200bps. This interface is used for data transmission and AT command communication.
- UART2 interface supports 115200bps baud rate. It is used for module debugging and log output.
- UART3 interface is used for outputting GNSS data or NEMA sentences. It can be multiplexed into SPI* interface.

The following tables show the pin definition of the three UART interfaces.

Table 11: Pin Definition of UART1 Interface

Pin Name	Pin No.	I/O	Description	Comment
DTR	30	DI	Sleep mode control	1.8V power domain
RXD	34	DI	Receive data	1.8V power domain
TXD	35	DO	Transmit data	1.8V power domain
CTS	36	DO	Clear to send	1.8V power domain
RTS	37	DI	Request to send	1.8V power domain
DCD	38	DO	Data carrier detection	1.8V power domain
RI	39	DO	Ring indicator	1.8V power domain

Table 12: Pin Definition of UART2 Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	23	DO	Transmit data	1.8V power domain
DBG_RXD	22	DI	Receive data	1.8V power domain

Table 13: Pin Definition of UART3 Interface

Pin Name	Pin No.	I/O	Description	Comment
UART3_TXD	27	DO	Transmit data	1.8V power domain
UART3_RXD	28	DI	Receive data	1.8V power domain

The logic levels are described in the following table.

Table 14: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8V UART interface. A level translator should be used if your application is equipped with a 3.3V UART interface. A level translator TXS0108EPWR provided by *Texas Instrument* is recommended. The following figure shows a reference design.

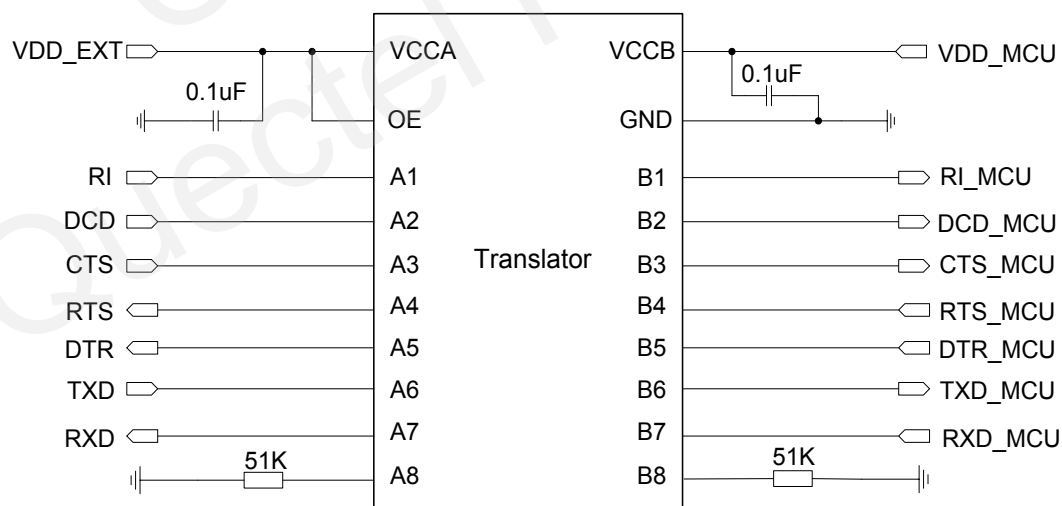


Figure 18: Reference Circuit with Translator Chip

Please visit <http://www.ti.com> for more information.

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the circuit design of solid line section, in terms of both module input and output circuit designs, but please pay attention to the direction of connection.

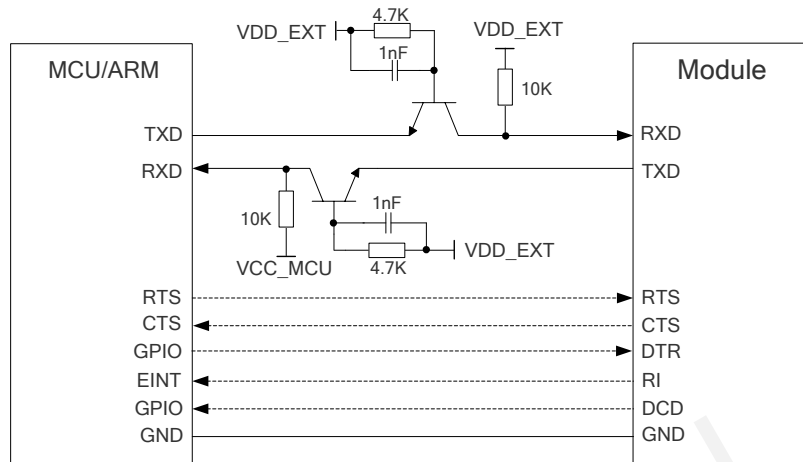


Figure 19: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.

3.11. I2S* and I2C Interfaces

BG96 provides one Inter-IC Sound (I2S) digital interface* and one I2C interface.

The following table shows the pin definition of I2S* and I2C interfaces which can be applied on audio codec design.

Table 15: Pin Definition of I2S* and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2S_MCLK*	63	DO	I2S master clock	1.8V power domain.
I2S_BCLK*	4	DO	I2S bit clock	1.8V power domain
I2S_WCLK*	5	DO	I2S data frame clock	1.8V power domain

I2S_D0*	6	IO	I2S data 0	1.8V power domain
I2S_D1*	7	IO	I2S data 1	1.8V power domain
I2C_SCL	40	OD	I2C serial clock	Require external pull-up to 1.8V
I2C_SDA	41	OD	I2C serial data	Require external pull-up to 1.8V

The following figure shows a reference design of I2S* and I2C interfaces with an external codec IC.

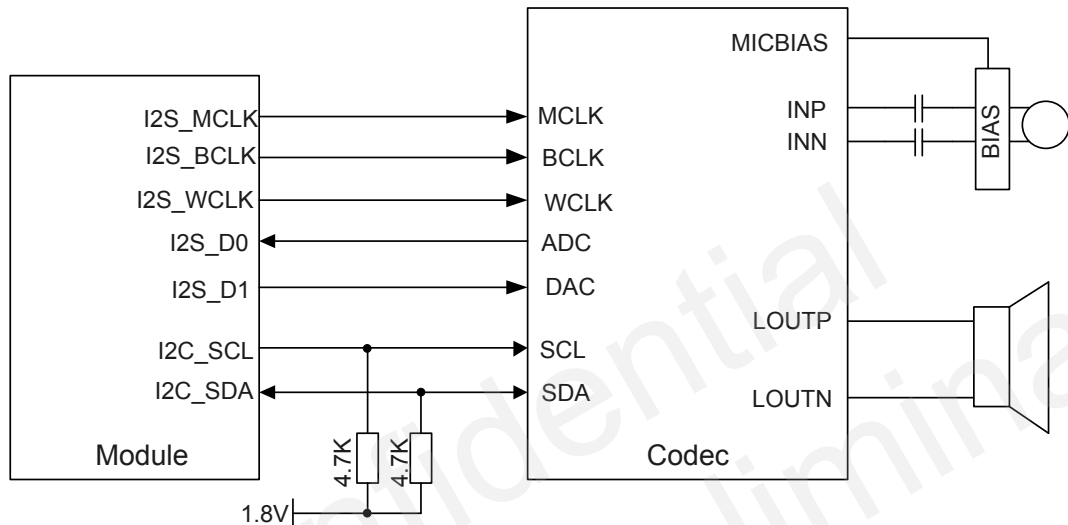


Figure 20: Reference Circuit of I2S Application with Audio Codec

NOTE

"*" means under development.

3.12. SPI* Interface

BG96 provides one Serial Peripheral Interface (SPI) digital interface* which is multiplexed from UART3 (default configuration).

The following table shows the pin definition of SPI* interface which can be used to transfer data.

Table 16: Pin Definition of SPI* Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK*	26	DO	SPI master clock	1.8V power domain.
SPI_MOSI*	27	DO	Master Out Slave in of SPI interface	1.8V power domain
SPI_MISO*	28	DI	Master In Slave Out of SPI interface	1.8V power domain

NOTE

“*” means under development.

3.13. Network Status Indication

BG96 provides one network indication pin: NETLIGHT. The pin is used to drive a network status indication LED. The following tables describe the pin definition and logic level changes of NETLIGHT in different network activity status.

Table 17: Pin Definition of Network Status Indicator

Pin Name	Pin No.	I/O	Description	Comment
NETLIGHT	21	DO	Indicate the module's network activity status	1.8V power domain

Table 18: Working State of the Network Status Indicator

Pin Name	Logic Level Changes	Network Status
NETLIGHT	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle
	Flicker quickly (125ms High/125ms Low)	Data transfer is ongoing
	Always high	Voice calling

A reference circuit is shown in the following figure.

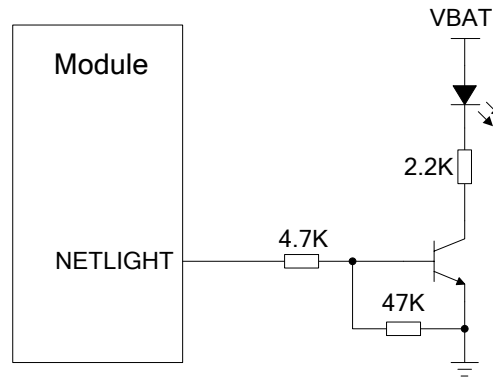


Figure 21: Reference Circuit of the Network Status Indicator

3.14. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It can be connected to a GPIO of DTE with a pulled up resistor, or as LED indication circuit as below. When the module is turned on normally, the STATUS will present a low state. Otherwise, the STATUS will present high-impedance state.

Table 19: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	OD	Indicate the module's operation status	Require external pull-up

The following figure shows different circuit designs of STATUS, and you can choose either one according to your application demands.

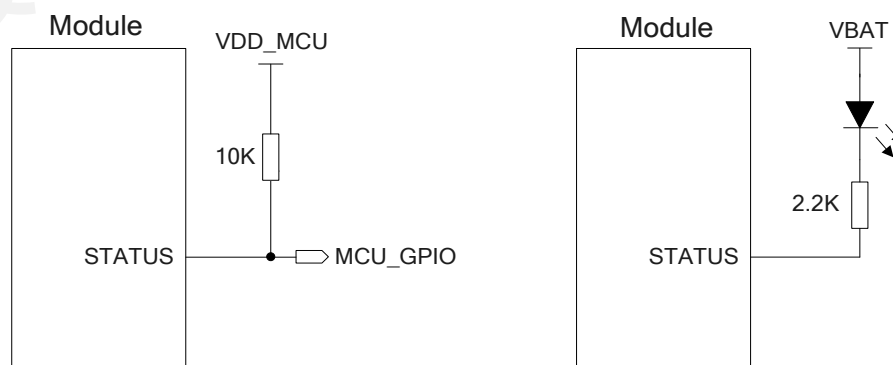


Figure 22: Reference Circuit of STATUS

3.15. Behaviors of RI

AT+QCFG="risignaltpe", "physical" command can be used to configure RI behavior.

No matter on which port URC is presented, URC will trigger the behavior of RI pin.

NOTE

URC can be outputted from UART port, USB AT port and USB modem port, through configuration via **AT+QURCCFG** command. The default port is USB AT port.

The default behaviors of RI are shown as below.

Table 20: Default Behaviors of RI

State	Response
Idle	RI keeps in high level.
URC	RI outputs 120ms low pulse when new URC returns.

The default RI behaviors can be configured flexibly by **AT+QCFG="urc/ri/ring"** command. **AT+QCFG** command is still under development. For more details, please refer to **document [2]**.

3.16. USB_BOOT Interface

BG96 provides a USB_BOOT pin. During development or factory production, USB_BOOT pin can force the module to boot from USB port for firmware upgrade.

Table 21: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module to boot from USB port	1.8V power domain. Active high. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT interface.

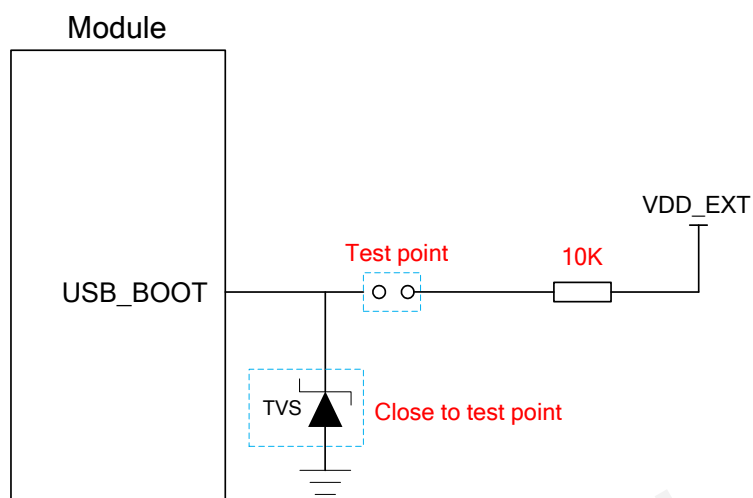


Figure 23: Reference Circuit of USB_BOOT Interface

4 GNSS Receiver

4.1. General Description

BG96 includes a fully integrated global navigation satellite system solution that supports Gen8C-Lite of Qualcomm (GPS, GLONASS, BeiDou/Compass, Galileo and QZSS).

BG96 supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1Hz data update rate via USB interface by default.

By default, BG96 GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to **document [3]**.

4.2. GNSS Performance

The following table shows the GNSS performance of BG96.

Table 22: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	TBD	dBm
	Reacquisition	Autonomous	TBD	dBm
	Tracking	Autonomous	TBD	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	TBD	s
		XTRA* enabled	TBD	s
	Warm start @open sky	Autonomous	TBD	s
		XTRA* enabled	TBD	s
	Hot start	Autonomous	TBD	s
		Autonomous	TBD	s

	@open sky	XTRA* enabled	TBD	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	TBD	m

NOTES

1. Tracking sensitivity: the lowest GNSS signal value at the antenna port on which the module can keep on positioning for 3 minutes.
2. Reacquisition sensitivity: the lowest GNSS signal value at the antenna port on which the module can fix position again within 3 minutes after loss of lock.
3. Cold start sensitivity: the lowest GNSS signal value at the antenna port on which the module fixes position within 3 minutes after executing cold start command.
4. “*” means under development.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in your design.

- Maximize the distance between GNSS antenna and main antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50Ω characteristic impedance for the ANT_GNSS trace.

Please refer to **Chapter 5** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

BG96 includes a main antenna interface and a GNSS antenna interface. The antenna interfaces have an impedance of 50Ω.

5.1. Main Antenna Interface

5.1.1. Pin Definition

The pin definition of main antenna interface is shown below.

Table 23: Pin Definition of Main Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	IO	Main antenna interface	50Ω impedance

5.1.2. Operating Frequency

Table 24: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
B1	1920~1980	2110~2170	MHz
B2 (PCS1900)	1850~1910	1930~1990	MHz
B3 (DCS1800)	1710~1785	1805~1880	MHz
B4	1710~1755	2110~2155	MHz
B5 (GSM850)	824~849	869~894	MHz
B8 (GSM900)	880~915	925~960	MHz
B12	699~716	728~746	MHz

B13	777~787	746~757	MHz
B18	815~829.9	860~874.9	MHz
B19	830~844.9	875~889.9	MHz
B20	832~862	791~821	MHz
B26	814~848.9	859~893.9	MHz
B28	703~748	758~803	MHz
B39	1880~1920	1880~1920	MHz

5.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN antenna pad is shown as below. A π -type matching circuit should be reserved for better RF performance, and the π -type matching components (R1/C1/C2) should be placed as close the antenna as possible. The capacitors are not mounted by default.

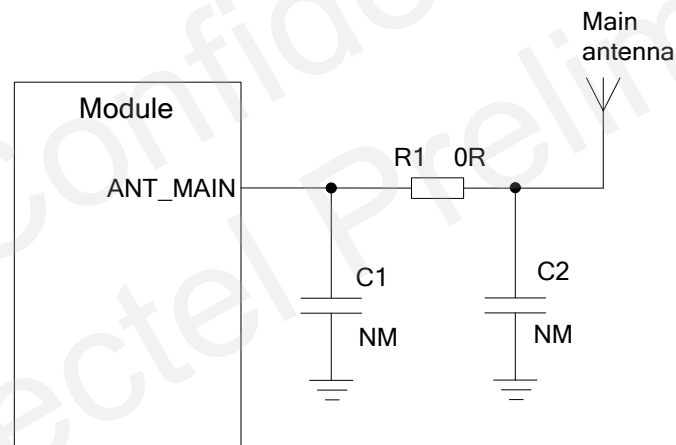


Figure 24: Reference Circuit of RF Antenna Interface

5.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the distance between signal layer and reference ground (H), and the clearance between RF trace and ground (S). Microstrip line or coplanar waveguide line is typically used in RF layout for characteristic impedance control. The following are reference designs of microstrip line or coplanar waveguide line with different PCB structures.

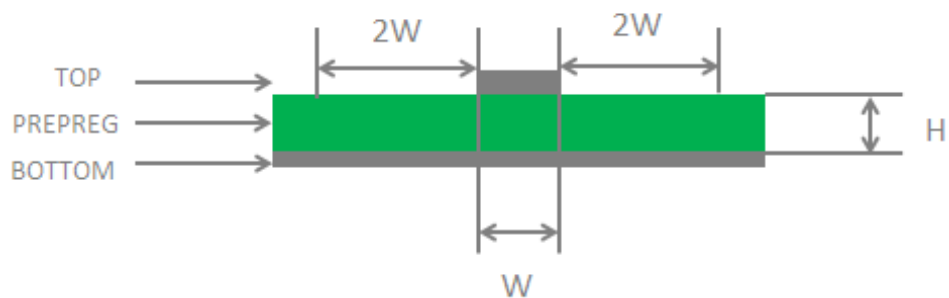


Figure 25: Microstrip Line Design on a 2-layer PCB

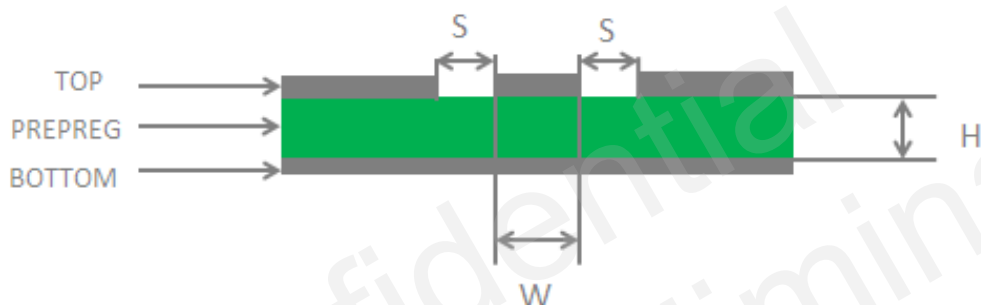


Figure 26: Coplanar Waveguide Line Design on a 2-layer PCB

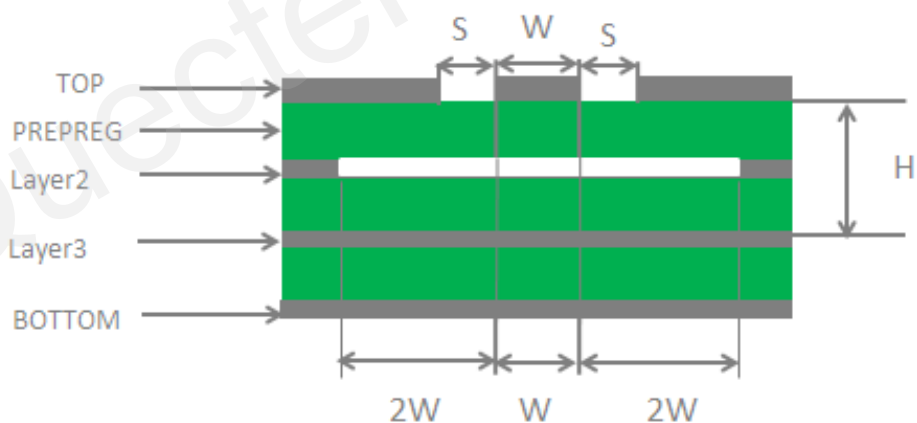


Figure 27: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

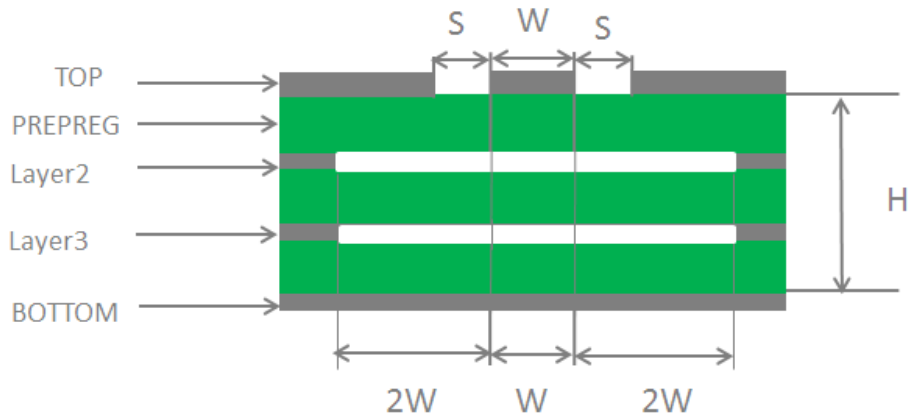


Figure 28: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to control the characteristic impedance of RF traces as 50Ω .
- The GND pins adjacent to RF pins should not be hot welded, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces ($2*W$).

For more details about RF layout, please refer to **document [4]**.

5.2. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 25: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50Ω impedance

Table 26: GNSS Frequency

Type	Frequency	Unit
GPS/Galileo/QZSS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
BeiDou	1561.098±2.046	MHz

A reference design of GNSS antenna is shown as below.

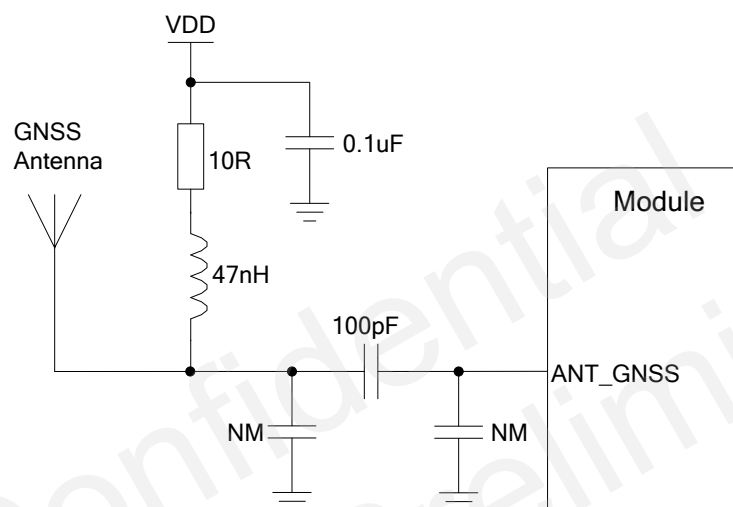


Figure 29: Reference Circuit of GNSS Antenna Interface

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirements

The following table shows the requirements on main antenna.

Table 27: Main Antenna Requirements

Type	Requirements
LTE/GSM	<p>VSWR: ≤ 2</p> <p>Gain (dBi): 1</p> <p>Max Input Power (W): 50</p> <p>Input Impedance (Ω): 50</p> <p>Polarization Type: Vertical</p> <p>Cable Insertion Loss: $< 1\text{dB}$</p> <p>(LTE B5/B8/B12/B13/B18/B19/B20/B26/B28 GSM850/GSM900)</p> <p>Cable Insertion Loss: $< 1.5\text{dB}$</p> <p>(LTE B1/B2/B3/B4/B39, DCS1800/PCS1900)</p>

5.3.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use the UF.L-R-SMT connector provided by *HIROSE*.

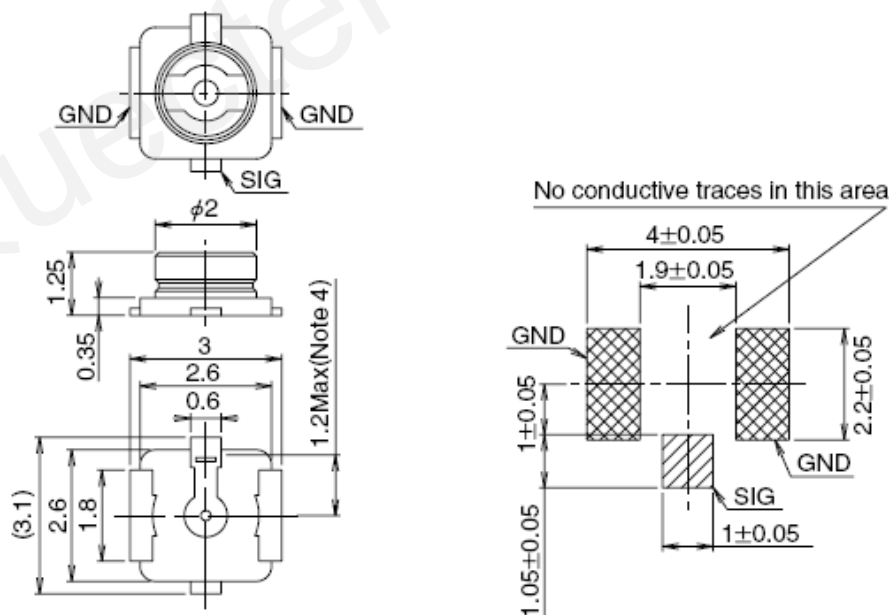


Figure 30: Dimensions of the UF.L-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.F.L-R-SMT.

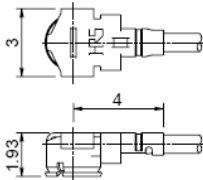
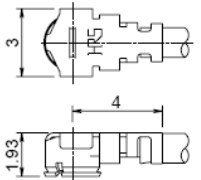
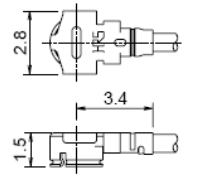
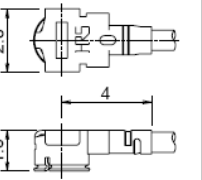
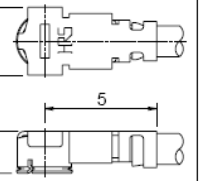
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 31: Mechanicals of U.F.L-LP Connectors

The following figure describes the space factor of mated connector.

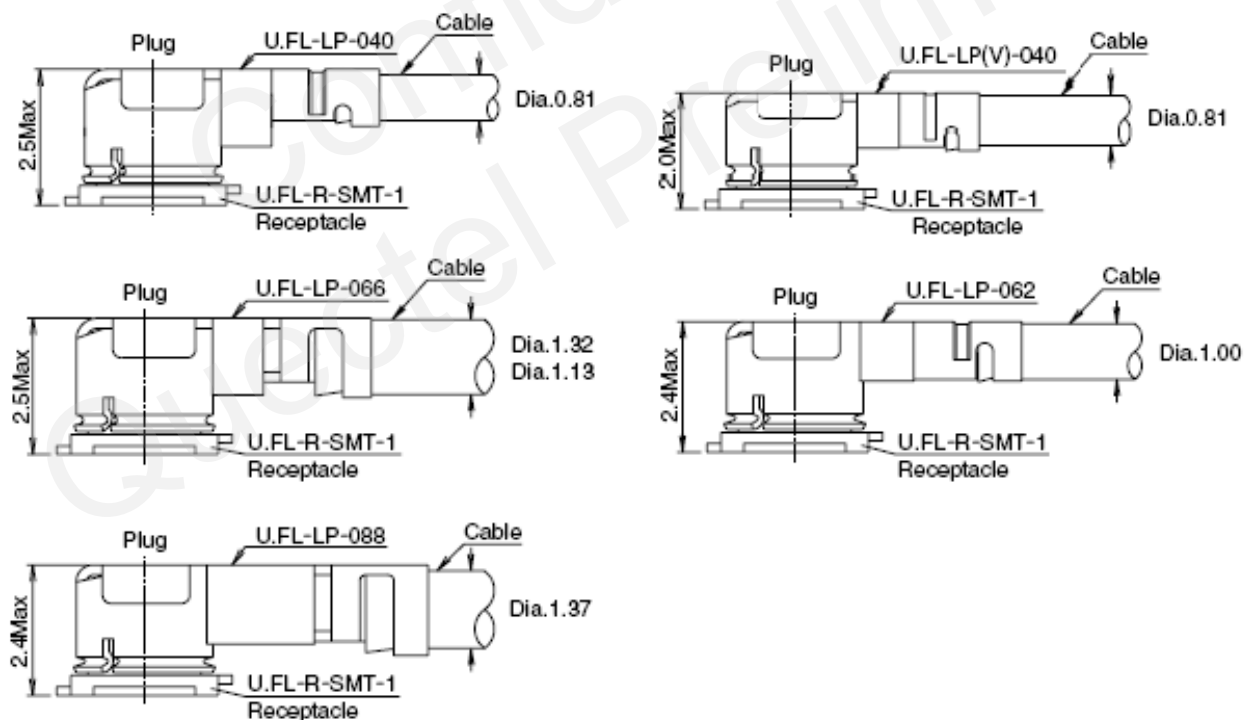


Figure 32: Space Factor of Mated Connector (Unit: mm)

For more details, please visit <http://www.hirose.com>.

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 28: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	TBD	A
Peak Current of VBAT_RF	0	TBD	A
Voltage at Digital Pins	-0.3	2.3	V

6.2. Power Supply Ratings

Table 29: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	Voltage must stay within the min/max values, including voltage drop, ripple and spikes.	3.3	3.8	4.3	V

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I _{VBAT}	Peak supply current (during transmission slot)			TBD	TBD	A
USB_VBUS	USB detection		3.0	5.0	5.25	V

6.3. Operation Temperature

The operation temperature is listed in the following table.

Table 30: Operation Temperature

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range ¹⁾	-35	+25	+75	°C
Extended Temperature Range ²⁾	-40		+85	°C

NOTES

- ¹⁾ Within operation temperature range, the module is 3GPP compliant.
- ²⁾ Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

6.4. Current Consumption

The information will be added in the future version of this document.

6.5. RF Output Power

The following table shows the RF output power of BG96 module.

Table 31: RF Output Power

Frequency	Max.	Min.
LTE-FDD B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/B26/B28	23dBm \pm 2.7dB	TBD
LTE-TDD B39	23dBm \pm 2.7dB	<-44dBm
GSM850/GSM900	33dBm \pm 2dB	5dBm \pm 5dB
DCS1800/PCS1900	30dBm \pm 2dB	0dBm \pm 5dB
GSM850/GSM900 (8-PSK)	27dBm \pm 3dB	5dBm \pm 5dB
DCS1800/PCS1900 (8-PSK)	26dBm \pm 3dB	0dBm \pm 5dB

6.6. RF Receiving Sensitivity

The following table shows the conducted RF receiving sensitivity of BG96 module.

Table 32: BG96 Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SISO	3GPP
LTE-FDD B1	TBD	Not Supported	TBD	-102.7dBm
LTE-FDD B2	TBD	Not Supported	TBD	-100.3dBm
LTE-FDD B3	TBD	Not Supported	TBD	-99.3dBm
LTE-FDD B4	TBD	Not Supported	TBD	-102.3dBm
LTE-FDD B5	TBD	Not Supported	TBD	-100.8dBm
LTE-FDD B8	TBD	Not Supported	TBD	-99.8dBm
LTE-FDD B12	TBD	Not Supported	TBD	-99.3dBm
LTE-FDD B13	TBD	Not Supported	TBD	-99.3dBm
LTE-FDD B18	TBD	Not Supported	TBD	-102.3dBm
LTE-FDD B19	TBD	Not Supported	TBD	-102.3dBm
LTE-FDD B20	TBD	Not Supported	TBD	-99.8dBm

LTE-FDD B26	TBD	Not Supported	TBD	-100.3dBm
LTE-FDD B28	TBD	Not Supported	TBD	-100.8dBm
LTE-TDD B39	TBD	Not Supported	TBD	-103dBm
GSM850/GSM900	TBD	Not Supported	TBD	-102.4dBm
DCS1800/PCS1900	TBD	Not Supported	TBD	-102.4dBm

6.7. Electrostatic Discharge

The information will be added in the future version of this document.

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7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm.

7.1. Mechanical Dimensions of the Module

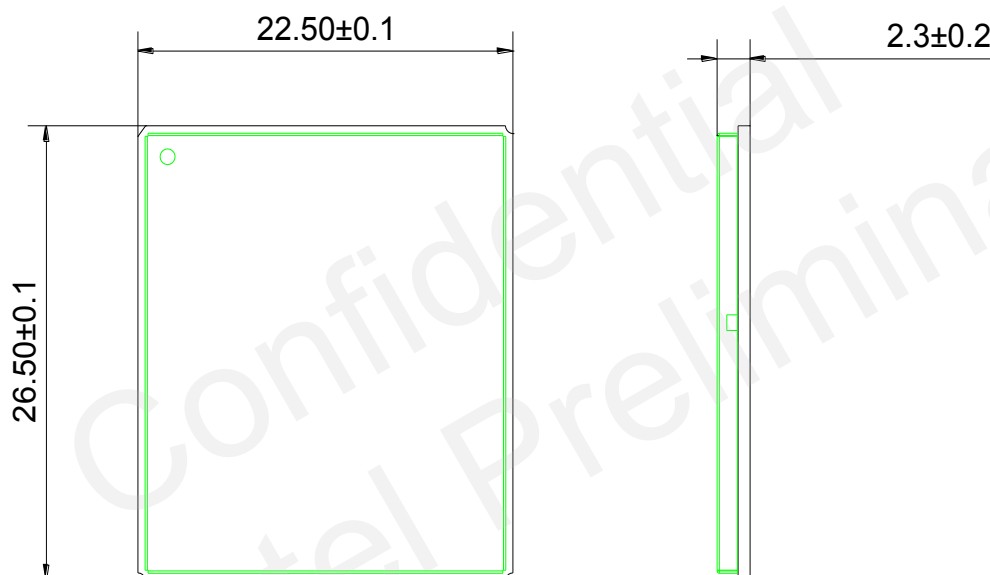
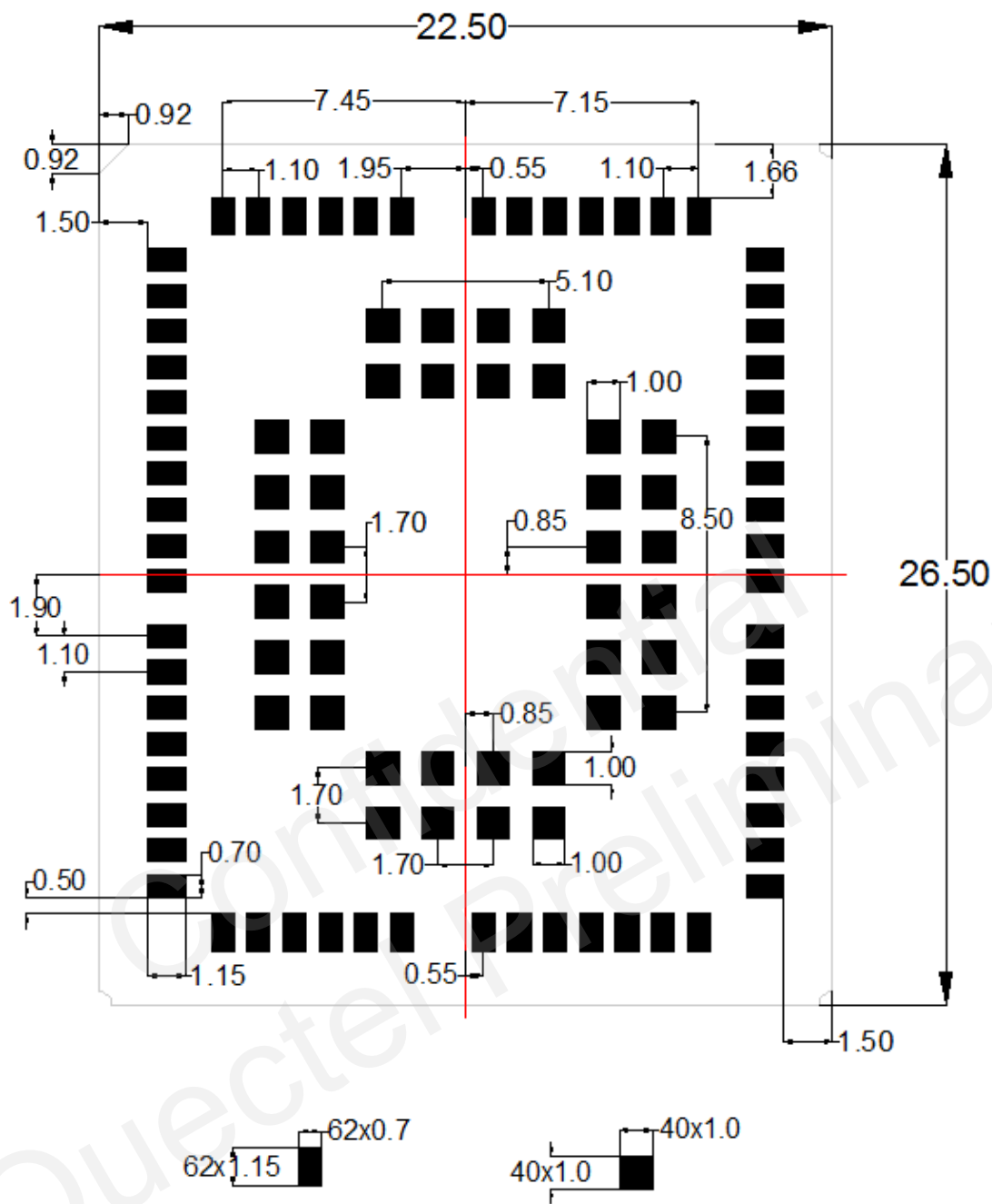


Figure 33: Module Top and Side Dimensions



7.2. Recommended Footprint

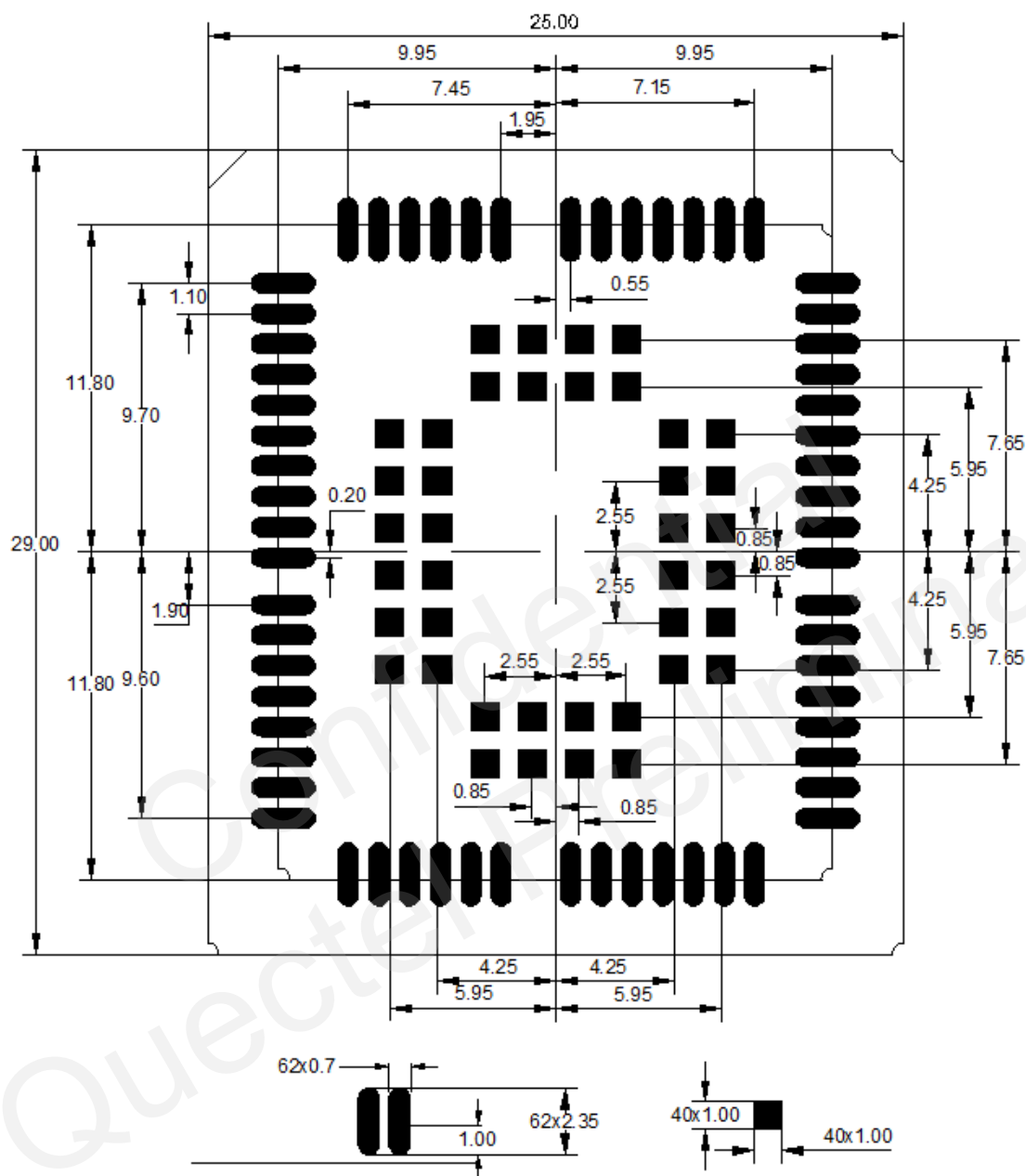


Figure 35: Recommended Footprint (Top View)

NOTE

For easy maintenance of the module, please keep about 3mm between the module and other components in the host PCB.

7.3. Design Effect Drawings of the Module



Figure 36: Top View of the Module

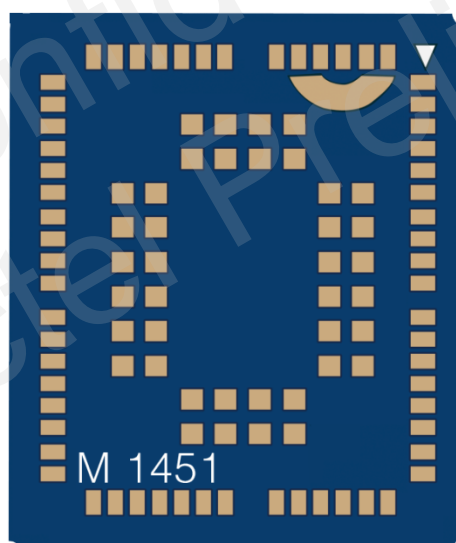


Figure 37: Bottom View of the Module

NOTE

These are design effect drawings of BG96 module. For more accurate pictures, please refer to the module that you get from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

BG96 is stored in a vacuum-sealed bag. The storage restrictions are shown as below.

1. Shelf life in the vacuum-sealed bag: 12 months at <40°C/90%RH.
2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:
 - Mounted within 72 hours at the factory environment of ≤30°C/60%RH.
 - Stored at <10%RH.
3. Devices require baking before mounting, if any circumstance below occurs.
 - When the ambient temperature is 23°C±5°C and the humidity indication card shows the humidity is >10% before opening the vacuum-sealed bag.
 - Device mounting cannot be finished within 72 hours at factory conditions of ≤30°C/60%
4. If baking is required, devices may be baked for 48 hours at 125°C±5°C.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (125°C) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly

so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18mm. For more details, please refer to **document [5]**.

It is suggested that the peak reflow temperature is 235~245°C (for SnAg3.0Cu0.5 alloy). The absolute max reflow temperature is 260°C. To avoid damage to the module caused by repeated heating, it is suggested that the module should be mounted after reflow soldering for the other side of PCB has been completed. Recommended reflow soldering thermal profile is shown below.

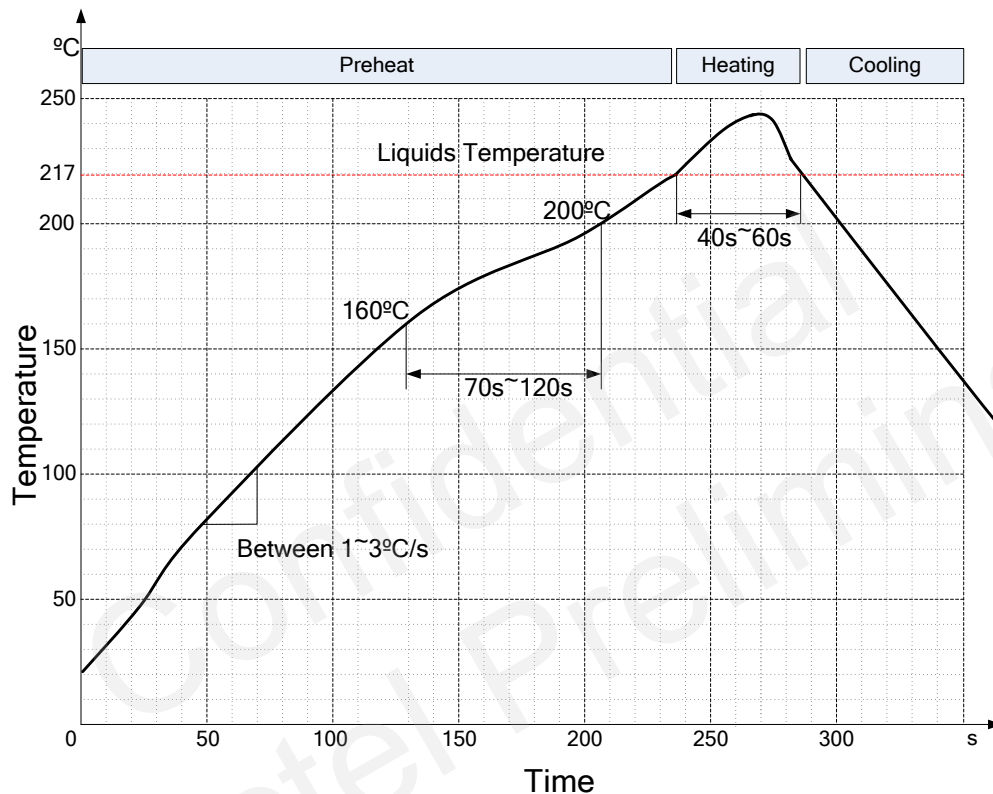


Figure 38: Reflow Soldering Thermal Profile

NOTE

During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module label with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc.

8.3. Packaging

The information will be added in the future version of this document.

9 Appendix A References

Table 33: Related Documents

SN	Document Name	Remark
[1]	Quectel_BG96_Power_Management_Application_Note	BG96 Power Management Application Note
[2]	Quectel_BG96_AT_Commands_Manual	BG96 AT Commands Manual
[3]	Quectel_BG96_GNSS_AT_Commands_Manual	BG96 GNSS AT Commands Manual
[4]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[5]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide

Table 34: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DC-HSPA+	Dual-carrier High Speed Packet Access
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate

ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station (GSM engine)
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive

SISO	Single Input Single Output
SMS	Short Message Service
TDD	Time Division Duplexing
TX	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
V _{max}	Maximum Voltage Value
V _{norm}	Normal Voltage Value
V _{min}	Minimum Voltage Value
V _{IHmax}	Maximum Input High Level Voltage Value
V _{IHmin}	Minimum Input High Level Voltage Value
V _{ILmax}	Maximum Input Low Level Voltage Value
V _{ILmin}	Minimum Input Low Level Voltage Value
V _I max	Absolute Maximum Input Voltage Value
V _I min	Absolute Minimum Input Voltage Value
V _{OHmax}	Maximum Output High Level Voltage Value
V _{OHmin}	Minimum Output High Level Voltage Value
V _{OLmax}	Maximum Output Low Level Voltage Value
V _{OLmin}	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

10 Appendix B GPRS Coding Schemes

Table 35: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

11 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 36: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5

12 Appendix D EDGE Modulation and Coding Schemes

Table 37: EDGE Modulation and Coding Schemes

Coding Schemes	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2:	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3:	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4:	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps