Jeffrey Wong

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Profile

First Year PhD student in Computer Engineering with prior experience in software/digital system design.

Experience

Terra (YC W21) **April 2023 – Sept. 2023**
Full-stack Engineer *London, UK*

- Led the full development lifecycle of the Graph API project, from inception to a successful launch, including the creation of the product and its associated SDK packages.
- Contributed to the expansion of the Terra Flash API to facilitate additional integrations. Involved in the maintenance of all Terra products, including Terra API, Python SDK, JavaScript SDK, and Terra webpages.
- Designed and developed Terra's mobile app, providing developers with an entry point for Terra integration.

DeepWok Lab, Imperial College London **May 2023 – Present**
Undergraduate Researcher *London, UK*

- Participated in developing the quantization transformation on the fx_graph within MASE to study the trade-offs involving mix-quantization schemes in a model and enabling further exploration of these trade-offs for users with a search.
- Implemented binarization linear and convolutional layer in Verilog and developed the related testbench with cocotb.
- Ported the LogicNets and LUTNet software stimulation to MASE and their related training workflow.
- Automating the generation of LogicNets and LUTNet hardware based on user configuration.

System and Circuit research group, Imperial College London **July 2022 – Sept. 2022**
Undergraduate Researcher *London, UK*

- Developed a Yolov3 model in TensorFlow with LUTNet, incorporating ReBNet as the Yolov3 backbone classifier, and devised a training scheme for rapid convergence.
- Investigated ways to boost software model accuracy, such as using transfer learning, regularizers, LUTNet pruning, and varying parameter initialization methods.
- Gained firsthand experience in FPGA neural network hardware design and testbench development in Vivado HLS and Csim tools.

Education

Imperial College London **Sep. 2024 – June 2028**
PhD. Electronic and Electrical Engineering *London, UK*

- Research focuses on intersections between hardware, algorithms, and security in the Machine Learning world.

Imperial College London **Sep. 2020 – June 2024**
MEng. Electronic and Information Engineering *London, UK*

- Achieved a 1st Class honor.
- Modules include: Advanced computer architecture, digital system design, compiler and verification technology.
- 2022 Head of Department's Prize for the top 2 highest performance groups in Second Year Final Project.
- Undergraduate Teaching Assistant for Instructure architecture and compiler; Advanced Deep learning system; Peer Tutor for Digital electronic and architecture modules

Majestic International College **Sep. 2017 – June 2020**
Cambridge Alevel *Guangdong, China*

- Mathematics (A*), Physics (A*), Chemistry (A*), Chinese (A*), Further Mathematics (A*)
- Achiever Scholarship and certificate of distinction winner.

Skills

Computer Languages: Python, C/C++, C#/F#, Typescript, SQL, Verilog, System Verilog, Swift
Engineering software: Intel Quartus, Xilinx Vivado HLS
Technologies/Frameworks: Linux, NextJS13, Flutter, React Native
Languages: Proficient in English, Mandarin, Cantonese

Projects

Multi-Precision, Arithmetic type Systolic Array-Based Accelerator | *Software-Hardware co-optimisation* **Present**

- Develop a systolic array-based accelerator for convolutional neural networks using multi-precision and different arithmetic types and its compiler using MLIR
- Investigate the accuracy and performance trade-off with intra-layer mix-precision operation

Digital System Design | *Intel Quartus, Verilog, FPGA* **Spring 2023**

- Designed a custom hardware accelerator for cordic operation that optimized the critical path through an analysis of the fix-point representation format of the domain and range, achieving an 805x speed improvement over pure software solutions.
- Conducted software code optimisation and hardware latency/throughput optimization methods optimisation such as word length analysis, and balancing pipeline stages, cache configuration and clock rate analysis.
- Achieved 83% as the overall marks

Mars Rover Design Project | *SystemVerilog, C++, Python, Intel Quartus, Computer vision, FPGA* **Summer 2022**

- Created a high-accuracy FPGA algorithm with minimal memory usage for real-time object detection and dimensional positioning of the rover using statistical pixel data
- Implemented and assessed the effectiveness of image processing filters in reducing noise and detecting edges.
- Designed solutions for obstacle avoidance and position error correction using data from ToF and ultrasonic sensors.
- Implemented A* algorithm on ESP32 and integrated all subsystems with suitable communication peripherals.
- Won Head of Department's Prize

Information Processing | *Verilog, Unity, C++, signal processing, C#, FPGA* **Spring 2022**

- Conceived and implemented the whole gaming logic on Unity with C# and multi-player solutions.
- Diagnosed and transformed FPGA's accelerometer data into direct gaming input using self-design filters on NIOS2 softcore in C.
- Designed solutions for obstacle avoidance and position error correction using data from ToF and ultrasonic sensors.
- Enabled communication between FPGA and Unity with different network protocols.
- Received group mark of A+

C Compiler | *C++, Compiler, IR* **Spring 2022**

- Gained hands-on experience on developing a C (C90) compiler & testbench supporting basic to advanced features such as various pointer type arithmetic, array arithmetic, and struct a sample banking transaction system using Java to simulate the common functions of using a bank account.
- Created a dynamic allocator for managing stack storage for memory optimization.
- Received top 10% marks of the department.

CPU Design Verilog | *Computer architecture, Verilog* **Spring 2021**

- Responsible for the whole CPU development from the concept through implementation with System Verilog.
- Achieved overall 98% of CPU accuracy on MIPS instruction

MU0 ARM CPU | *Computer architecture, Verilog* **Summer 2020**

- Led a team of 3 to the 1st class grade (81%). Developed an MU0 ARM architecture CPU in digital electronics design tool ISSIE supporting UART, Floating-point arithmetic, and Dual Core from scratch.

Issie development | *F#, functional programming* **spring 2023**

- Developed an algorithm to enable seamless snapping between multiple components and wires in Issie.
- Gained first-hand experience in functional programming development.

Volunteering & Interests

Teaching Assistant for Advanced Deep Learning System, Imperial College London **Present**

- Run weekly labs and problem classes guiding students with coursework and assignments

Teaching Assistant for Instruction Architecture and Compiler, Imperial College London **Spring 2023**

- Run weekly labs and problem classes guiding students with coursework and assignments

Peer Tutor for Digital electronic and architecture, Imperial College London **Present**

- Provided one-off tutorial to first year students who are struggling with a DECA.

Teaching Assistant, CamExpress, Educational Information Consultancy Co, Ltd (JTE) **Summer 2020**

- Run daily tutorials and mock interviews to help students improve their communication skills, physics, and math.

Treasurer Assistant, Imperial Chinese Students and Scholars Associations **Spring 2020 - 2022**

- Analyzed and drafted budgets for the activities under society.
- Started a database project to store past expenses of active accounts for future reference.

Experience Manager, AIESEC **Spring 2022 - 2023**

- Responsible for the experience the Exchange Participant has during his/her engagement with AIESEC.

Hack Cambridge Atlas **Winter 2020**

- Developed a web application prototype that could predict the main idea from a live speech with Django and React

1st Runner Up Winner in The Challenge Room X Hackspace **Winter 2020**

- A competition of logic, powers of deduction, and reasoning organized by The Imperial College Advanced Hackspace.