Queen Mary
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Science and Engineering

EBU4202: Digital Circuit Design
Hazards and Glitches

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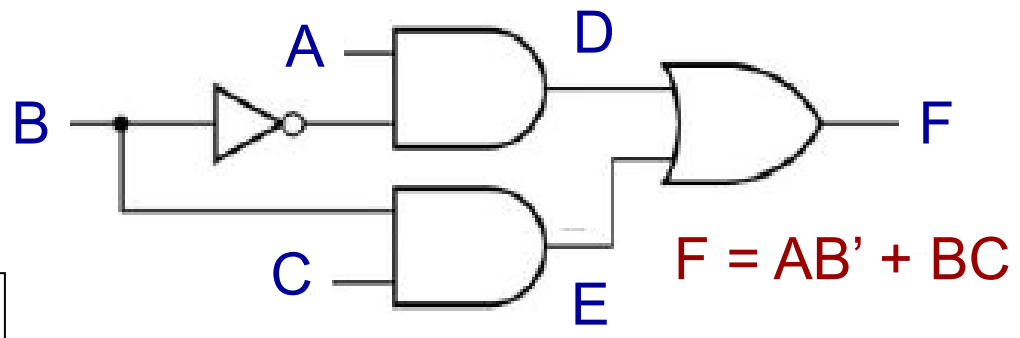
Timing Hazards and Output Glitches

- *Output glitch*: A momentary unexpected output change (short pulse) when an input changes; usually caused by gate propagation delays.
- *Hazards*: A timing hazard exists in a combinational circuit when it produces an *output glitch* when one or more inputs change.
  - Static Hazards (*static-1* and *static-0*): when 1 input variable changes, the output changes momentarily before stabilising on the correct value.
    - Can usually be fixed by adding redundant logic
  - Dynamic Hazards: possibility of an output changing more than once as a result of a single input change.

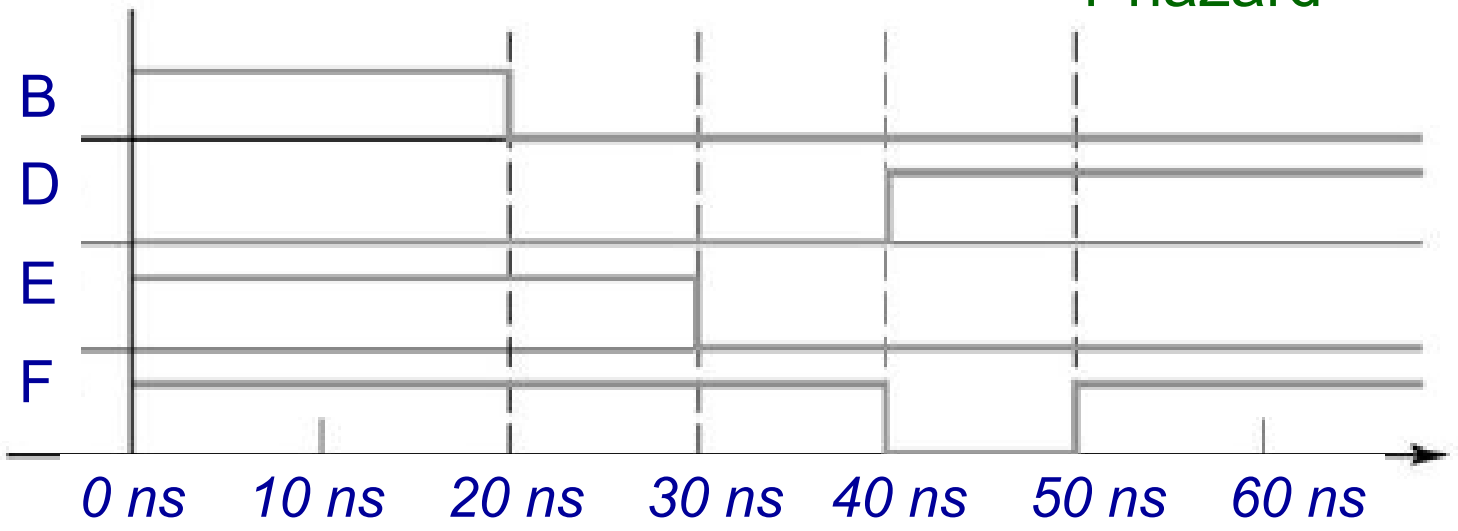
Timing Hazards and Output Glitches

- Example of *static-1 hazard*



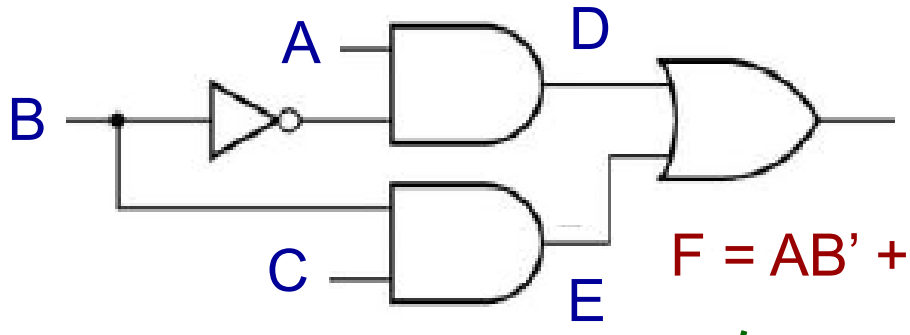
A \ BC	00	01	11	10
0	0	0	1	0
1	1	1	1	0

1-hazard



Timing Hazards and Output Glitches

- Example of *static-1 hazard (cont.)*:

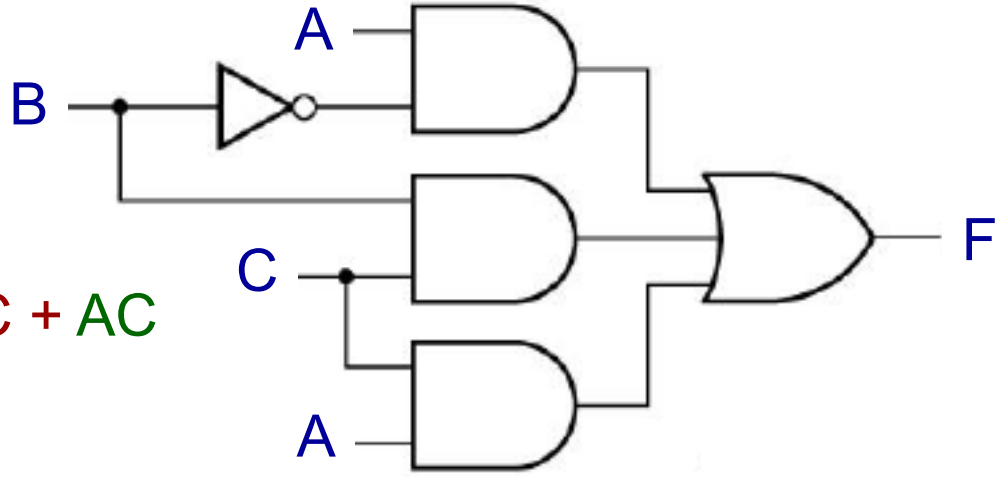


F = AB’ + BC

A \ BC	00	01	11	10
0	0	0	1	0
1	1	1	1	0

removing the *static-1 hazard*

F = AB’ + BC + AC



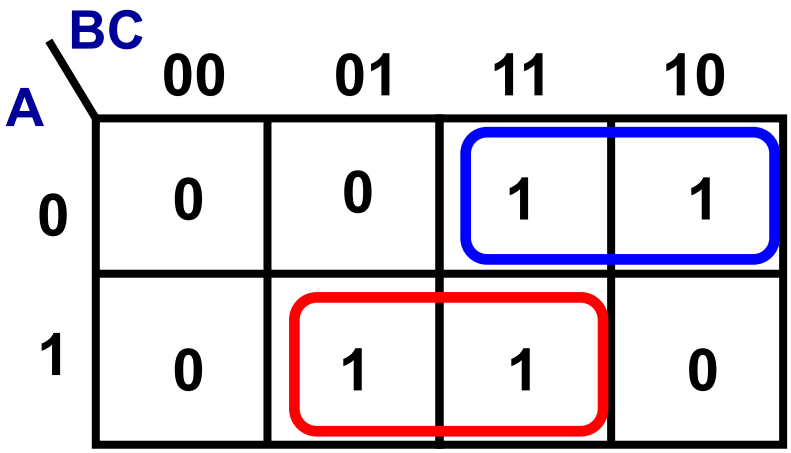
Static Hazards

- A **static-1 hazard** is a pair of input combinations that: (i) differ in only one input variable and (ii) both give a 1 output; such that it is possible for a momentary 0 output to occur during a transition in the differing input variable.

- A **static-0 hazard** is a pair of input combinations that: (i) differ in only one input variable and (ii) both give a 0 output; such that it is possible for a momentary 1 output to occur during a transition in the differing input variable.

Timing Hazards

Question: Is there any static hazard on the combinational circuit shown in the Karnaugh Maps? How can we eliminate this?



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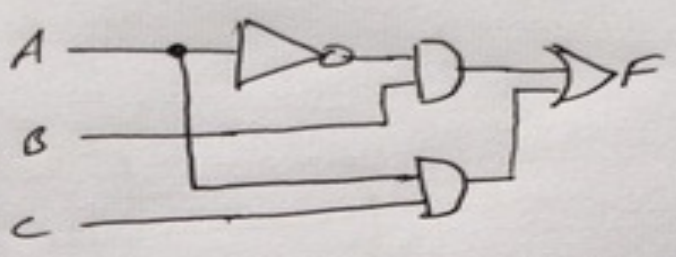
Timing Hazards

$F = A'.B + A.C$



A \ BC	00	01	11	10
0	0	0	1	1
1	0	1	1	0

F

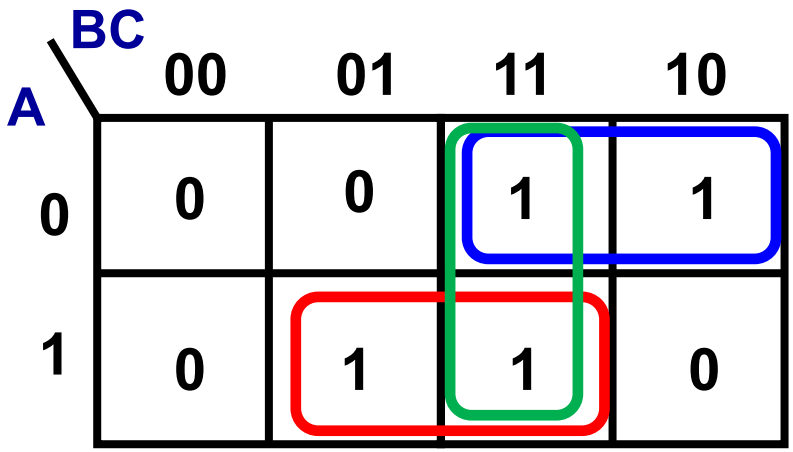
STATIC – 1 HAZARD ('RACE' HAZARD)

IF ONE OF THE AND GATE OUTPUTS GOES TO 0 BEFORE THE OTHER.

Timing Hazards

Is there any static hazard on the combinational circuit shown in the Karnaugh Maps? How can we eliminate this?

Answer: add a redundant group:



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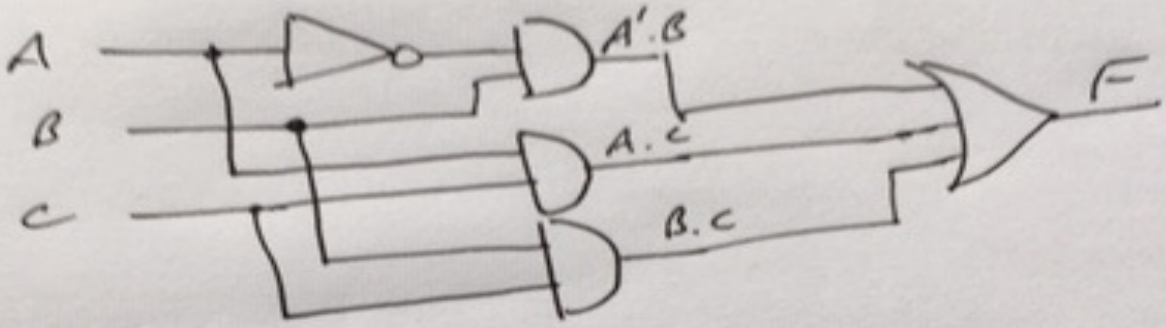
Timing Hazards

$$F = A'.B + A.C + B.C$$



STATIC – 1 HAZARD ELIMINATED

A \ BC	00	01	11	10
0	0	0	1	1
1	0	1	1	0

F

Timing Hazards

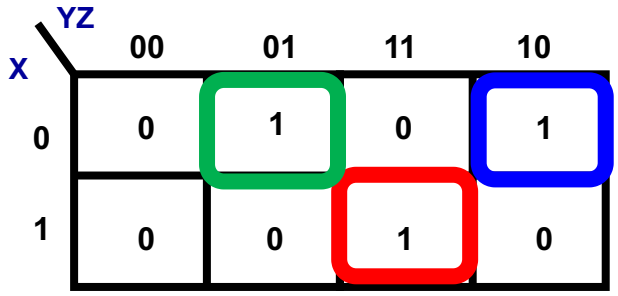
Example: F = X'Y'Z + X'YZ' + XYZ = (X ⊕ Y)'.Z + (X + Z)'.Y

Three input combinations give output 1.

XYZ = 001

XYZ = 010

XYZ = 111



If we investigate any two input combinations, we see that there are two variable changes. So, no Static-1 Hazard.

But according to the static-0 definition, there is a possibility to exist a Static-0 hazard (for input combinations XYZ = 000, 100). However, a properly designed two-level SoPs (AND-OR) circuit has no Static-0 hazard. You can draw the corresponding timing diagram for both circuits and check if there is any hazard.

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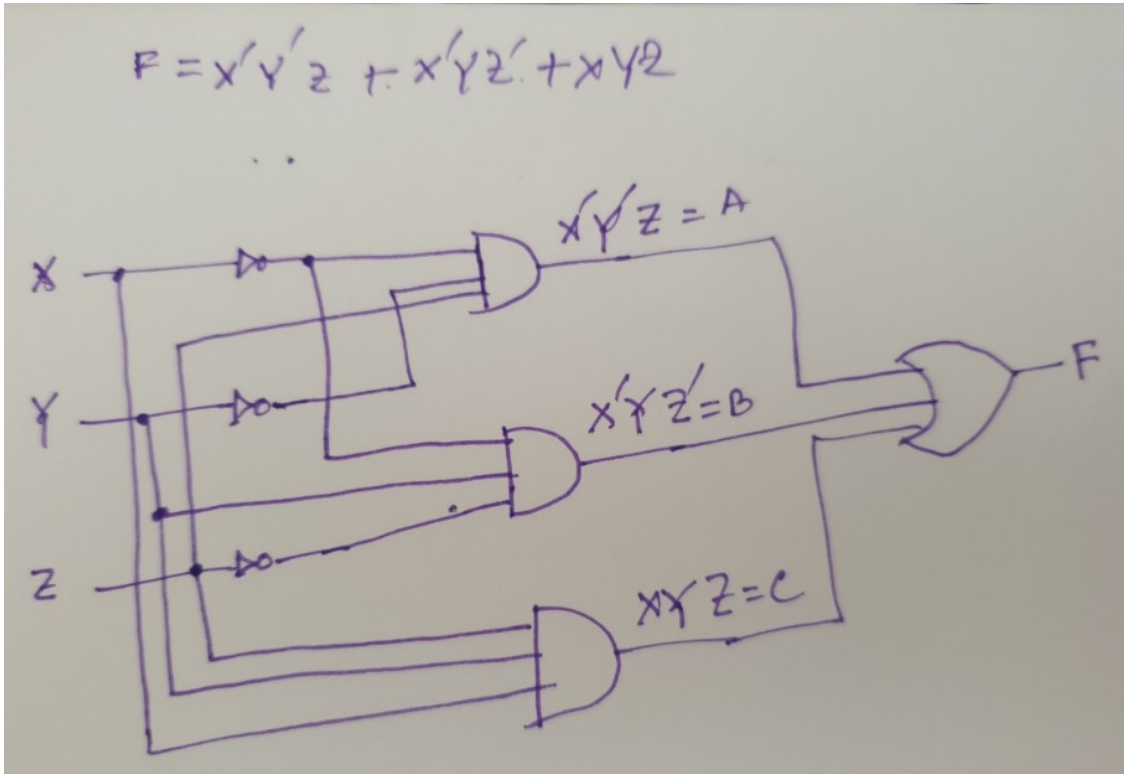
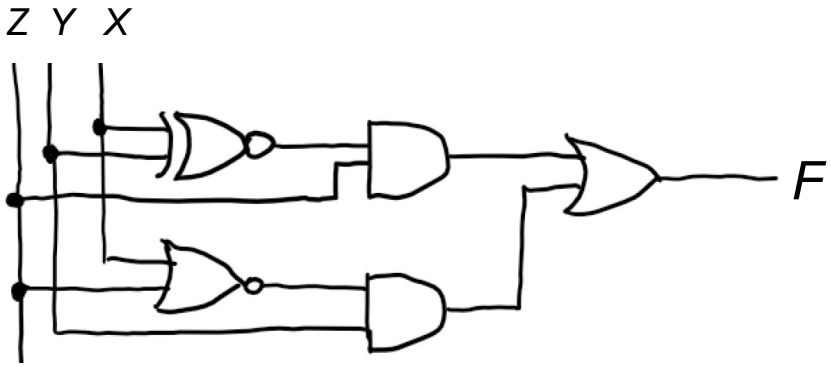
Timing Hazards





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