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LABORATORY REPORT

Digital Circuit Design

Introduction to Design using VHDL

INTRODUCTORY SUMMARY

Recently, I tried to use a powerful software-VHDL to design digital circuit in the lab. The aims of this Lab Session are to learn how to use VHDL and Modalism (an Image processing software) to design and simulate some basic logic circuits, namely: a NAND gate and three types of Adders (Half, Full and Parallel).

In order to have a better comprehension of VHDL codes and logic circuit designing, I used VHDL to test and evaluate some basic logic circuit, and collected the output image to verify whether the procedure codes work or not.

LAB MATERIALS

This lab analysis relies on two software, VHDL and Modalism. VHDL is a software that use its unique programing codes to express logic circuit, and Modalism is to convert those digital signal into visible image.

LAB PROCEDURE

After installing VHDL and Modalism and learning some VHDL programing method, our specific lab procedure consisted of these following steps:

Step 1

The first stage in the design of our circuits is to create one of the most basic components; this is the NAND gate. In order to do this, I used two tools:

1. A VHDL tool called “Xilinx Project Navigator”.
2. A simulation environment for verifying the source code and timing models of my designs.

By using Xilinx Project Navigator, I create a new project named “LAB1” to design and test the digital circuit.

Step 2

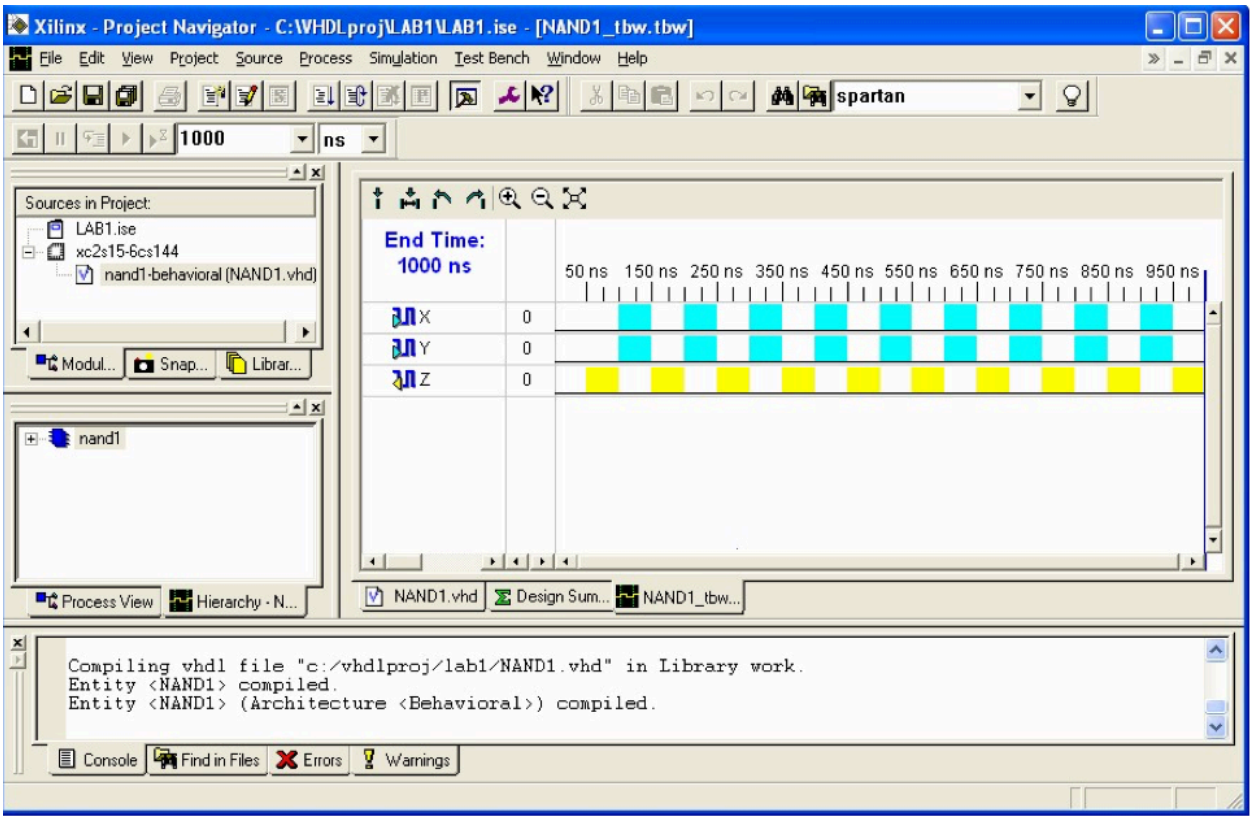
After preparation, I designed a NAND digital circuit by using following code:

Code:

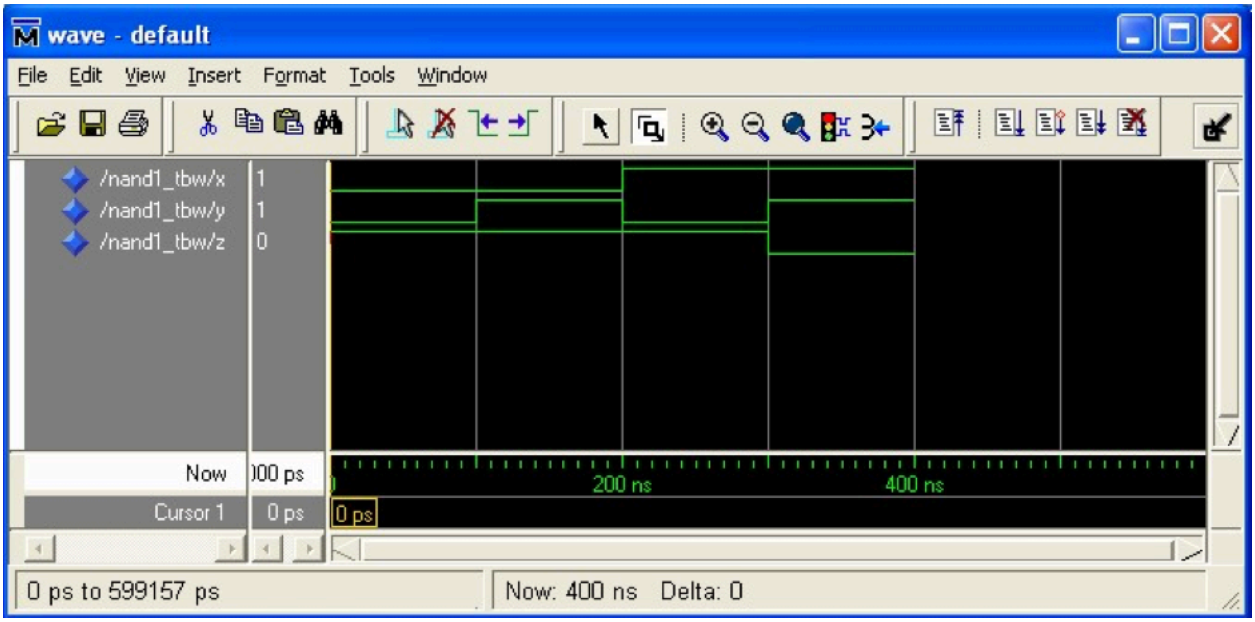
```
Library IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.SED_LOGIC_UNSIGNED.ALL;
```

```
ENTITY NAND IS

PORT (X, Y:IN STD_LOGIV:

Z:OUT STD_LOGIC);

END ENTITY NAND;

ARCHITECTURE ART OF NAND IS

BEGIN

Z<=X NAND Y;

END ART;
```

Then I created the test bench and get the waveform of this circuit as follows:



After this, I simulated this circuit design using Modalism and got the output waveform of NAND gates like this:



Step 3

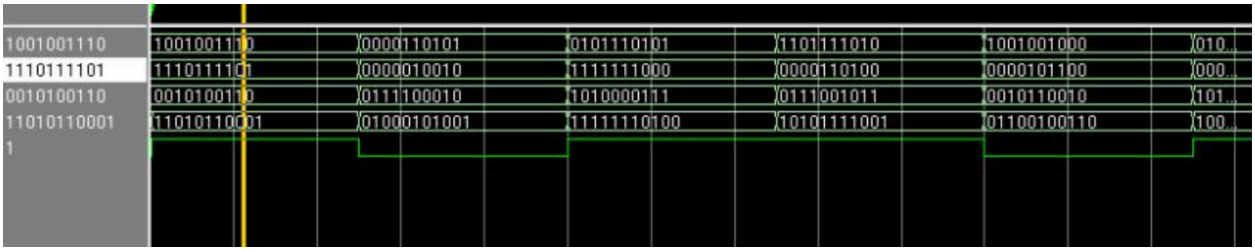
The next stage of the design consists of using our NAND gate design to make a Half Adder. In order to do this, I created a Half Adder entity and architecture pair that calls the NAND design. Next, I am going to use our Half Adder design to create a Full Adder, this will take full advantage of VHDL's hierarchical nature as we are using one of our designs in the formation of another.

Code：

```
Entity half adder is
PORT (a, b: IN STD_LOGIC; CO, SO: OUT STD_LOGIC);
END HALFADDER;
```

```
BEGIN
SO<= ((a NAND b) NAND a) NAND ((a NAND b) NAND b);
CO<= a and b;
End behavioral;
```

After complied these codes and used Modelsim, I got the result like this, which was in accordance to the truth table:



PROBLEMS ENCOUNTERED

Since this was my frist time using VHDL and Modelsim, I got some troubles in creating the image of the output waveform. Though failed several times to transform the codes into the images because of the wrong operation, fountunately, with the help of teacher, I overcame the difficullties finally and got the right image. I also encountered some problems in programing, VHDL is absolutely a new computer language for me , and it's not so easy understanding.

COCLUSION

Through this lab of Digital Circuit Design, I learned some basic knowledge of VHDL and Modalism. With the help of these software, I designed and simulated some basic logic circuits successfully.

What's more, I not only improved my ability of programing, but also learned the basic skills of writing an informer report. Since this was my first time writing an informer report, I will appreciate it very much if you could take your precious time to point out some deficiencies on my report.

Sincerely,

Liu Xiangchong