SOLUTIONS

Module:	Digital Circuit Design		
Module Code	EBU4202	Paper	B
Time allowed	2hrs	Filename	**Solutions_2021_EBU4202_B**
Rubric	ANSWER ALL FOUR QUESTIONS		
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Question 1

a) Fill in the table by putting the correct numbers in different bases by doing suitable conversion. Write your answers in the table directly.
Show THREE fractional places for decimal and binary value. [6 marks]

Decimal	Binary	Octal	Hexadecimal
160.430	10100000.011	240.3	A0.6
577.625	1001000001.101	1101.5	241.A

Each answer has one marks.

b) Figure Q1b) shows the IEEE-754 floating point format.

Sign bit s	8-bit exponent e	23-bit mantissa f

Normal Value = (-1)s 1.f * 2e-127

Figure Q1b)

Express the decimal number - 0.43 in this format to 6 fractional places. [6 marks]

Answer:

Convert -0.43 to binary:

$0.43 \times 2 = 0.86$
$0.86 \times 2 = 1.72$
$0.72 \times 2 = 1.44$
$0.44 \times 2 = 0.88$
$0.88 \times 2 = 1.76$
$0.76 \times 2 = 1.52$

[2 marks]

So $-0.43_{10} = -0.011011_2$ to 6 fractional places

$= -1.1011 \times 2^{-2}$
$= -1.1011 \times 2^{125-127}$
$= (-1)^1 \times 1.1011 \times 2^{1111101_2-127}$

[2 marks]

Therefore floating point format is: 1/01111101/10110000000000000000000 [2 marks]

c) Combinational logic circuit was designed, such that its functionality can be described by the Switching Algebra equation: $F(X, Y, Z) = XY'Z' + YZ + X'Y'Z$. Answer the following questions:

i) Write the Truth Table for this circuit.

[3 marks]

ii) Plot its logic circuit diagram.

[3 marks]

iii) Derive the product of maxterms expression that describes it.

[2 marks]

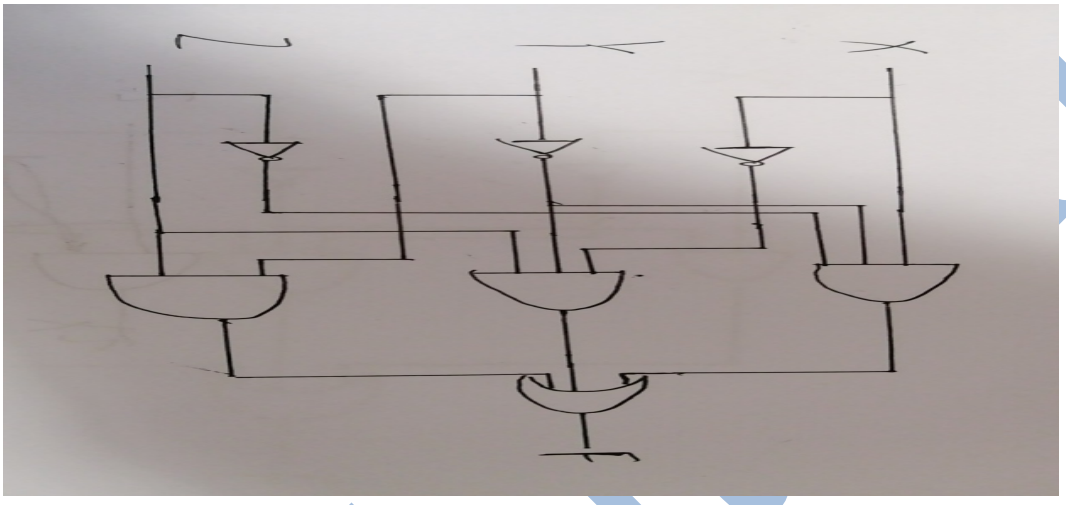
Answer:

i) The truth table is:

X	Y	Z	XY'Z'	YZ	X'Y'Z	F
0	0	0	0	0	0	0
0	0	1	0	0	1	1
0	1	0	0	0	0	0
0	1	1	0	1	0	1
1	0	0	1	0	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	0	1	0	1

[3 marks]

ii) Logic circuit diagram is



[3 marks]

iii) The product of maxterms expression that describes it is $F(X,Y,Z)=\prod \mathrm{M}(0,2,5,6)$ or $F(X,Y,Z)=(X+Y+Z)(X+Y'+Z)(X'+Y+Z')(X'+Y'+Z)$.

[2 mark]

d) Using Switching Algebra theorems to simply
$\mathrm{F(A,B,C)} = \mathrm{AB} + \mathrm{AB'C} + (\mathrm{A} + \mathrm{B'})(\mathrm{A} + \mathrm{B'} + \mathrm{C})$.
Hint: Use Adsorption Theorem $X + X'Y = X + Y$ and the list of theorems given in the **Appendix.**
[5 marks]

Answer:

$\mathrm{F(A,B,C)} = \mathrm{AB} + \mathrm{AB'C} + (\mathrm{A} + \mathrm{B'})(\mathrm{A} + \mathrm{B'} + \mathrm{C})$

$= A(B + B'C) + A + B'$ [1 mark]

$= A(B + C) + A + B'$ [1 mark]

$= AB + AC + A + B'$ [1 mark]

$= AB + A + AC + A + B'$ [1 mark]

$= A(B + 1 + C + 1) + B'$

$= A + B'$ [1 mark]

Question 2

a) Let ABCD represent a 4 bit BCD number.

[15 marks]

i) Draw the truth table for a combinational logic circuit **that produces a '1' output when the input ABCD is an odd number or also when the number is 2**. The input combination 0000 is not allowed to occur.

(2 marks)

ii) Draw the Karnaugh map for this circuit.

(2 marks)

iii) From the Karnaugh map, determine a minimal expression for the output expressed in Sum of Product (SoP) form and in all NAND form.

(4 marks)

iv) Using a truth table, show the state of the output for each of the "**can't happen**" input states as a result of the minimisation.

(1 mark)

v) Draw the circuit diagrams for the minimal SoP and all NAND implementations of the function.

(4 marks)

vi) Does the circuit have a static hazard? Justify your answer.

(2 marks)

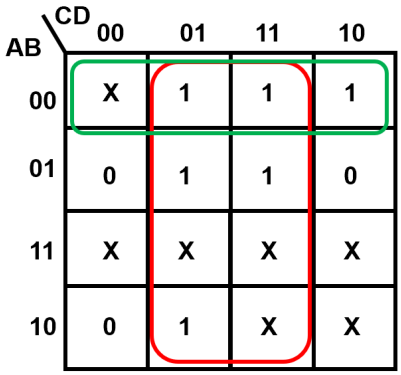
Solution:

i) The truth table is:

A	B	C	D	F(A,B,C,D)
0	0	0	0	X
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	X
1	0	1	1	X
1	1	0	0	X
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X

[2 marks for the correct truth table]

ii) The Karnaugh map is:



[2 marks]

iii) The minimal SoP expression is: F = A'B' + D [2 marks]

To find the all NAND expression of F, we apply De Morgan's theorem as:

F = A'B' + D

= ((A'B')')' + (D')'

= ((A'B')'.D')' [since X' + Y' = (X.Y)']

[2 marks for the correct answer]

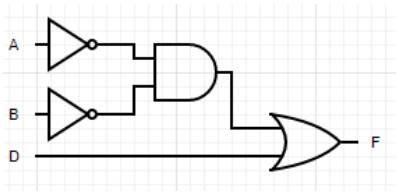
iv)

A	B	C	D	F(A,B,C,D)
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

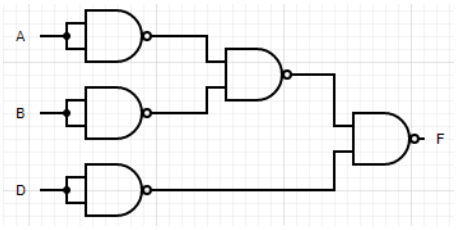
[1 mark]

v) The circuit diagrams are:

SoP:



All NAND gates:



[4 marks = 2 marks for each correct diagram]

vi) The circuit does not have a static hazard [1 mark] because the map groupings overlap [1 mark].

b) Minimize the following Boolean functions using Karnaugh Maps:

[6 marks]

i) $F(A,B,C) = \Sigma m(0,1,6,7) + \Sigma d(3,5)$

ii) $G(A,B,C) = \Sigma m(1,2,5,7) + \Sigma d(0,4,6)$

Solution:

i)

A \ BC	00	01	11	10
0	1	1	x	0
1	0	x	1	1

(1 mark for correctly drawing and entering minterms on the K-map)

F = AB + A'B'

(2 marks for correctly expressing the minimized expression)

ii)

A \ BC	00	01	11	10
0	x	1	0	1
1	x	1	1	x

(1 mark for correctly drawing and entering minterms on the K-map)

G = A + B' + C'
(2 marks for correctly expressing the minimized expression)

c) This question is about **Timing Hazards and Output Glitches**:

[4 marks]

i) What is a dynamic hazard? Do dynamic hazards occur in a properly designed two-level AND-OR or OR-AND circuit?

(2 marks)

ii) For the following logic expression, find all the static hazards in the corresponding two-level AND-OR or OR-AND circuit. Also, design a hazard-free circuit that realizes the same logic function:

$$F = AB' + B.C$$

(2 marks)

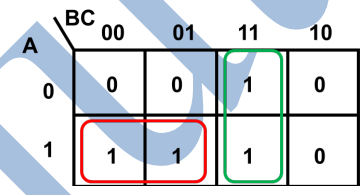
Solution:

i)

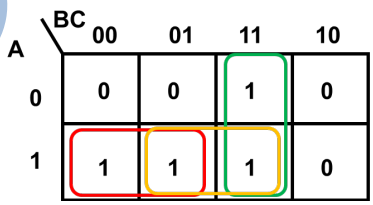
A dynamic hazard is the possibility of an output changing more than once as a result of a single input change. [1 mark]

No, dynamic hazards do not occur in a properly designed two-level AND-OR or OR-AND circuit. [1 mark]

ii) It is seen from the K-map that 101 to 111 change can cause a static-1 hazard [1 mark].



For a hazard-free circuit design, an extra product term is included to cover the hazardous inputs [1 mark].



[Note – showing Karnaugh map only also gets full marks]

Question 3

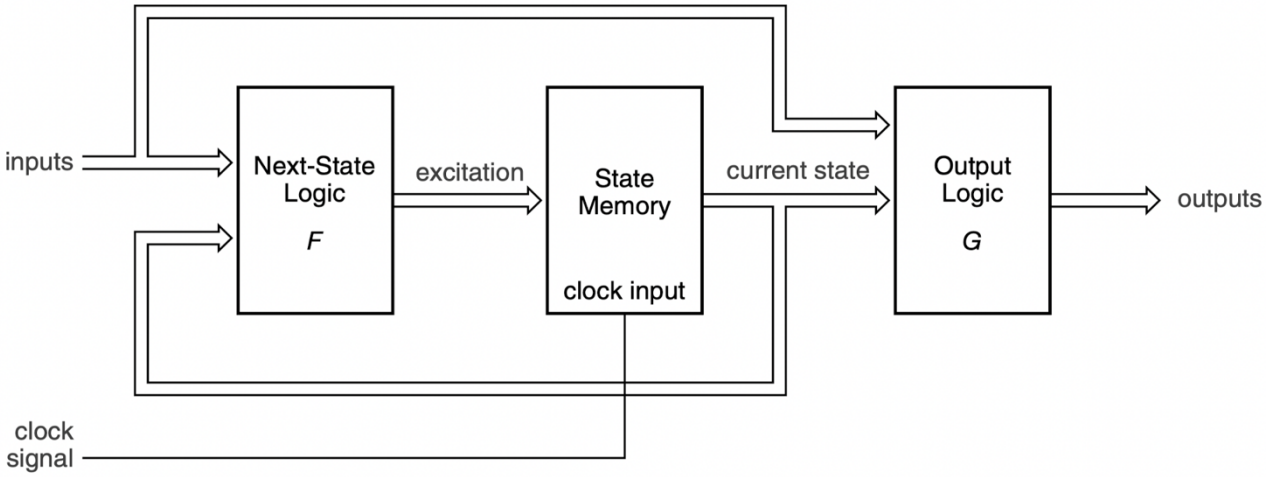
a) A Sequential Circuit requires feedback. [6 marks]

i) List the THREE equations that are necessary to allow a sequential circuit to be analysed.
(3 marks)

ii) Draw a general block diagram of a sequential circuit showing which part of the circuit these equations relate to.

(3 marks)

Answer: i) The three equations are:
excitation equations, characteristic equations, output equations [3 marks,1 mark each]



b) Figure Q3b is a sequential circuit.

Name the circuit and describe its behaviour. [4 marks]

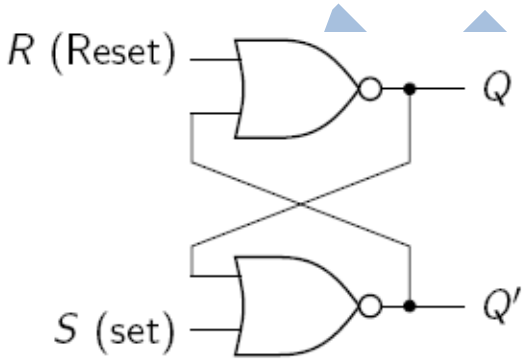


Figure 3b

Name the sequential circuit in Figure Q3b and describe its behaviour.

Figure 3b *represents an "SR latch" sequential circuit* ***[1 mark]****. In this type of latch, after either input is negated, the latch remains in the state that it was forced into* ***[1 mark]****; it behaves like a bistable element* ***[1 mark]****. In addition, the circuit goes into an indeterminate state after we use input* **`S = R = 1`** ***[1 mark]****.*

c) Design an autonomous sequential circuit using D-type bistables to continuously generate the following sequence:

100. 101, 111, 110, 010, 011, 001, 000. [15 marks]

i) Derive the Boolean logic functions that minimise the combinational logic. (9 marks)

ii) Draw the Circuit Diagram. (3 marks)

iii) Does your minimised circuit contain Hazards? (3 marks)

i) Complete a table of present and next states:

Present State			Next State		
Q_A	Q_B	Q_C	Q_A^*	Q_B^*	Q_C^*
1	0	0	1	0	1
1	0	1	1	1	1
1	1	1	1	1	0
1	1	0	0	1	0
0	1	0	0	1	1
0	1	1	0	0	1
0	0	1	0	0	0
0	0	0	1	0	0

For D bistables, the next output is the present input, so we can now draw a Karnaugh map for each next output in terms of the present state.
Group to minimise number of terms

Input Logic K-Map		Q_AQ_B			
		00	01	11	10
Q_C	0	1	0	0	1
	1	0	0	1	1

Q_A^*

$D_A = Q_B'Q_C' + Q_AQ_C$

Input Logic K-Map		Q_AQ_B			
		00	01	11	10
Q_C	0	0	1	1	0
	1	0	0	1	1

Q_B^*

$D_B = Q_BQ_C' + Q_AQ_C$

		Q_AQ_B			
		00	01	11	10
Q_C	0	0	1	0	1
	1	0	1	0	1

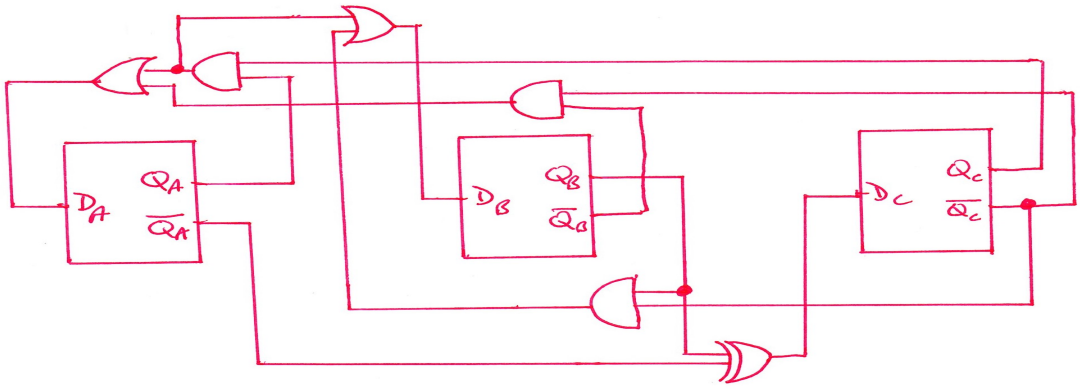
Q_C^*

$D_C = Q_A'Q_B + Q_AQ_B'$

[9 marks: 3 for next state table, 1 for each K-Map, 1 for each Boolean expression]

ii) Circuit diagram:

[3 marks: 1 for each input logic]



iii) Yes, D_A and D_B have static hazards. [3 marks, 1 for each statement]

Question 4

a) In the context of solid-state memory devices, explain what is meant by each of the following terms:

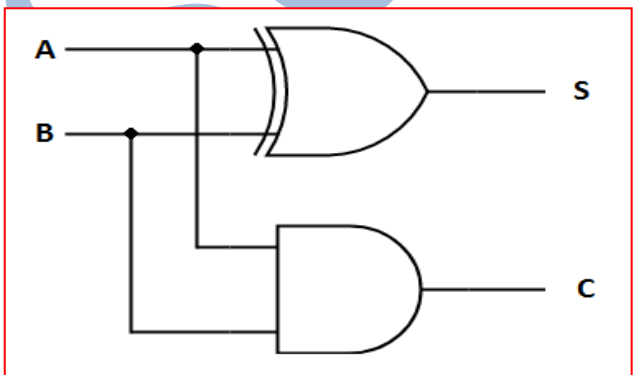
i) Volatile
ii) SRAM
iii) EPROM

[3 marks]

- Volatile memory loses its contents when the power is switched off. **[1 mark]**
- Static RAM uses transistors to store a single bit of information and does not need to be refreshed periodically. **[1 mark]**
- Erasable Programmable Read-Only Memory. It can be programmed only once and cannot be erased afterwards.. **[1 mark]**

b) Draw the gate logic diagram of a half adder and provide its truth table.

[5 marks]



$$S = XY + XY = X \oplus Y$$
$$C = XY$$

X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

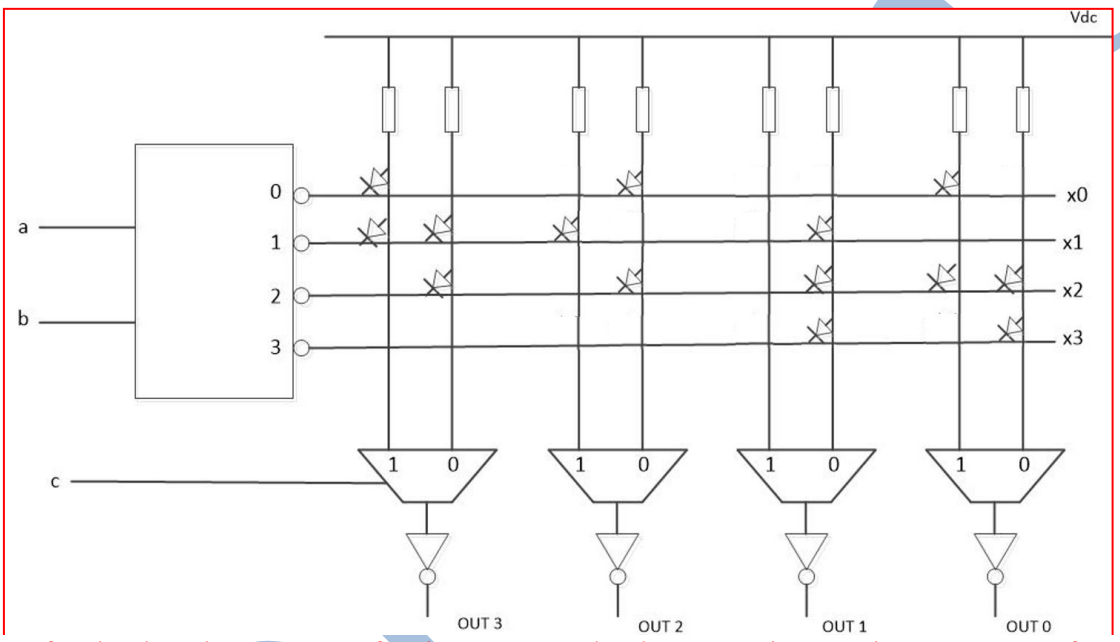
[3 marks for diagram with logical expression and **2 marks** for the truth table.**]**

c) Design an 8 x 4-bit read-only memory (ROM) circuit pre-programmed with the data shown in the table below. (Hint: diodes, decoder, multiplexer etc. are required in the ROM circuit).

[12 marks]

Address	Data (4-bit)
0	4
1	9
2	10
3	12
4	15
5	1
6	3
7	0

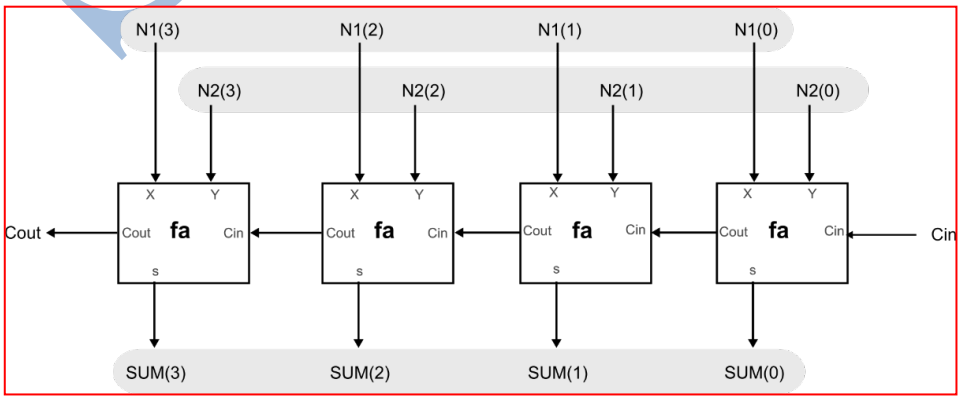
Table Q4c)



[**3 marks** for the decoder, **3 marks** for the MUX, and Vdc connections to those, **6 marks** for correct diode connections] (You can deduct 0.5 marks for each wrong placements of diodes).

d) Use a suitable diagram to demonstrate how a 4-bit parallel ripple adder can be used as an adder, where you want to perform (N1+N2) operation. Explain the mechanism in your own words.

[5 marks]



[3 marks]

The carry input to the least significant bit is normally set to 0 and the carry output of each full adder is connected to the carry input of the next most significant full adder. (Students can write in their own words) **[2 marks]**