Digital Circuit Design

Queen Mary University of London

Course Code: EBU4202

School of Electronic Engineering and Computer Science

Lab Sheet 3: Sequential Logic Circuits	Date: May 31, 2023
Student's Family Name, Given Name (pinyin):	Student's BUPT Number, Class Number:
Official Email:	Total Mark (out of **40**):

IMPORTANT:

(a) In advance of the lab session: Print this Lab Sheet, read it and complete all the indicated "Preparatory Work".
(b) On the day of the lab session : Ensure that you have your notes to hand (taken during **Lab Session 1**) about how to set up the *Test Bench*.
(c) Write all your answers on this Lab Sheet, where indicated.
(d) Use additional A4 sheets of paper if you require more space to write your answers, ensuring that the question numbers are indicated clearly.
(e) Before handing in your Lab Sheet, make sure that you fill in the Table above with your personal details, ***and*** staple any additional answer sheets (with your name written on them) together with this Lab Sheet.

1. Learning Objectives

In this set of experiments, you will study and build sequential digital circuits. These circuits have memory and include flip-flops, which are the basic building blocks of computer registers and memories. You will be looking at latches and flip-flops, as well as shift registers which are built from flip-flops.

Please note that all the circuits you build during this experiment will require the *Test Bench* previously described in **Lab Sheet 1**; you need to assemble this before you start your experiments.

2. Preparatory Work

It is essential to be well prepared before starting this Lab Session. Read the Lab Sheet thoroughly, do all the background design work for **Experiments 1** and **2**, and produce properly numbered circuit diagrams where indicated. You should do all the **Preparatory Work** before the Lab Session takes place.

Use your textbook and lecture slides to review what SR latches and JK flip-flops do and how they can be implemented using the combinational logic gates that you used previously. Then plan how you will build or investigate the circuits in **Experiments 1** through to **3**.

3. Logic Gates

You will be using the following TTL integrated circuits to build and investigate the sequential circuits described in this Lab Sheet:

- ✓ 2 x 7400 (labelled *HD74LS00P*) Quadruple 2-input NAND gates
- ✓ 1 x 7404 (labelled *HD74LS04P*) Hex inverters
- ✓ 1 x 7408 (labelled *HD74LS08P*) Quadruple 2-input AND gates
- ✓ 1 x 7474 (labelled *HD74LS74P*) Dual D type flip-flops
- ✓ 2 x 7476 (labelled *HD74LS76P*) Dual JK flip-flops with preset and clear

The pin-outs and schematic diagrams for these ICs can be found in the **Appendix** of this Lab Sheet. In addition, you also require a power supply unit and an oscillator with a TTL output (see **Figure 1**).

Figure 1 – Oscillator with TTL output[1].

4. Experiments

For the Characteristic Table of each latch/flip-flop, take the present state, **Qn**, of the output **Q**, to be an effective input to the following latches/flip-flops. Therefore e.g., the inputs to the first latch in this Lab Session are **Qn**, **S** and **R**, and the output is **Qn+1**, giving 8 lines in the Characteristic Table (see **Table 1**).

Inputs		*Current State*	*Next State*	**State Comment**
S R		**Qn**	**Qn+1**	
0 0		0	0	Hold
0 0		1	1	Hold
0 1		0	0	Reset
0 1		1	0	Reset
1 0		0	1	Set
1 0		1	1	Set
1 1		0	Oscillating	Invalid
1 1		1	Oscillating	Invalid

Table 1 – Characteristic Table of an SR latch.

[1] Please **note** that the picture of an oscillator in **Figure 1** is provided for illustration purposes only, as the oscillator available in your hardware lab may not look exactly like this (e.g., it may be from a different manufacturer).

EXPERIMENT 1 – SR Latches & D Latches

In this experiment, you will be studying and constructing three different types of latches: an SR latch, an SR latch with Control Input (*aka* Clocked SR latch) and a D latch (*aka* Clocked D latch).

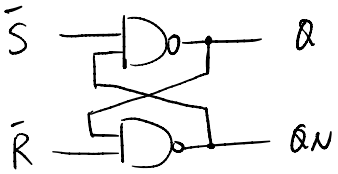
Question 4.1.1 [**1 Mark**] – (**Preparatory Work**) Write the Functional Table for an SR latch (using two NAND gates).

Answer to Question 4.1.1

Inputs		Outputs	
S_L	R_L	Q	Q_N
0	0	1	1
0	1	1	0
1	0	0	1
1	1	lastQ	lastQ_N

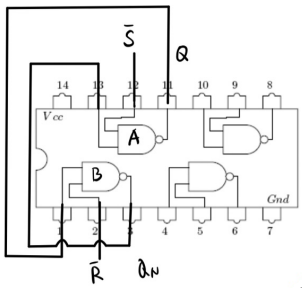
Question 4.1.2 [**2 Marks**] – (**Preparatory Work**) Draw a labelled circuit diagram of an SR latch using two NAND gates.

Answer to Question 4.1.2



Question 4.1.3 [**6 Marks**] – Study, construct and verify the operation of an SR latch (built using two NAND gates – see **Figure 4**), and then describe in your own words how an SR latch works. Your answer must also include a labelled schematic diagram of your SR latch. **Note**: Please make sure you indicate how different pins are connected. ✓

Answer to Question 4.1.3



$\bar{R}$ → 2 inputs of GateA : 3, 12

$\bar{S}$ → 12 inputs of GateB : 2, 12

Q → 11

Q_N → 3

when $\bar{S}=\bar{R}=1$, $Q^{n+1}=Q^n$ SR latch holds the original state

when $\bar{S}=0$, $\bar{R}=1$, $Q^{n+1}=1$ SR latch set to 1

when $\bar{R}=0$, $\bar{S}=1$, $Q^{n+1}=0$ SR latch reset to 0

when $\bar{S}=0$, $\bar{R}=0$, invalid inputs, oscillate.

truth

Question 4.1.4 [**2 Marks**] – (**Preparatory Work**) Write both the Characteristic Table and Functional Table for a clocked SR latch (using four NAND gates).

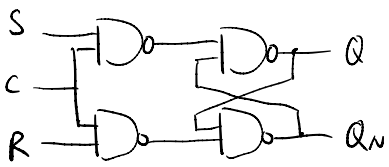
Answer to Question 4.1.4

S	R	C	Q^*
X	X	0	Q
0	0	1	Q
0	1	1	0
1	0	1	1
1	1	1	Invalid

S R C	Q^n	Q^{n+1}	State comment
X X 0	0	0	memory
X X 0	1	1	
0 0 1	0	0	memory
0 0 1	1	1	
0 1 1	0	0	reset
0 1 1	1	0	
1 0 1	0	1	set
1 0 1	1	1	
1 1 1	0	oscillate	X
1 1 1	1		

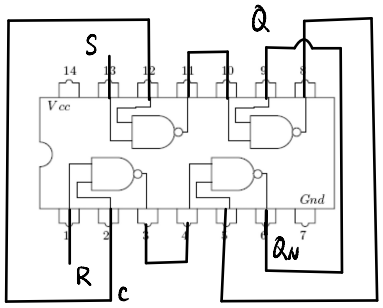
Question 4.1.5 [**2 Marks**] – (**Preparatory Work**) Draw a labelled circuit diagram of a clocked SR latch using four NAND gates.

Answer to Question 4.1.5



Question 4.1.6 [**6 Marks**] – Study, construct and verify the operation of a clocked SR latch (built using four NAND gates – see **Figure 4**), and then describe in your own words how a clocked SR latch works. Your answer must also include a labelled schematic diagram of your clocked SR latch. **Note**: Please make sure you indicate how different pins are connected.

Answer to Question 4.1.6



when $C = 0$ $Q^* = Q$.

when $C = 1$

$S = R = 0$ $Q^* = Q$

$S = 1, R = 0$ $Q^* = 1$ (set)

$S = 0, R = 1$ $Q^* = 0$ (reset)

$S = 1, R = 1$ Q^* Oscillating (Invalid)

S → 13

R → 1

C → 12, 2

S, R output 11, connected to 10

C, R output 3, connected to 4

5 is the output of 8

9 is the output of 6

Question 4.1.7 [**2 Marks**] – (**Preparatory Work**) Write both the Characteristic Table and Functional Table for a D latch.

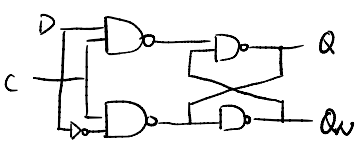
Answer to Question 4.1.7

C	D	Q	Q_N
0	x	lastQ	lastQN
1	1	1	0
1	0	0	1

C	D	Q^n	Q^{n+1}	state comment
0	x	0	0	memory
0	x	1	1	
1	0	0	0	reset
1	0	1	0	
1	1	0	1	set
1	1	1	1	

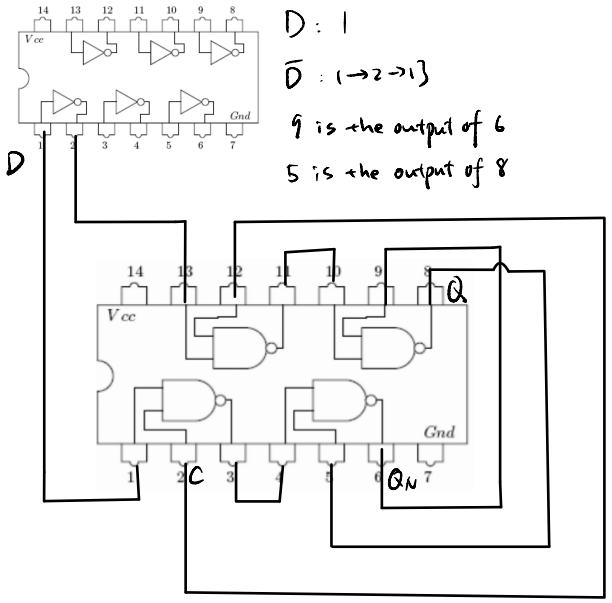
Question 4.1.8 [**2 Marks**] – (**Preparatory Work**) Draw a labelled circuit diagram of a D latch, formed by adding a NOT gate to a clocked SR latch.

Answer to Question 4.1.8



Question 4.1.9 [**6 Marks**] – Study, construct and verify the operation of a D latch (built by adding a NOT gate to a clocked SR latch – see **Figure 4** and **Figure 5**), and then describe in your own words how a D latch works. Your answer must also include a labelled schematic diagram of your D latch. **Note**: Please make sure you indicate how different pins are connected.

Answer to Question 4.1.9



when C = 0 $Q^* = Q$

when C = 1

D = 1 $Q^* = D = 1$ set

D = 0 $Q^* = D = 0$ reset

EXPERIMENT 2 – JK Flip-Flops

In this experiment, you will be studying and constructing a JK type Master-Slave Flip-Flop, using 7476 IC (see **Figure 8**). When building this flip-flop, please note the following:

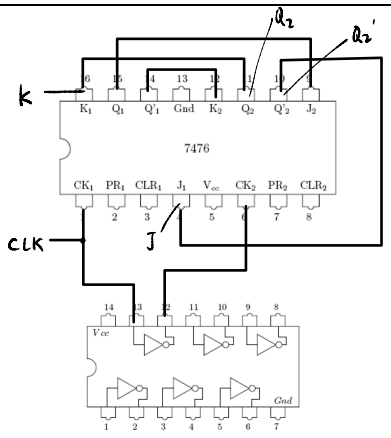
1. The **PRESETnot** (**P'**) and **CLEARnot** (**C'**) inputs enable the flip-flop's initial conditions to be established.
2. Both inputs **P'** and **C'** are active low, so that if **P'=0** and **C'=1**, then **Q=1**. However, if **P'=1** and **C'=0**, then **Q=0**.
3. For normal operation, set up your JK flip-flop so that **P'=C'=1**.

Question 4.2.1 [**3 Marks**] – (**Preparatory Work**) Describe in your own words how a JK master-slave flip-flop works. Your answer must include an explanation of what the "master-slave" part of the flip-flop's name means.

Answer to Question 4.2.1

A JK master-slave flip-flop is a type of sequential logic circuit that can store one bit of information. The "master-slave" part of its name refers to the two stages or sections within the flip-flop that work together to control the storage and updating of the stored value. The master stage, which is triggered by the clock signal, captures the input and holds it temporarily. The slave stage, triggered by the inverse clock signal, latches the value from the master stage and outputs the stored value. This arrangement allows for precise control of when the input is accepted and when the output is updated, avoiding any potential race conditions and providing a stable and synchronized operation.

Question 4.2.2 [**4 Marks**] – Study, construct and verify the operation of a JK flip-flop (built using a 7476 IC – see **Figure 8**), by writing the Characteristic Table for a JK master-slave flip-flop. **Note**: Please take into account the instructions given at the beginning of this experiment.



Answer to Question 4.2.2

J	K	C	Q^*
X	X	0	Q
0	0	1	Q
0	1	1	0
1	0	1	1
1	1	1	$\overline{Q}$

EXPERIMENT 3 – Shift Registers

In this experiment, you will be studying and constructing a Shift Register, using four D flip-flops and an inverter. A Shift Register is so called because it "shifts" its output by one-bit position, once every clock cycle. It consists of a set of flip-flops (usually D flip-flops or SR flip-flops) connected together so that the output of one becomes the input of the next and so on, in series.

Therefore in a Shift Register:

1. The same clock pulse is used to drive all the D flip-flops.
2. At each clock pulse, one bit is loaded into the first flip-flop, old bits are shifted down to the next flip-flop and the last bit is shifted out of the last flip-flop.
3. An *n-bit* number takes ***n*** clock cycles to be loaded.

A 4-bit Shift Register can be used either:

- ✓ as a buffer or delay for serial-in, serial-out data (see **Figure 2**); ***or***
- ✓ as a series-in to parallel-out converter (see **Figure 3**).

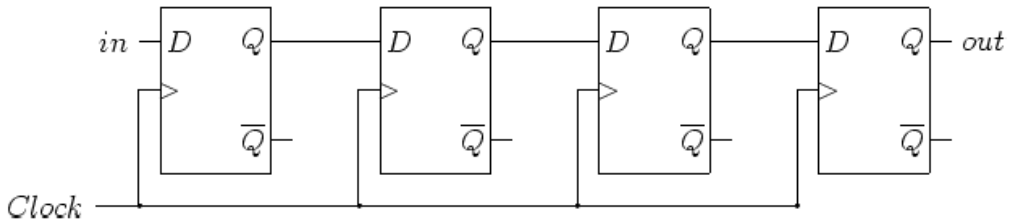


Figure 2 – 4-bit serial-in serial-out Shift Register, implemented using D flip-flops.

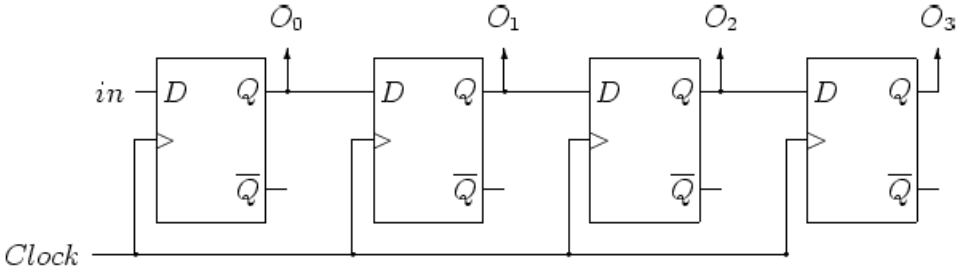
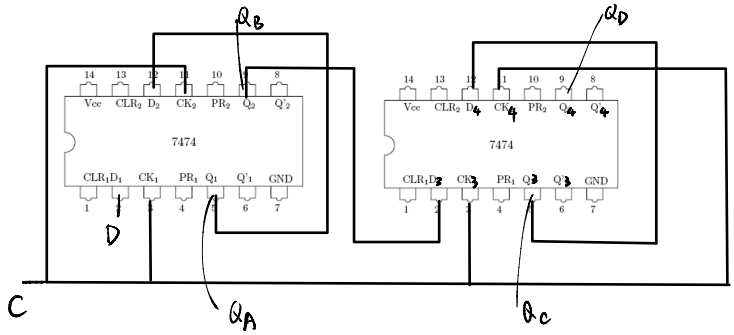


Figure 3 – 4-bit serial-in parallel-out Shift Register, implemented using D flip-flops.

Question 4.3.1 [**4 Marks**] – Construct a 4-bit Shift Register (serial-in, parallel-out) using four D-type flip-flops (see **Figure 7**). Draw a labelled schematic diagram of the 4-bit shift register, indicating how different pins are connected.

Answer to Question 4.3.1



The parallel outputs are

$Q_A Q_B Q_C Q_D$

Question 4.3.2 [**2 Marks**] – Verify the operation of the 4-bit Shift Register, and indicate what is the value of the next state **$Q(t+1)=Q_0Q_1Q_2Q_3$** at the next positive clock edge when the input and current state are **in = 1** and **$Q(t)=Q_0Q_1Q_2Q_3=0110$**, respectively.

Answer to Question 4.3.2

$Q_0^* = Q_{in}$ $Q_2^* = Q_1$

$Q_1^* = Q_0$ $Q_3^* = Q_2$ $Q(t+1) = 1011$

5. Appendix

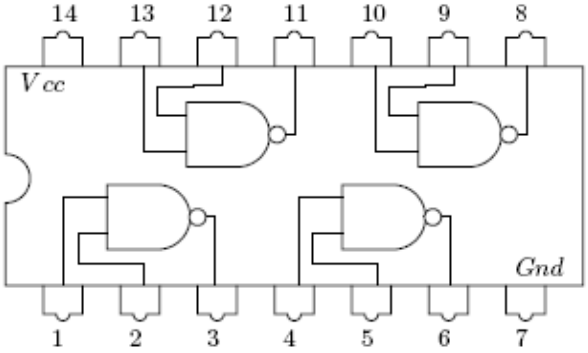


Figure 4 – 7400 (labelled *HD74LS00P*) Quadruple 2-input NAND gates.

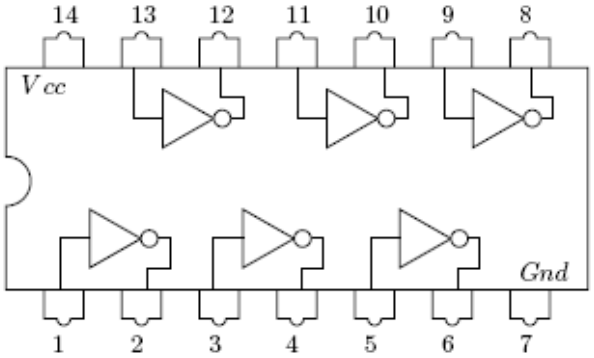


Figure 5 – 7404 (labelled *HD74LS04P*) Hex inverters.

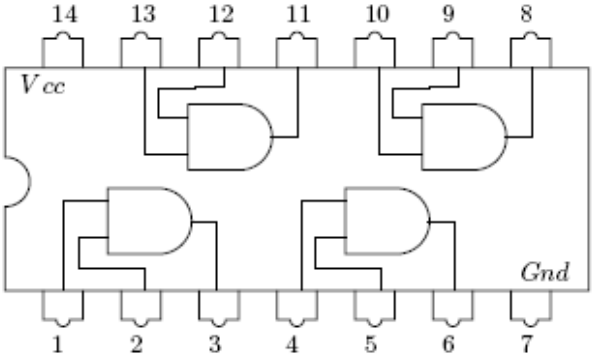


Figure 6 – 7408 (labelled *HD74LS08P*) Quadruple 2-input AND gates.

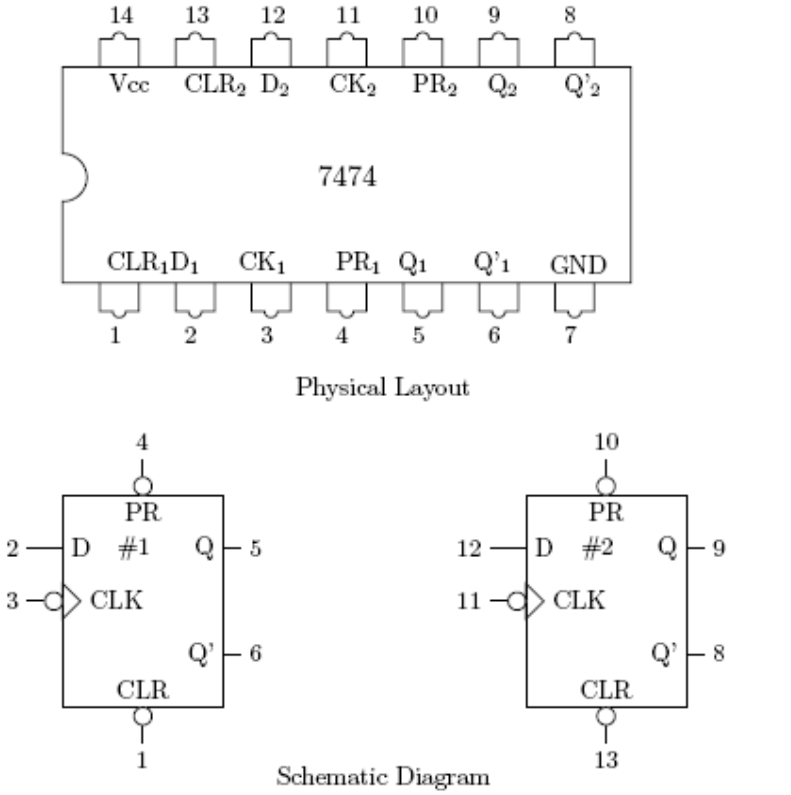


Figure 7 – 7474 (labelled *HD74LS74P*) Dual D-type Flip-Flops.

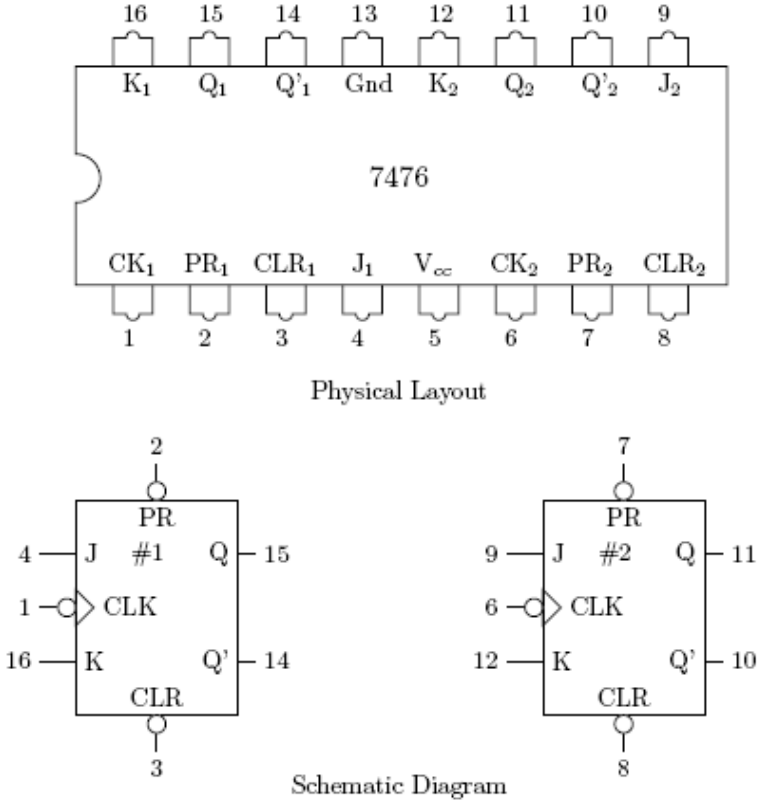


Figure 8 – 7476 (labelled *HD74LS76P*) Dual JK Master-Slave Flip-Flops.

END OF Lab Session 3: Sequential Logic Circuits