



Queen Mary

University of London

Science and Engineering

## **EBU4202: Digital Circuit Design**

### **Block 3 Tutorial**

Dr. Md Hasanuzzaman Sagor (Hasan)

Dr. Chao Shu (Chao)

Dr. Farha Lakhani (Farha)

School of Electronic Engineering and Computer Science,  
Queen Mary University of London,  
London, United Kingdom.

# Question 1

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Draw the circuit diagram of a SR Latch with Control Input using only NAND gates.

## Question 2

Consider the circuit shown in Figure 2. Answer the following questions:

- What is the name for this type of sequential circuit?
- Imagine that S now goes low.  $R = 0$  and  $C = 1$ . Use your knowledge of the operation of gates to determine the new values of Q and QN
- Imagine that C now goes low.  $S = 0$  and  $R = 1$ . Use your knowledge of the operation of gates to determine the new values of Q and QN
- Imagine that C now goes high.  $S = 1$  and  $R = 0$ . Use your knowledge of the operation of gates to determine the new values of Q and QN

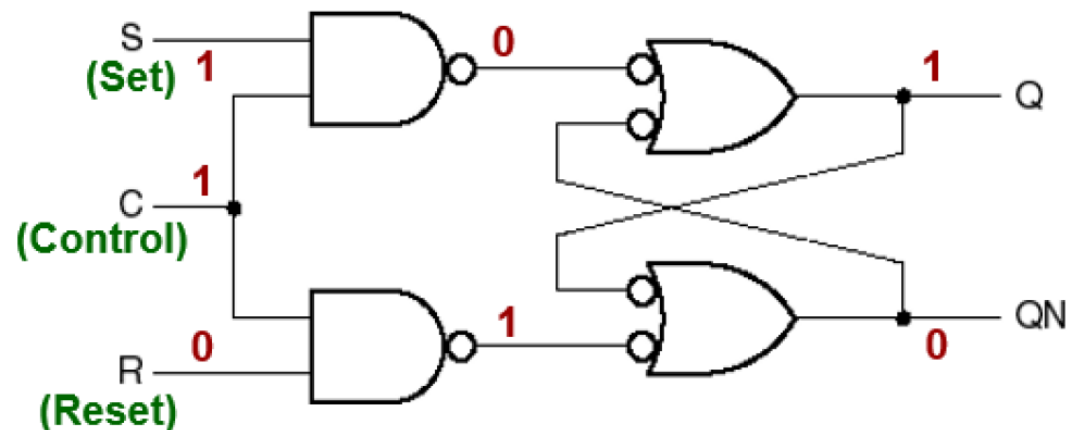


Figure 2

## Question 3

Consider the circuit shown in Figure 3. Answer the following questions:

- What is the name for this type of sequential circuit?
- Imagine that C now goes high.  $D = 1$ . Use your knowledge of the operation of gates to determine the new values of Q and QN
- Imagine that D now goes low.  $C = 1$ . Use your knowledge of the operation of gates to determine the new values of Q and QN
- Imagine that C now goes low.  $D = 1$ . Use your knowledge of the operation of gates to determine the new values of Q and QN

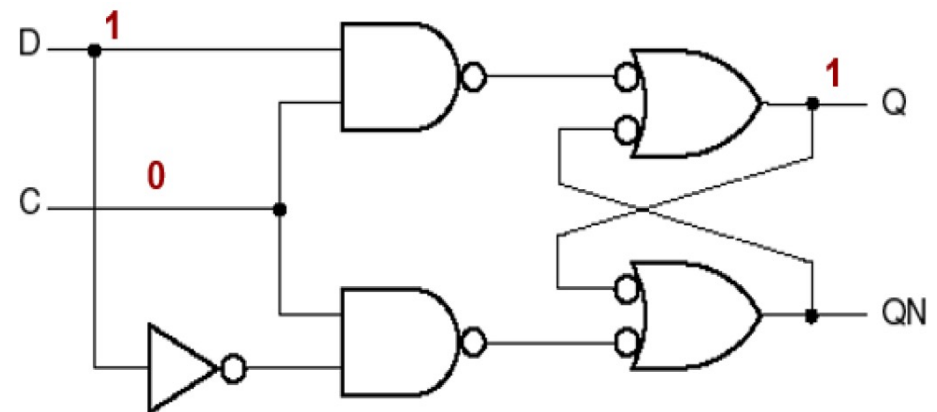


Figure 3

# Question 4

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What is a synchronous state machine?

## Question 5

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In the context of bistable elements and state machines, what is meant by the term “metastability”?

# Question 6

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Explain the difference between a Moore and Mealy machine.

# Question 7

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What is the minimum number of flip-flops required to store 35 states?



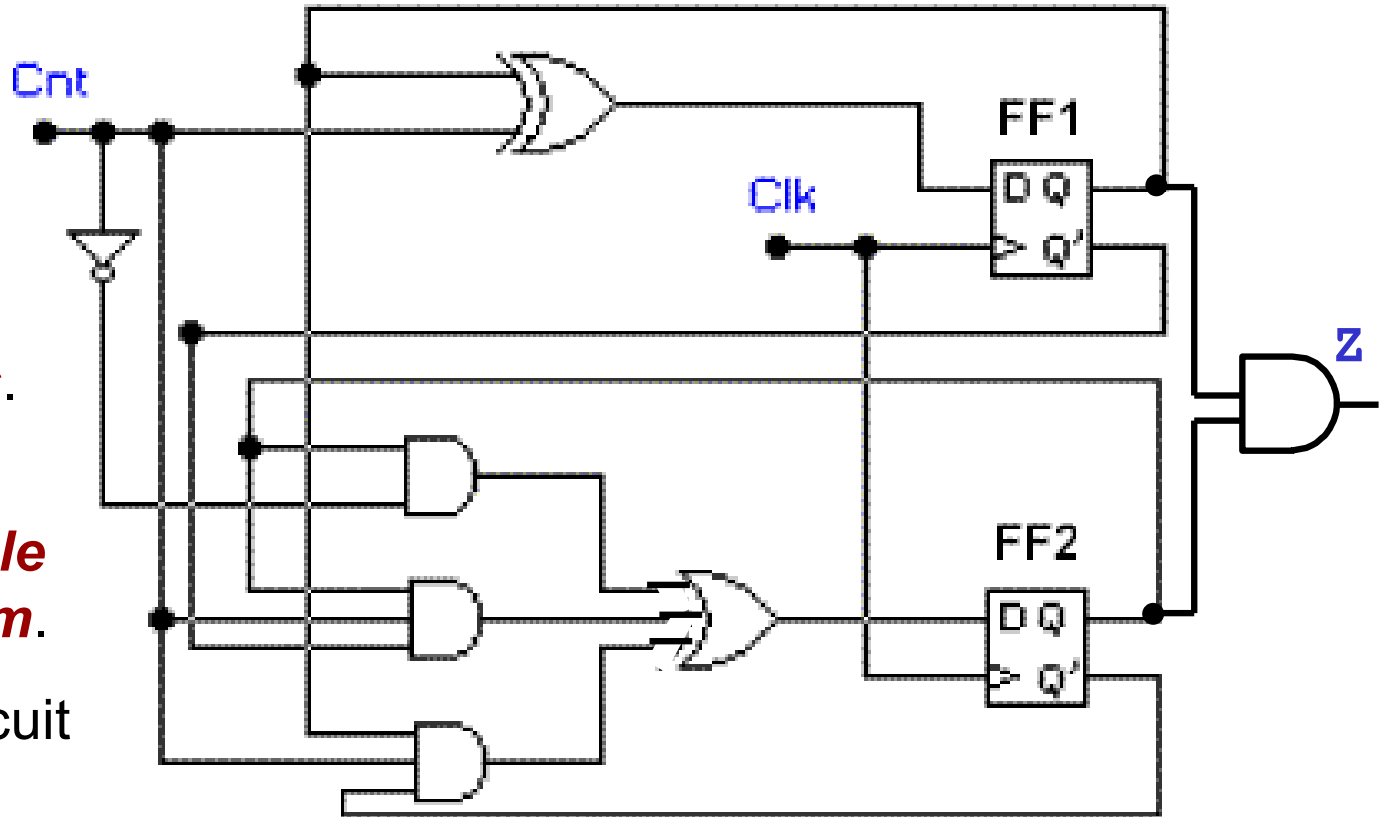
## Question 8

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What is the maximum clock frequency for a state machine having a maximum delay  $T_D$ ? How can the circuit become unstable?

## Question 9

- Answer the questions about the sequential circuit on the right:
  - Derive the **input**, **transition** and **output equations**.
  - Derive the **State/Output Table** and **State Diagram**.
  - What does the circuit do?



# 5 minutes

# Question 10

Design an autonomous sequential circuit, based on edge-triggered JK flip-flops, which generates the following sequence of states: 000, 010, 111, 101, 100 110. The transition table of JK Flip-Flop is given in Figure 5 below. Note: You must draw the circuit diagram, but there is no need to draw the state diagram.





J	K	CLK	Q	QN
x	x	0	last Q	last QN
x	x	1	last Q	last QN
0	0		last Q	last QN
0	1		0	1
1	0		1	0
1	1		last QN	last Q

Figure 5: Transition Table for Edge Triggered JK Flip-Flop