

# **ULTIMATION**

## **Service Manual**

### **Section 3**

#### **Studio Computer Service Information**

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**CAUTION**

All the computer cards contain static-sensitive devices. Proper anti-static precautions should be observed when handling these assemblies.

## 3. Studio Computer Service Information

### 3.1 Card Descriptions

#### *82E356 Moving Fader CA Interface*

This card controls the flow of data between the CA computer and the console, and provides an RS-232 serial diagnostic port. One 82E356 card drives up to eight console bus cards, i.e. 64 channels maximum. Normally, either one or two 82E356 cards are used per console.

This card may be considered in four sections - the CPU and peripheral chips, the CA communication circuitry, the data interface, and the console interface.

The CPU, IC41, is an 8-bit device with multiplexed address and data lines, internal RAM area, three parallel ports, and one serial port. Program memory is held in IC40. There is provision for external RAM, IC39 - this is currently not fitted. IC42 demultiplexes the low-order CPU address lines via the ALE signal. IC38 decodes the high-order CPU address lines and read/write strobes, providing enable lines for each peripheral chip. Bi-directional buffer IC22 interfaces the CPU data bus to the console interface circuitry data bus, address information for the console interface being set up on the outputs of IC49 under the control of IC38. The CPU serial port is interfaced to RS-232 levels by IC2 (Rx Data) and IC8 (Tx Data). Power-up resetting is controlled by IC50, which checks that the supply voltage is stable before initiating the reset pulse. SW2 allows the board to be manually reset.

The CA communication circuitry comprises the 16-bit CA data buffer, IC7 and IC25, the board address decoder, IC51, CA interface control chips IC23-24, and CA signal buffer IC44. The board address is selected via links LK1-2. LK1 should be inserted for board 1; LK 2 should be inserted for board 2. LK3 should not be fitted. Data transmission through the buffer is controlled by the B\_EN and B\_DR signals from IC51.

The data interface between the CA computer and the 82E356 card (and thence the console) comprises two dual port RAM chips, IC4-5. One port of each chip interfaces with the CPU address and data buses under control of the chip enable signals (UR\_EN and LR\_EN) from IC38 and the CPU read and write lines; the second port of each chip interfaces with the CA data buffer, IC7 and IC25, under control of the W\_WR, W\_CE, and W\_OE signals from IC23-24. CA addresses are clocked into IC6 via the IC24 SCHN line. Data *written* by the CA (i.e. fader updates) passes to IC4-5 where it is read under the control of the CPU, IC41. Data to be *read* by the CA is placed in IC4-5 with bit 15 set (to signify new data). After reading the data, the CA clears bit 15. Thus the CA need only transfer channel data that has changed since the previous read (perhaps only 2 or 3 channels out of 64). Finally, some CA commands (e.g. Resets) are decoded by IC24 under control of EXEC, written to IC4-5, interrupt the CPU, IC41, and cause SER to be asserted (to the CA) while the 82E356 card is busy.

The console interface comprises eight identical circuits - one per bus card (or console bay). For the BAY7 interface, IC48 decodes the address data and read/write signals from IC49 to provide three chip enable signals EN0-2 (and three more, EN3-5, for the BAY8 interface). Data is written *to* the faders via IC22 and IC19, and is read *from* the faders via IC36 and IC22. The channel address within the bay (i.e. from 0 to 7 max.), together with channel read and write control lines, appear at the output of IC37. Reading and writing of data is controlled by the CPU, IC41.

### *82E357 Analogue Output Card Description*

This card converts digital data on the CA Data Bus into analogue voltages, and outputs these voltages to up to 64 channel faders and one master fader in turn. The channel faders are addressed in banks of 8. The CA addresses each bank in turn, followed by the master fader.

IC8 and IC16, together with the associated logic, constitute the address decoder, the address being placed on the CA Address Bus A0-7. The Card address is 60H, and the Data Bus Output Address is 61H. For a second card with the 'Over 65' link inserted, these addresses will be 64H and 65H respectively.

IC54-55 provide latched outputs of the 16-bit CA Data Bus via the S38E ribbon to the Master Transport Selector (if fitted). Data is latched into IC54-55 when the OUT line is pulsed low with an address of 61H.

Fader data on CA Data Bus bits 0-11 is inverted by IC40-41 before being latched into the 12-bit DAC, IC48, when the OUT line is pulsed. The analogue output appears on the SIG\_1 line.

The fader address is latched into IC32 and IC34 when EXEC is pulsed low. Bits 0-2 of the CA Data Bus provide a 0-7 count on SIG\_2, SIG\_3, and SIG\_4 for decoding each 8-wide bank of faders, and bits 3-5 of the CA Data Bus are decoded by multiplexer IC6 to provide 8 bank select lines (SIG\_5 to SIG\_12). Bit 6 of the CA Data Bus is only driven when the master fader is being addressed, and is otherwise used to enable channel fader bank addresses through IC6. Also, when EXEC is pulsed low, monostable IC24 is triggered: this pulses whichever channel fader bank address line (SIG\_5 to SIG\_12) is selected via IC6.

The multiplexers are supplied by  $\pm 6V$  in order to cater fully for the DAC output voltage range of  $\pm 5V$ , therefore open collector inverters IC15 and IC33 are used to level-shift the outputs from latches IC32 and IC34 and monostable IC24. The  $\pm 6V$  supplies are derived from the  $\pm 12V$  supplies via IC61-62.

Each of eight analogue multiplexers, IC39, IC46, IC23, IC30, IC14, IC5, IC60, and IC53, route the analogue data on SIG\_1 to one *bank* of eight output interfaces (IC35-38 etc.), *each* interface comprising a Sample-and-Hold circuit and an Integrator. The analogue output line, SIG\_1, provides the data input for *each* of these multiplexers, and addressing is accomplished by the bank decode lines (SIG\_2 to SIG\_4) and *one* of the channel fader bank address lines (SIG\_5 to SIG\_12) for *each* multiplexer.

IC25 decodes the master fader address (CA Data Bus bit 6) and switches the DAC output (SIG\_1) via switch IC47 to a further Sample-and-Hold/Integrator output interface (IC31).

The output voltages to the faders appear on S36E and S37E.

## 3.2 Test and Calibration

### 3.2.1 82E356 Moving Fader CA Interface Card

If, during the course of these tests, you suspect a fault on the 82E356 card itself, you may need to implement the card's diagnostic routines - see Section 10.14.

Enter the test program by typing '!TES EX' then 'L' (for Lights and Switches).

Pressing any fader status button at this point tests the three LEDs (trim, abs, and alt) on that fader. Subsequently pressing 'EX' similarly tests the LEDs on *all* the faders.

A choice can now be made between 'S' for the View All Switches Test or 'F' for the Fader Control Bit Test.

#### View All Switches Test

The View All Switches Test displays a table of 4-digit numbers which relate to assigned channels from each of the possible two CA Interface Cards. Unused channels on either card are denoted by a row of four dashes. Each 4-digit number is a hexadecimal display of the bit pattern returning from each fader. This bit pattern indicates if the fader status button is being pressed, if the touch sense is on, etc.

Each time that a status button or cut switch is pressed (for example), a message at the top of the screen will give a 'decoded version' of that operation. In addition, a particular bit in the associated hexadecimal word will change state. This test gives a quick indication of the state of communication between the CA and the micro controller on the CA Interface Card. The pointer value ('Pntr:') will increment for every word that is passed between the CA and the micro controller. If the message 'TIMED OUT' appears above either of the two board layout grids it means that the card has failed to communicate.

To provide a quick functionality check, some of the bits read in by this test are echoed back to the console. These are as follows:

- The status button lights the trim LED
- Touch sense lights the alt LED
- Fader Stall lights the abs LED
- The cut switch lights the cut switch lamp

If there is a fault on a specific fader then use the Fader Control Bit Test. Return to the Lights and Switches Menu by pressing 'END', and then press 'F'.

#### Fader Control Bit Test

This test provides a means of monitoring the bits coming *from* the fader *and* of setting the bits going *to* the fader. The test usually works in single channel mode. Two columns are presented: the Output column allows the setting of the bits going to the fader, and the Input column allows the reading of the bits coming back from the fader. To select the channel to work on, either use the left/right cursor keys or press the fader status button (if it works) on the relevant channel. The channel number will be shown, at the bottom of the display, in terms of both its physical channel number (e.g. Fader 10) and its logical mix channel number.

The information coming back from the fader can now be seen in the Input column. A blot will appear when each bit is set. The thumbwheel position will appear as a number (between 0 and 8), or the letter 'T'. To send a bit to a fader, use the up/down cursor keys to position the blot in the Output column opposite the bit to be sent. Pressing the 'O' key will now toggle that bit on and off. Any desired combination of bits may be set by this method.

To send the same bit pattern to another fader, simply move to the required channel (using either the cursor keys or the fader status button, as described above).

To toggle the entire desk at once, press the LARGE/SMALL key; this puts the test into global mode. The Input column will now disappear from the display, and any output bit that is selected will be toggled on all the channels each time that the 'O' key is pressed. To return to single channel mode, press the LARGE/SMALL key again.

During this test, the output voltage going to the VCA is normally provided by the computer after having been read in from the fader. Once the fader motor has been turned on, this is no longer possible, as it would start to slowly feedback and move around. To prevent this, while the Motor bit is on, the fader and VCA are driven at the voltage last read from the fader. Therefore, to position the fader with the motor on, first move the fader to the desired position and then set the Motor bit on.

To test a stall sensor, set the fader to roughly the halfway position and set the Motor bit on. This also locks the computer outputs to their current input value. Use your finger nail or a piece of plastic to push the fader up. Check that the stall sensor turns the motor off after about 0.5 seconds. After about a second it should turn back on. The Stall blot should appear on the screen. Push the fader down and check for the same thing. Repeat this test for all the faders. Finally, turn all the motors off.

To test the cuts, press all the cut switches (excluding groups) down. Check that all the switches are read by the computer in the Input column. None of the cut lamps should light. Turn the cut outputs on. All cut lamps should light. Turn the cut outputs off. Turn FCUT on. This instructs the CA interface card to loop all cut inputs directly back to the corresponding output. All the cut lamps should light. The cut switches should still be read by the computer. Turn FCUT off. Turn TR on. All the cut lamps should light. This time the cut switches will not be read by the computer.

The VCA bit will be checked when testing the faders with the Analogue Output Test (see Section 10.4).

Press 'END' twice at this point to return to the Main Test Menu.

### **3.2.2 82E357 Analogue Output Card**

Because of the duality of the system, two types of Analogue Output test are provided.

Enter the Test program by typing '!TES EX'.

Having pressed 'O' to select the Output tests, you are now offered 'V' for the VCA Output test, and 'M', for the Moving Fader tests.

#### **Moving Fader Tests**

Selecting 'A' after 'M' calls up the All Faders Test. This test is designed to check the DC accuracy of the servo system for all faders. To start the test, press 'A' again. All the faders are moved across their range, and any faders that are out of tolerance will display a red LED. Pressing 'T' enables the threshold value to be changed; the normal setting is 8. Pressing 'A' will run the test again. Press 'END' to exit. Any faders that are out of tolerance should be examined more closely using the Individual Fader Test.

Selecting 'I' calls up the Individual Fader Test. This test is used to check the servo accuracy of a particular fader by allowing the manipulation of the output level going to the fader, and then displaying the fader's level as read back by the computer. The program computes the difference between these two values, which it then displays as an error value.

Channels can be selected either with the left/right cursor keys or by pressing the fader status button of the desired channel. The red LED will light on the selected fader. The up/down cursor keys increase/decrease the value sent to the fader. If you wish to set the fader to a particular value, then pressing 'I' will allow the input of a value, up to 1023, followed by 'EXECUTE'. Alternatively, the '+' and '-' keys can be used to move the fader to either extreme of travel. The error value should normally be within the range  $\pm 4$ . Press the 'END' key to exit the test.

Selecting 'W' selects the Wave Test. This creates an outstanding and hypnotic wave pattern of faders which will continue to cycle across the desk until you press 'END'. Impress your friends - and the studio owner!

#### **VCA Output Test**

The VCA Output test can be used to check that the computer is controlling the channel VCAs correctly. It should not be necessary to run this test, but details are given for completeness.

Having selected 'V', the computer will generate a slow ramp followed by a cut for, first, odd numbered channels, and then even numbered channels.

By switching 'VCAs to Meters', the VCA levels can be observed. Check that the channel thumbwheel switches are set to 0 or I. To check the VCA groups, switch an odd numbered channel to the odd numbered groups and an even numbered channel to the even numbered groups. The ramp on a channel switched to a group will be at a faster rate compared to a channel not on a group.

Pressing a channel status button causes a fast ramp to be generated on that channel alone, at a rate controlled by the position of the channel fader. This allows faults to be investigated with an oscilloscope. Pressing 'A' will restore the normal ramp test.

Typing END returns you to the main test menu.

### **Calibration**

The Analogue Output Card is factory set and should not require further adjustment. In case it does, here is the procedure:

Fit the card to an extender. Now choose a channel and measure between its output on S36E (pin 1 = channel 1, pin 2 = channel 2, etc.) and analogue ground (S36E pin 50).

Use the Individual Fader Test to set the D-A to 0000. Adjust VR1 for a reading of  $\pm 1\text{mV}$ . Now set the D-A to 1023 and adjust VR2 for a reading of 4.998 Volts  $\pm 1\text{mV}$ .

### **3.2.3 Fader Calibration**

In order to avoid fader movement due to errors in the fader/computer servo loop a calibration procedure has been incorporated in the program.

The data produced by this process is stored on the program disk and re-loaded when the computer is booted up. Because of the constraints of space on the program disk, the data is stored along with the custom bargraph setup file. In order for this calibration procedure to be effective the desk must have a custom console setup; indeed, it is impossible to carry out the calibration procedure without one. If you are not familiar with the procedure for setting up a custom console configuration, refer to Section 1 of the G Series Computer Service Manual.

The calibration procedure measures the offset and gain errors of the faders and produces a map which contains the adjustments for each fader. This map must be present in order that the faders can be read in correctly. Because of this, the system generates, if needed, a default map which assumes all the faders to be perfect. That is, it has the effect of making no adjustment to the value read in from the hardware. The system generates this default map under the following circumstances:

- If the system is configured not to be a custom console setup.
- If the bargraph file is missing when loading the custom setup.
- If a fader fails the calibration routine its entry is set to default.

Once the calibration procedure has started it is important to let it finish and END as described below so that the new map is saved to disc correctly. Failure to do this could result in a calibration map that is part 'perfect' and part measured from the hardware.

The fader calibration procedure is as follows:

The calibration routine is currently hiding in the Console Objects setup routine. With 'Custom Console' and 'Bargraphs' set to YES, pressing 'O' will get you into the Objects setup routine. If this is the first time that you have set up the Custom Console and Bargraph configuration, it is important that you complete the setup and END right out of the Setup menus as normal, in order to set up something that the calibration procedure can use. Then go back into the Objects menu and press the 'SETUP' key. The cut lights will come on and the message 'Calibrating faders..' will appear on the screen.

All the faders should now move from the bottom to the top and back down again. Red LEDs will appear on the faders that failed to calibrate. (Failure is frequently due to 'stickiness' in the fader mechanics.) The number of faders that failed (if any) will be displayed on the screen. At this point pressing 'END' will return to the Object menu. (If no faders failed the test, the program exits automatically.) Remember to END right out of the setup menus to store the file on disc. (This calibration data is copied across with the COPY CUSTOM routine.)

### **3.2.4 82E353 Fader Servo Card (fitted to each SL678 Fader - see Section 2.)**

VR4 and VR5 adjust the offset and gain of the computer send respectively. They do not normally need adjustment but should be checked following the procedure detailed in Section 2.2.1.

### 3.3 82E356 Card Diagnostic Routines

The 82E356 Moving Fader Interface Card in the CA rack has a series of built in test facilities operated by a terminal connected to the serial port on board. This allows fairly thorough testing of the card, its communication with the CA system, the console bus cards and channel modules. In order to use these tests a terminal is connected to PL5 on the front of the card.

For most terminals, or a PC running a terminal emulator, a ribbon cable may be used with pin 1 of the ribbon cable connected to pin 1 of the 25-way D-Type connector. The terminal serial protocol is 9600 baud, one start bit, no parity bit and one stop bit. No hardware handshaking is supported so this should be set to XON/XOFF or disabled.

In Issue A software no initial prompt or start up message is issued. The tests are called by a single key entry followed by data where appropriate. Entering a question mark '?' will print up a 'help screen' showing all the available commands and their structure. It is important to realise that, once a test is started by entering in the key character, the operation of the card will be suspended, although some command interrupts will be acknowledged to prevent the CA control software from timing out.

Key	Function	Key	Function
D [ADDR]	View block of Dual Port Memory	P	Set Cyclic Buffer Pointer
I	View Processor Memory	L	Clear Cyclic Buffer
B	View Cyclic Buffer Page 1	H	Halt Procedure
N	View Cyclic Buffer Page 2	S	Bay Sequencer
O	View CA Output Buffer	F	Write to Bay Data and Control lines
W	Write to CA via Cyclic Buffer	R	RAM Test ** DESTROYS RAM DATA **
M [ADDR]	Modify Dual Port Memory	K	Non-destructive RAM Test
C [ADDR]	Change Processor Memory		

#### VIEW BLOCK OF DUAL PORT MEMORY (D [ADDRESS])

Shows the contents of a block of dual port memory: 128 16-bit words. The address is the address of the first byte to be shown.

#### VIEW PROCESSOR MEMORY (I)

Shows the contents of the processor's internal memory as a block of 256 bytes.

*Note:*

Addresses 40H to 7FH contain the condition of the switches on the channel modules at the previous time they were read. Addresses 80H to BFH contain the present condition of the switches on the channel modules. Addresses C0H to FFH contain the control data to be sent to the fader modules. All data is stored as high being true.

The arrangement of the bits is as follows:

### FADER READ

BIT	FUNCTION
0	Thumbwheel switch position
1	0..8 are positions 0 to 8
2	9 is position I (isolate)
3	Hex F is error
4	status switch pressed
5	cut switch ON
6	motor servo failed
7	touch being sensed

### FADER WRITE

BIT	FUNCTION	BIT	FUNCTION
0	Selects TR	4	Group enabled
1	LED1 (bottom) ON	5	Cut ON
2	LED2 (middle) ON	6	Motor ON
3	LED3 (top) ON	7	VCA select

VIEW CYCLIC BUFFER PAGE 1 (B)

VIEW CYCLIC BUFFER PAGE 2 (N)

Shows the present contents of the cyclic buffer used to send update information to the CA. The buffer is 256 words long and is displayed as screens of 128 words. The 16 bits of the data word are arranged thus:

BIT	FUNCTION
0	Thumbwheel switch position
1	0..8 are positions 0 to 8
2	9 is position I (isolate)
3	Hex F is error
4	status switch pressed
5	cut switch ON
6	motor servo failed
7	touch sensor
8	
9	
10	
11	
12	
13	
14	
15	Data Available flag (see below)

The Data Available flag (bit 15) is set by the interface when data is presented and cleared by the CA when data is read.

**CHANGE PROCESSOR MEMORY (C [ADDRESS])**

Allows modification of the contents of the processor's internal memory area. The address is entered after the command, the processor puts the space in, the present contents of that memory address are shown and the new data may be entered. If no new data entry is required then hitting the Return key will leave the data unchanged. In both cases the processor will move on to the next location in the memory. To leave this mode enter the halt command <H>.

**SET CYCLIC BUFFER POINTER (P)**

Allows inspection and modification of the contents of the cyclic buffer pointer used to communicate data to the CA. The present contents of the buffer pointer are shown and the new data may be entered. If no new data entry is required then hitting the Return key will leave the data unchanged. To leave this mode enter the halt command <H>.

**CLEAR CYCLIC BUFFER (L)**

Not implemented.

**HALT PROCEDURE (H)**

Used to leave test mode and return the interface to normal operating condition providing you haven't done something stupid like incorrectly modifying the cyclic buffer pointer.

**BAY SEQUENCER (S)**

Walks a high bit up the bay data lines and counts on the bay address lines: useful for finding stuck bay data or address bits. This is difficult to get out of but if the H key is held down (with key repeat on), this normally works.

**RAM TEST (T [START ADDRESS] [END ADDRESS])**

Tests the dual port RAM between the addresses specified: the high order address bytes only are entered. The processor returns with 'OK' if the test passed. If not, 'RD' or 'WR' is returned, followed by the address of the first byte at which a failure was detected. If 'WR' is returned the fault is probably a stuck data line, if a 'RD' is returned the fault is probably a stuck address line. As this is quite a thorough test, all the data in the dual port RAM will be destroyed when it is run. This may cause some strange problems with the faders immediately after it is run.

**NON DESTRUCTIVE RAM CHECK (K [START ADDRESS] [END ADDRESS])**

Tests the dual port RAM between the addresses specified without destroying the data within the memory. The high order address bytes only are entered. The processor returns with 'OK' if the test passed. If not, the address of the first byte at which a failure was detected is returned.

**WRITE TO BAY DATA AND CONTROL LINES (F)**

This allows direct operation of the bay data, address, control and strobe lines. Upon entering this mode the status display lines shown below will appear on the terminal followed by the special prompt '@'.

Bay	Chann	Read	Write	Strobe
00	00	00	00	00
@				

A different bay may be selected or the condition of the output latches may be set by entering the first letter for the relevant parameter followed by the new data. The new data will be set on the latches, the data read, and an updated status display shown on the terminal. For the read instruction the data for the selected bay is read and an updated display shown. Examining the circuit diagram will show that the channel select latch also includes the read and write control lines for the bay. So, in order to *write* data to a fader, bit 3 must be high and bit 4 set low, i.e. add 08H to the channel number, and to *read* data from a fader bit 3 must be set low and bit 4 set high, i.e. add 10H to the channel number. Note that when writing data to a bay the read status should show the same data as the write status. If not, suspect a stuck data line or, more likely, incorrect setting of the bay control lines. When reading data from a bay the write data field should have no effect.

Each bit of the strobe byte operates the strobe of the corresponding bay, i.e. bit 3=strobe\_bay\_3 etc. In order to write data to a fader the strobe line must be taken low then high again, the data being written on the low to high transition.

Remember that both the bay and fader number start with Zero so the first bay is bay 00 and the first channel is 00 (set 10H to read and 08H to write).

*Connection of serial port*

20-Way Ribbon (PL 5 on board)	25-Way D-Type (on terminal)	Function
Pin	Pin	
1	1	Screen/Case Ground
3	2	Data Board > Term
5	3	Data Term > Board
13	7	Signal Ground

*Protocol*

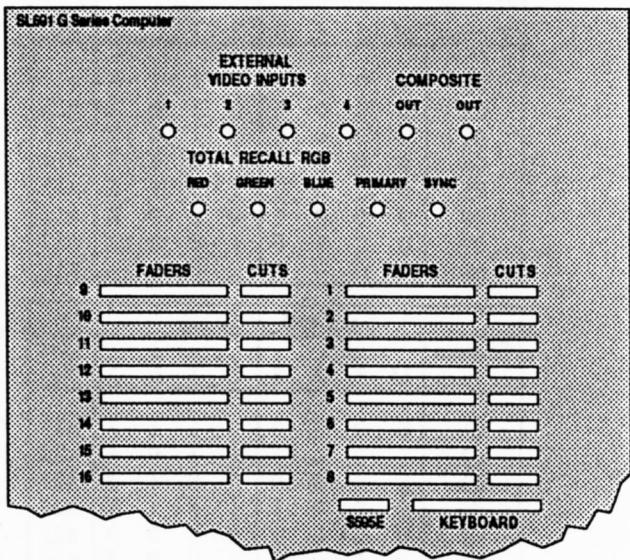
Baud Rate:	9600	Stop Bits:	ONE
PARITY:	NONE	Handshake:	NONE
Start Bits:	ONE		

### 3.4 TR Address Switch Settings

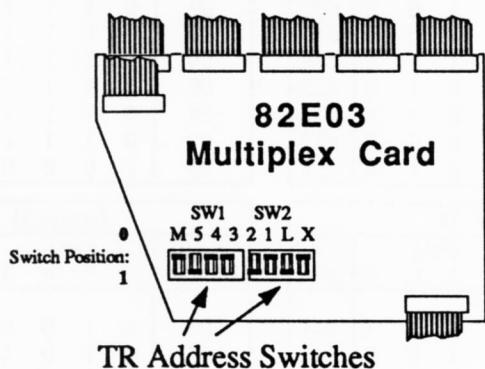
*It should only ever be necessary to carry out the procedures described in this section when replacing SL611 channel strips, or when otherwise reconfiguring or extending the console.*

*Note that if TR fails to operate correctly on a single channel, it is most likely that the TR Address Switches on that channel strip have been inadvertently altered, and they should be reset according to the procedures outlined below.*

The settings of the TR Address Switches on each SL611 Multiplex Card are dependant upon where the corresponding S14E cable is plugged into the computer. The computer rear panel is shown opposite. (Note that the panel legends and layout of earlier revisions may differ from those shown here.) For consoles with a single I/O system, only the right-hand column of connectors is used. With a dual I/O system, the ribbons should be shared out equally between both columns of connectors. Note, however, that the S14E cable from the VCA groupers is *always* plugged into an even-numbered input on the right-hand column, otherwise the computer is not able to find the master fader.



To find the required address switch settings for a particular channel, first determine where the S14E for that corresponding bay is plugged into the computer. Then refer to the table at the top of the following page to obtain a 'logical bay' ID (A-H). The table for that bay (see the lower tables on the following page) will then show the address switch settings for each channel in that bay. The location on the 82E03 Multiplex Card of each of the switch elements referred to in these tables is shown in the diagram below.



An alternative way of determining the address switch settings, once the system is all connected, is to use the CA Interface Card (Lights and Switches) Test (see Section 3.2.1). Pressing the status button of the required channel will cause a 3-digit number to be displayed next to the 'Last' message. The 'Last' number columns in the tables on the following page can then be used to translate this into the correct address switch settings.

## SL4000/6000 Series Moving Fader Service Information

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S14E Connector Number †	S14E Connector Number	Logical Bay Table
9	1	A
10	2	B
11	3	C
12	4	D
13	5	E
14	6	F
15	7	G
16	8	H

† Dual I/O only

Logical Bay A									
Channel Number	SW1				SW2				'Last' No.
	M	5	4	3	2	1	L	X	
01	0	0	0	0	1	1	1	X	π11
02	0	0	0	1	0	1	0	X	π12
03	0	0	0	0	1	1	0	X	π13
04	0	0	0	1	0	1	1	X	π14
05	0	0	0	0	1	0	1	X	π15
06	0	0	0	1	0	0	0	X	π16
07	0	0	0	0	1	0	0	X	π17
08	0	0	0	1	0	0	1	X	π18

Logical Bay E									
Channel Number	SW1				SW2				'Last' No.
	M	5	4	3	2	1	L	X	
01	0	1	0	0	1	1	1	X	π51
02	0	1	0	1	0	1	1	0	π52
03	0	1	0	0	0	1	1	0	π53
04	0	1	0	1	0	1	0	1	π54
05	0	1	0	0	1	0	1	1	π55
06	0	1	0	1	0	0	1	0	π56
07	0	1	0	0	1	0	0	0	π57
08	0	1	0	1	0	0	1	X	π58

Logical Bay B									
Channel Number	SW1				SW2				'Last' No.
	M	5	4	3	2	1	L	X	
01	0	0	0	0	0	1	1	X	π21
02	0	0	0	1	1	1	0	X	π22
03	0	0	0	0	0	0	1	X	π23
04	0	0	0	1	1	1	1	X	π24
05	0	0	0	0	0	1	0	X	π25
06	0	0	0	1	1	0	0	X	π26
07	0	0	0	0	0	0	0	X	π27
08	0	0	0	1	1	0	1	X	π28

Logical Bay F									
Channel Number	SW1				SW2				'Last' No.
	M	5	4	3	2	1	L	X	
01	0	1	1	0	1	1	1	X	π61
02	0	1	1	0	1	1	0	X	π62
03	0	1	1	0	1	0	1	X	π63
04	0	1	1	0	1	0	0	X	π64
05	0	1	1	0	0	1	1	X	π65
06	0	1	1	0	0	0	1	X	π66
07	0	1	1	0	0	1	0	X	π67
08	0	1	1	1	1	1	1	X	π68

Logical Bay C									
Channel Number	SW1				SW2				'Last' No.
	M	5	4	3	2	1	L	X	
01	0	0	1	0	1	1	1	X	π31
02	0	0	1	1	0	1	0	X	π32
03	0	0	1	0	1	1	0	X	π33
04	0	0	1	1	0	1	1	X	π34
05	0	0	1	0	1	0	1	X	π35
06	0	0	1	1	0	0	0	X	π36
07	0	0	1	0	1	0	0	X	π37
08	0	0	1	1	0	0	1	X	π38

Logical Bay G									
Channel Number	SW1				SW2				'Last' No.
	M	5	4	3	2	1	L	X	
01	0	1	1	1	1	1	0	X	π71
02	0	1	1	1	1	0	0	X	π72
03	0	1	1	1	0	1	1	X	π73
04	0	1	1	1	0	1	0	X	π74
05	0	1	1	1	0	1	0	X	π75
06	0	1	1	1	1	0	0	1	π76
07	0	1	1	1	0	0	0	0	π77
08	1	0	0	0	0	0	0	0	π78

Logical Bay D									
Channel Number	SW1				SW2				'Last' No.
	M	5	4	3	2	1	L	X	
01	0	0	1	0	0	1	1	X	π41
02	0	0	1	1	1	1	0	X	π42
03	0	0	1	0	0	0	1	X	π43
04	0	0	1	1	1	1	1	X	π44
05	0	0	1	0	0	1	0	X	π45
06	0	0	1	1	1	0	0	X	π46
07	0	0	1	0	0	0	0	X	π47
08	0	0	1	1	1	0	1	X	π48

Logical Bay H										
Channel Number	SW1				SW2				'Last' No.	
	M	5	4	3	2	1	L	X		
01	0	1	0	0	0	1	1	X	π81	
02	0	1	0	1	1	1	0	X	π82	
03	0	1	0	0	0	0	1	X	π83	
04	0	1	0	1	1	1	1	X	π84	
05	0	1	0	0	0	0	1	0	X	π85
06	0	1	0	0	1	1	0	0	X	π86
07	0	1	0	0	0	0	0	0	X	π87
08	0	1	0	1	1	0	1	X	π88	

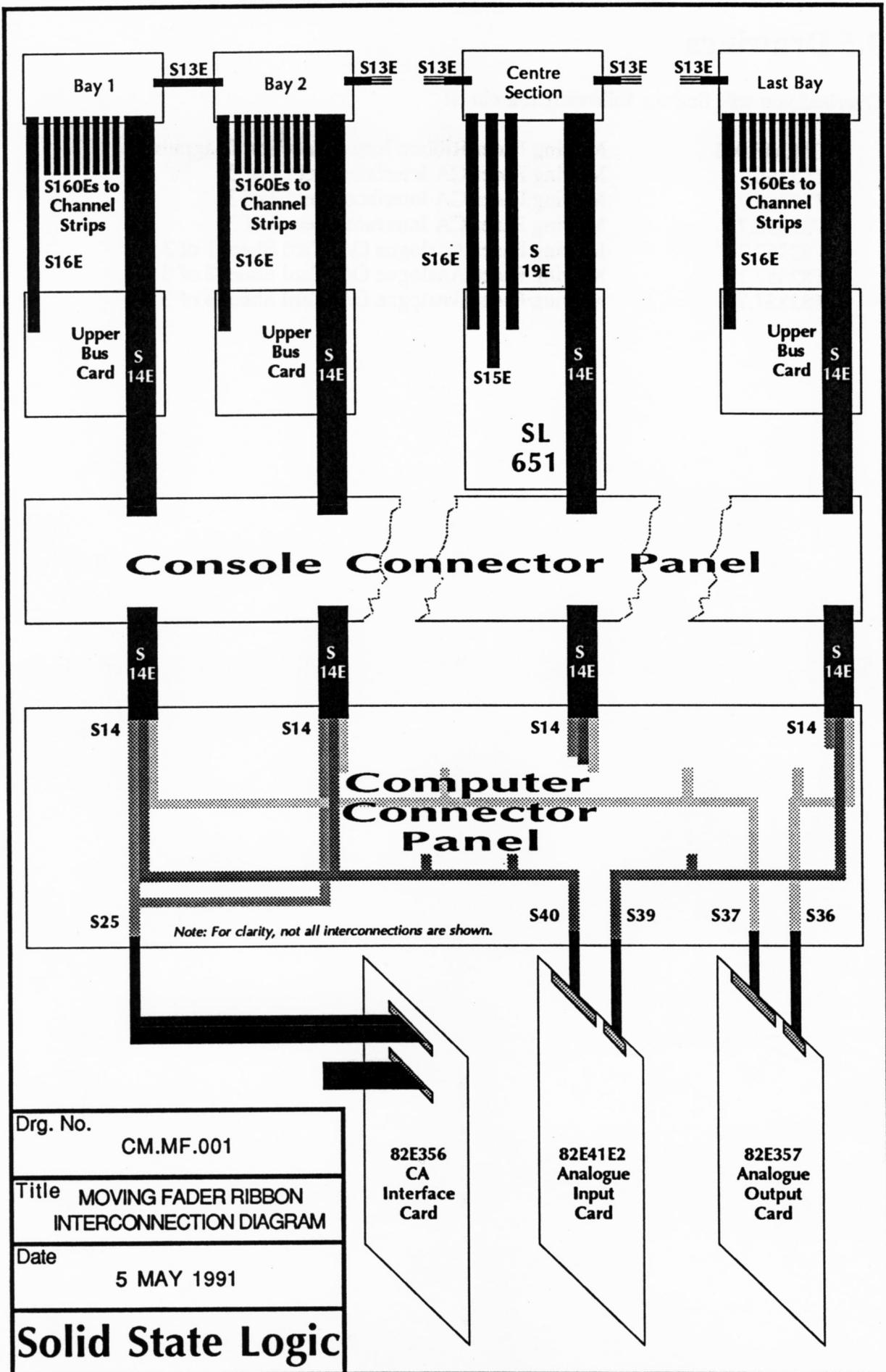
**Note:** In the 'Last' Number Column in the above tables, 'π' represents the CA Interface Card number. For consoles with a single I/O system, this number will always be '1'. For consoles with dual I/O systems, the number will be '1' or '2', depending upon which card is driving that bay.

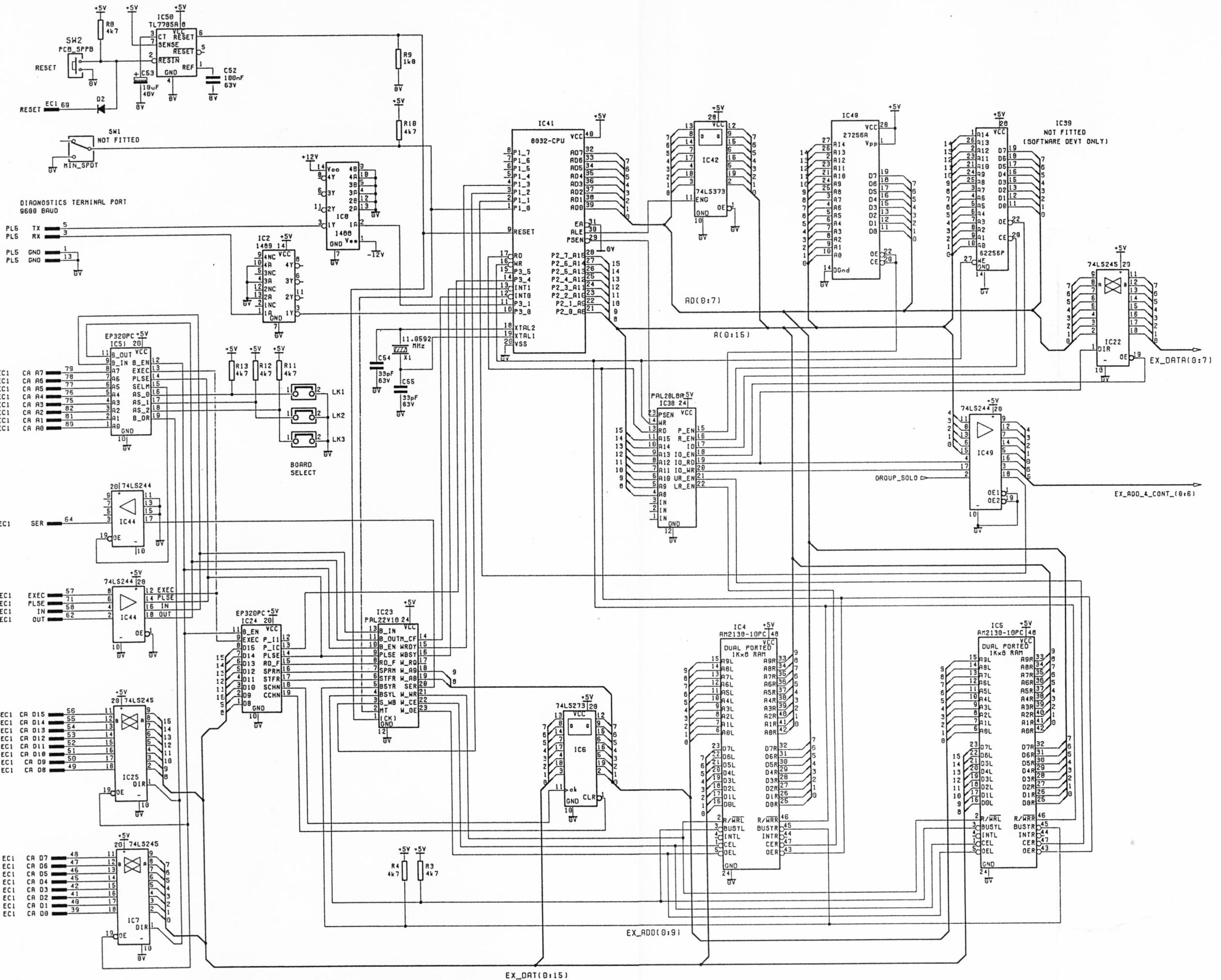
As an example, consider a dual I/O system: the number for Channel 2 of a Bay driven from S14E connector 15 (see top table) would be '272'. If that bay was driven instead from connector 11, the number would be '232'. If that bay was driven instead from connector 5, the number would be '152'.

### **3.5 Drawings**

Overleaf you will find the following drawings:

CM.MF.001	Moving Fader Ribbon Interconnection Diagram
T82356.71	Moving Fader CA Interface Sheet 1 of 3
T82356.72	Moving Fader CA Interface Sheet 2 of 3
T82356.73	Moving Fader CA Interface Sheet 3 of 3
T82357.71	Moving Fader Analogue O/P Card Sheet 1 of 3
T82357.72	Moving Fader Analogue O/P Card Sheet 2 of 3
T82357.73	Moving Fader Analogue O/P Card Sheet 3 of 3





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REV	ISS	DATE	DETAILS	
0	A	28 MAR 91	NEW DRAWING	BC MM
1	A	11 SEP 91	ECO 4K/772 NO CHANGE	MM

PCB ISSUE CD

USED ON SL678 A2

**TITLE** MOVING FADER  
CA INTERFACE

RG.NO. T82356 71

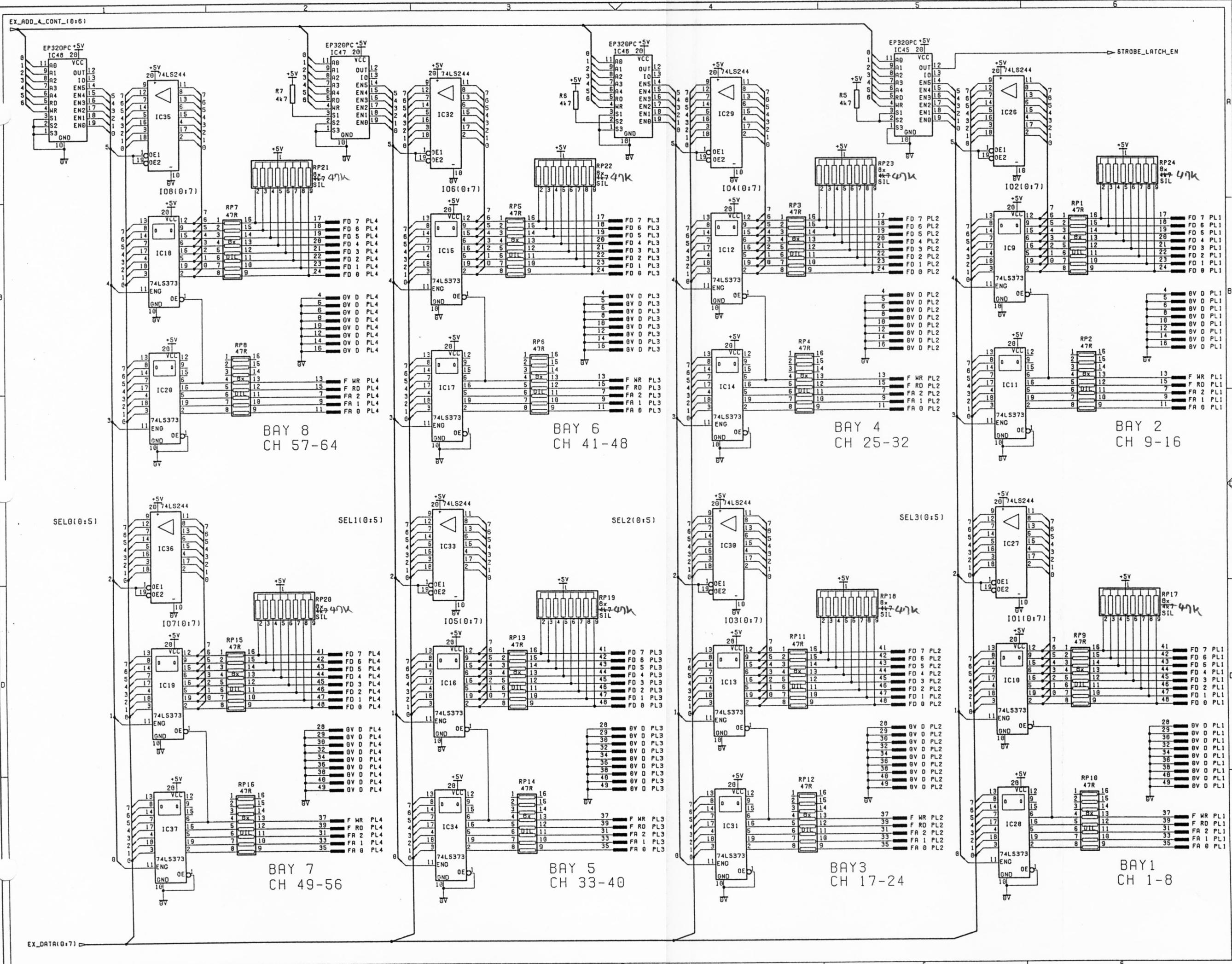
SHEET 1 OF 3

# Solid State Logic

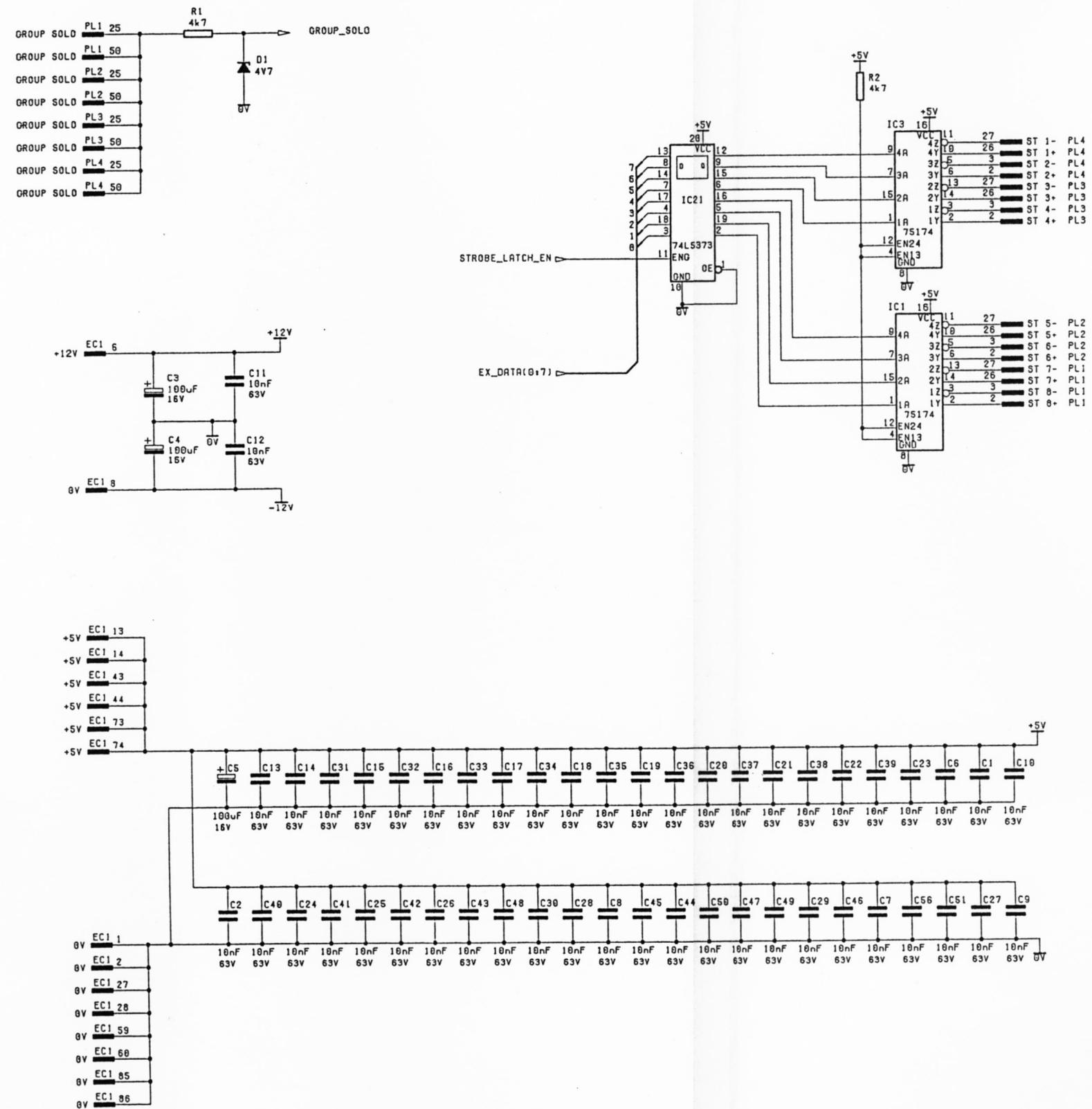
REV	ISS	DATE	DETAILS
0	A	28 MAR 91	NEW DRAWING BC MM
1	A	11 SEP 91	ECO 4K/772 NO CHANGE MM

PCB ISSUE CD  
USED ON SL678 A2  
TITLE MOVING FADER CA INTERFACE  
ORG.NO. T82356.72  
SHEET 2 OF 3

**Solid State Logic**



ISS	DATE	DETAILS	
A	28 MAR 91	NEW DRAWING	BC MM
A	11 SEP 91	ECO 4K/772 NO CHANGE	MM



PCB ISSUE CD

SED ON SL678 A2

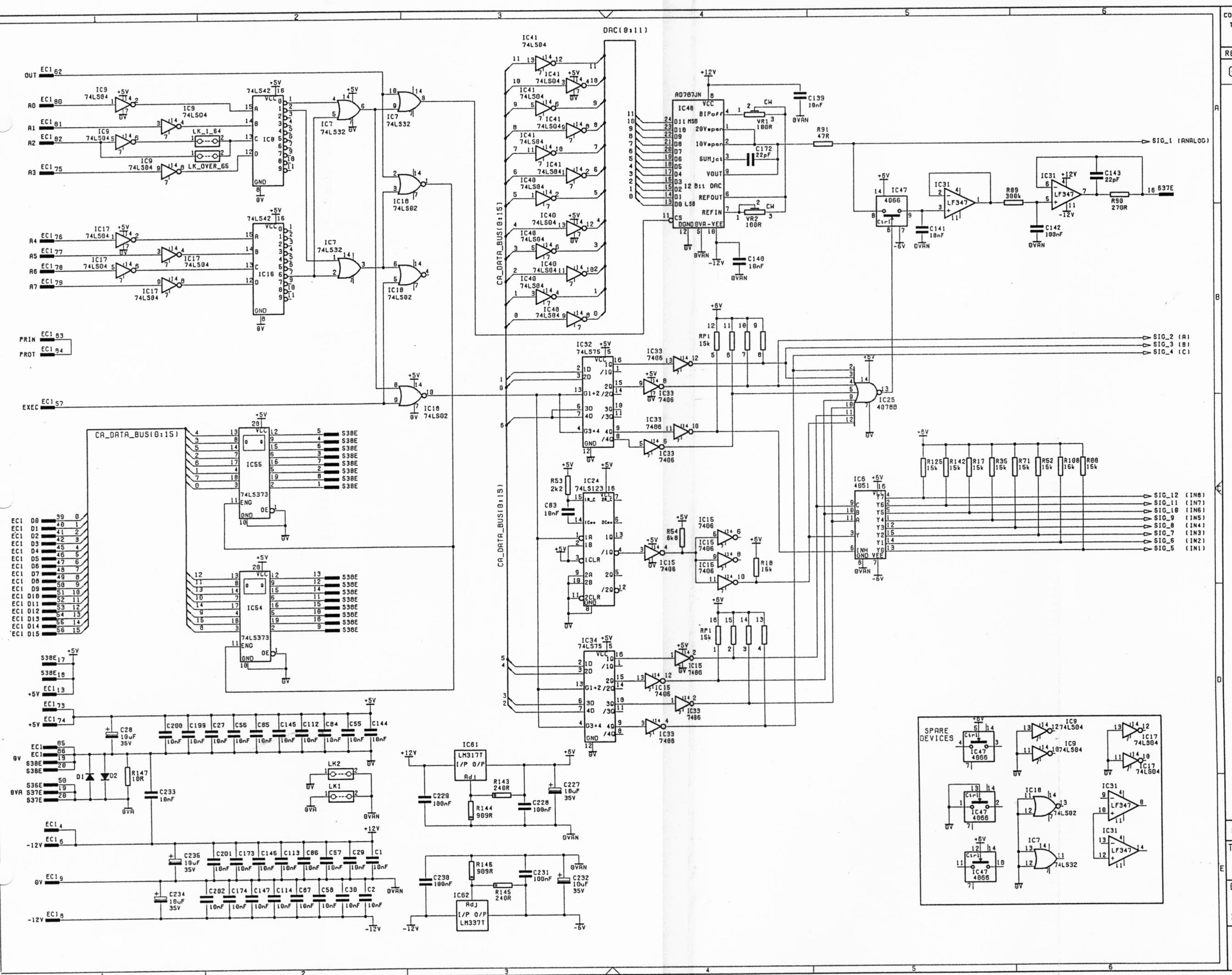
TLE MOVING FADER  
CA INTERFACE

RG.NO.

182356.75

RECEIVED 5-8-5

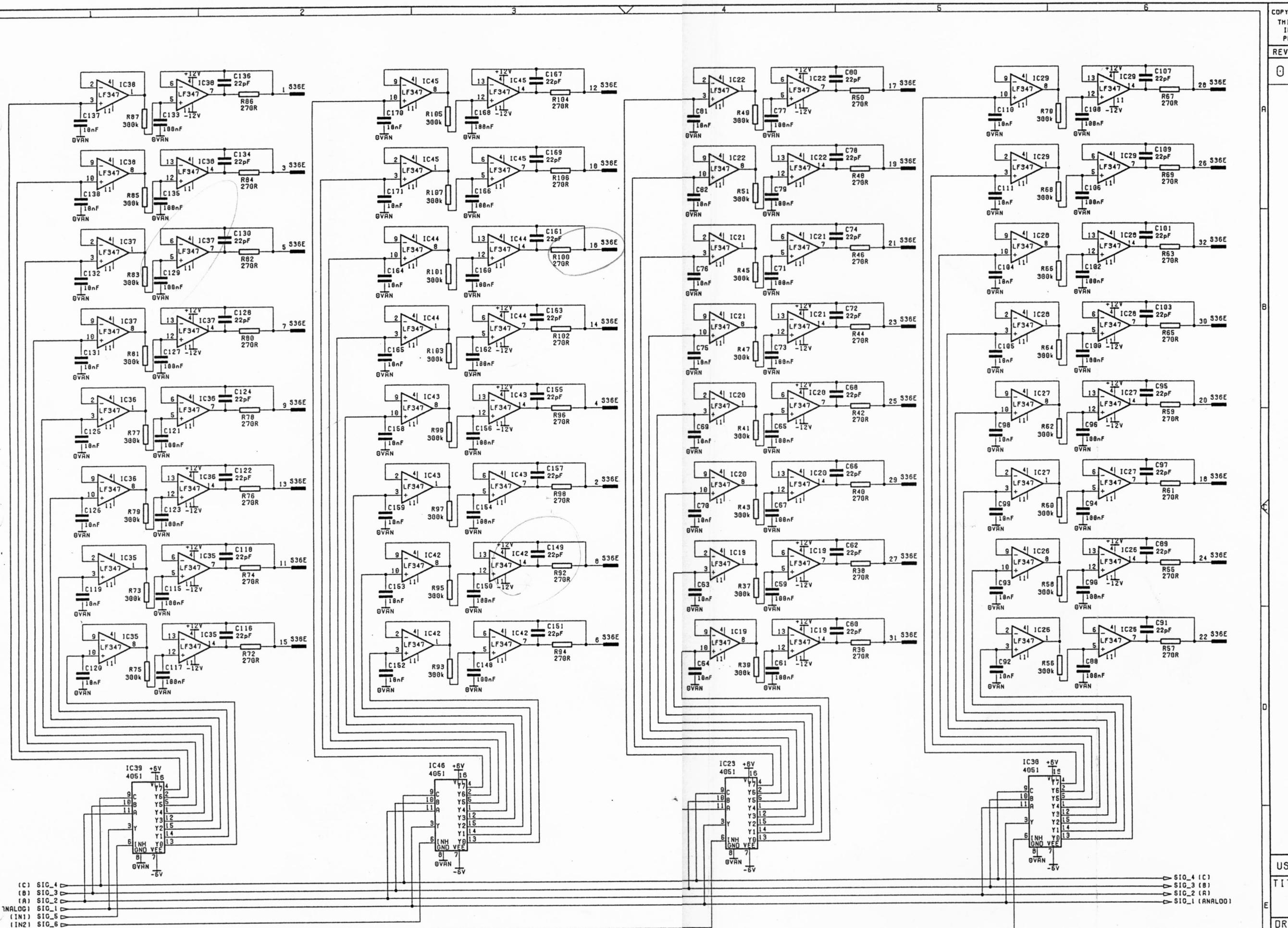
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EV	ISS	DATE	DETAILS
0	A	18 MAR 91	NEW DRAWING MM
PCB ISSUE CO			
USED ON		SL678	A2
TITLE			
MOVING FADER ANALOGUE O/P CARD			
ORG. NO.			
T82357.71			
SHEET 1 OF 3			

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V	ISS	DATE	DETAILS	
	A	18 MAR 91	NEW DRAWING	RP MM
				PCB ISSUE CD

USED ON SL678 HZ

MOVING FADER  
ANALOGUE O/P CARD

RG.NO.

T82357.72

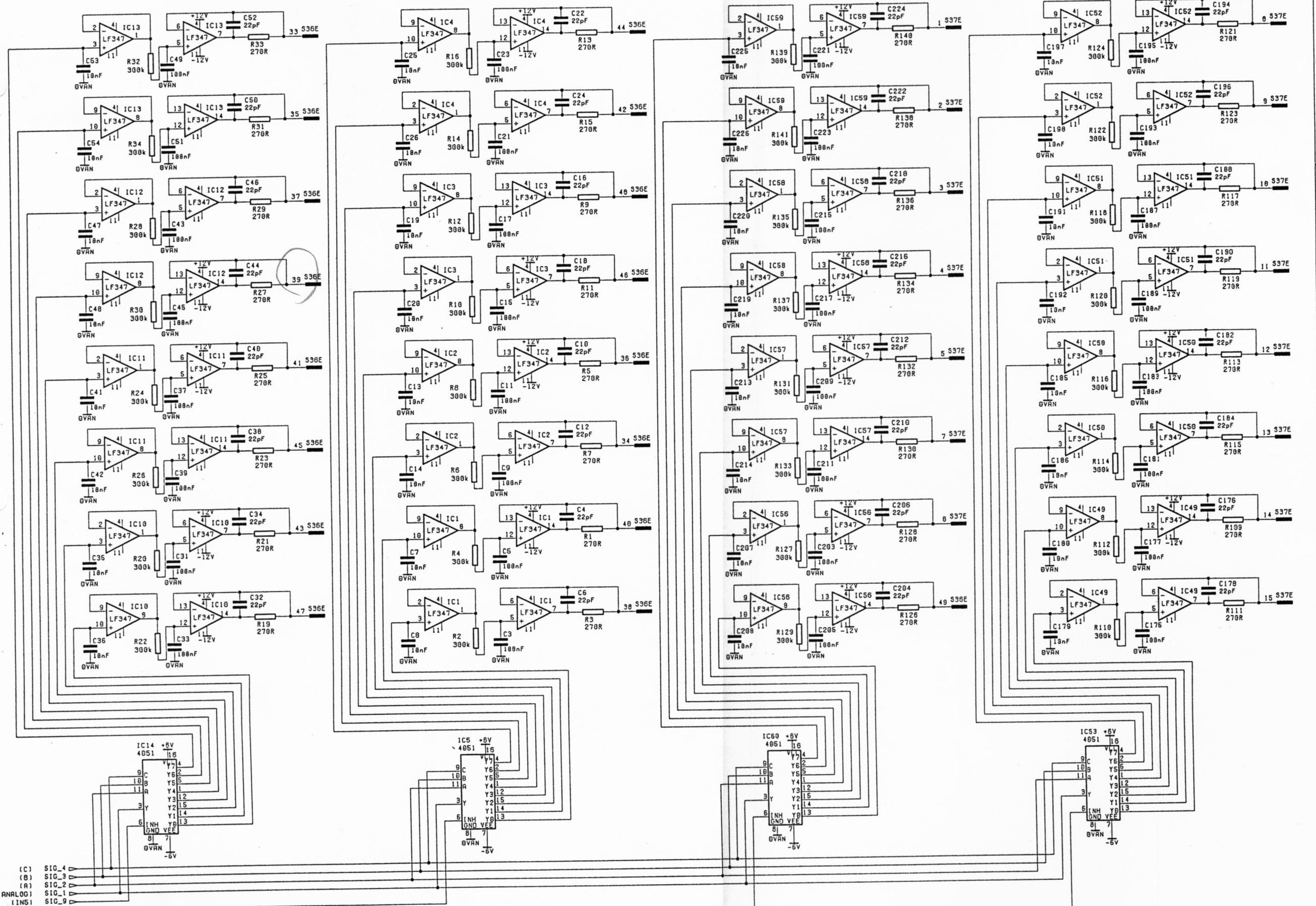
SHEET 2 OF 3

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REV	ISS	DATE	DETAILS
0	A	18 MAR 91	NEW DRAWING RP M1



(C) SIG\_4  
(B) SIG\_3  
(A) SIG\_2  
SIG\_1  
(ANALOG)  
(INS)  
(ING) SIG\_10  
(IN7) SIG\_11  
(IN8) SIG\_12

PCB ISSUE CO  
USED ON SL678 A2

TITLE MOVING FADER  
ANALOGUE O/P CARD

ORG.NO. T82357.73

SHEET 3 OF 3

**Solid State Logic**