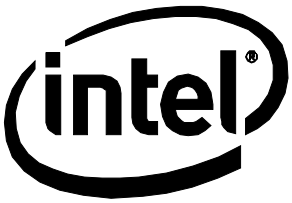


Intel® Desktop Board D2700MUD

Technical Product Specification

June 2012

Part Number: G34953-002

The Intel® Desktop Board D2700MUD may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board D2700MUD Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the Intel® Desktop Board D2700MUD Technical Product Specification.	December 2011
-002	Specification Clarification	June 2012

This product specification applies to only the standard Intel® Desktop Board D2700MUD with BIOS identifier MUCDT10N.86A.

Board Identification Information

Basic Desktop Board D2700MUD Identification Information

AA Revision	BIOS Revision	Notes
G32419-502	MUCDT10N.86A.0047	1,2
G32419-503	MUCDT10N.86A.0067	1,2
G32419-504	MUCDT10N.86A.0067	1,2
G32419-600	MUCDT10N.86A.0067	1,2
G32419-601	MUCDT10N.86A.0067	1,2
G32419-602	MUCDT10N.86A.0069	1,2

Notes:

1. The AA number is found on a small label on the component side of the board.
2. The Intel® NM10 Express Chipset used on this AA revision consists of the following component:

Device	Stepping	S-Spec Numbers
CG82NM10	B0	SLGXX

Specification Changes or Clarifications

Table 1 indicates the Specification Changes or Specification Clarifications that apply to the Intel® Desktop Board D2700MUD.

Table 1. Specification Changes or Clarifications

Date	Type of Change	Description of Changes or Clarifications
June 2012	Spec Clarification	Added a Note to section 1.4 System Memory on page 18.

Errata

Current characterized errata, if any, are documented in a separate Specification Update. See http://developer.intel.com/products/desktop/motherboard/index.htm for the latest documentation.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the Intel® Desktop Board D2700MUD. It describes the standard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the Intel Desktop Board D2700MUD and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on the board
2	A map of the resources of the board
3	The features supported by the BIOS Setup program
4	A description of the BIOS error messages, beep codes, and POST codes
5	Regulatory compliance and battery disposal information

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
GB	Gigabyte (1,073,741,824 bytes)
GB/s	Gigabytes per second
Gb/s	Gigabits per second
KB	Kilobyte (1024 bytes)
Kb	Kilobit (1024 bits)
kb/s	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/s	Megabytes per second
Mb	Megabit (1,048,576 bits)
Mb/s	Megabits per second
TDP	Thermal Design Power
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
*	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

Contents

Figures

Tables

1 Product Description

1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the major features of Intel Desktop Board D2700MUD.

Table 2. Feature Summary

Form Factor	Mini-ITX (6.7 inches by 6.7 inches [170 millimeters by 170 millimeters]) compatible with microATX
Processor	Passively-cooled, soldered-down Dual-Core Intel® Atom™ processor with integrated graphics and integrated memory controller
Memory	• Two 204-pin DDR3 SDRAM Small Outline Dual Inline Memory Module (SO-DIMM) sockets • Support for DDR3 1066 MHz, DDR3 1333 MHz, and DDR3 1600 MHz SO DIMMs Note: DDR3 1333 MHz and DDR3 1600 MHz memory will run at 1066 MHz • Support for up to 4 GB of system memory on a single SO-DIMM
Chipset	Passively cooled, Intel® NM10 Express Chipset
Audio	Multi-streaming 5.1 (6-channel) audio subsystem support based on the Realtek* ALC662 high definition audio codec
Internal Graphics	Onboard Intel® graphics subsystem with support for: • Analog displays (VGA) • Digital displays (DVI-D) • Flat Panel displays (LVDS interface)
Legacy I/O Control	Winbond W83627DHG-P based Legacy I/O controller for hardware management, serial, parallel, and PS/2* ports
Peripheral Interfaces	• Seven USB 2.0 ports: — Four back panel ports — Two ports are implemented with a dual port internal header for front panel cabling — One port is implemented with an internal header (brown-colored) that supports an Intel® Z-U130 USB Solid-State Drive or compatible device • Two Serial ATA (SATA) 3.0 Gb/s connectors (supporting IDE and AHCI mode) • One parallel port connector on the back panel • Two serial port headers • PS/2-style keyboard/ mouse ports
LAN Support	10/100/1000 Mb/s Ethernet LAN subsystem using an Intel® 82574L Gigabit Ethernet Controller

continued

Table 2. Feature Summary (continued)

BIOS	• Intel® BIOS (resident in the SPI Flash device) • Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS
Instantly Available PC Technology	• Suspend to RAM support • Wake on PCI, PCI Express*, PS/2, serial, front panel, USB ports, and LAN
Expansion Capabilities	• One Conventional PCI bus connector (with riser card support for up to two PCI cards) • One PCI Express Full-/Half-Mini Card slot
Hardware Monitor Subsystem	• Hardware monitoring through the Windbond I/O controller • Voltage sense to detect out of range power supply voltages • Thermal sense to detect out of range thermal values • One fan header • One fan sense input used to monitor fan activity • Fan speed control

1.1.2 Board Layout

Figure 1 shows the location of the major components.

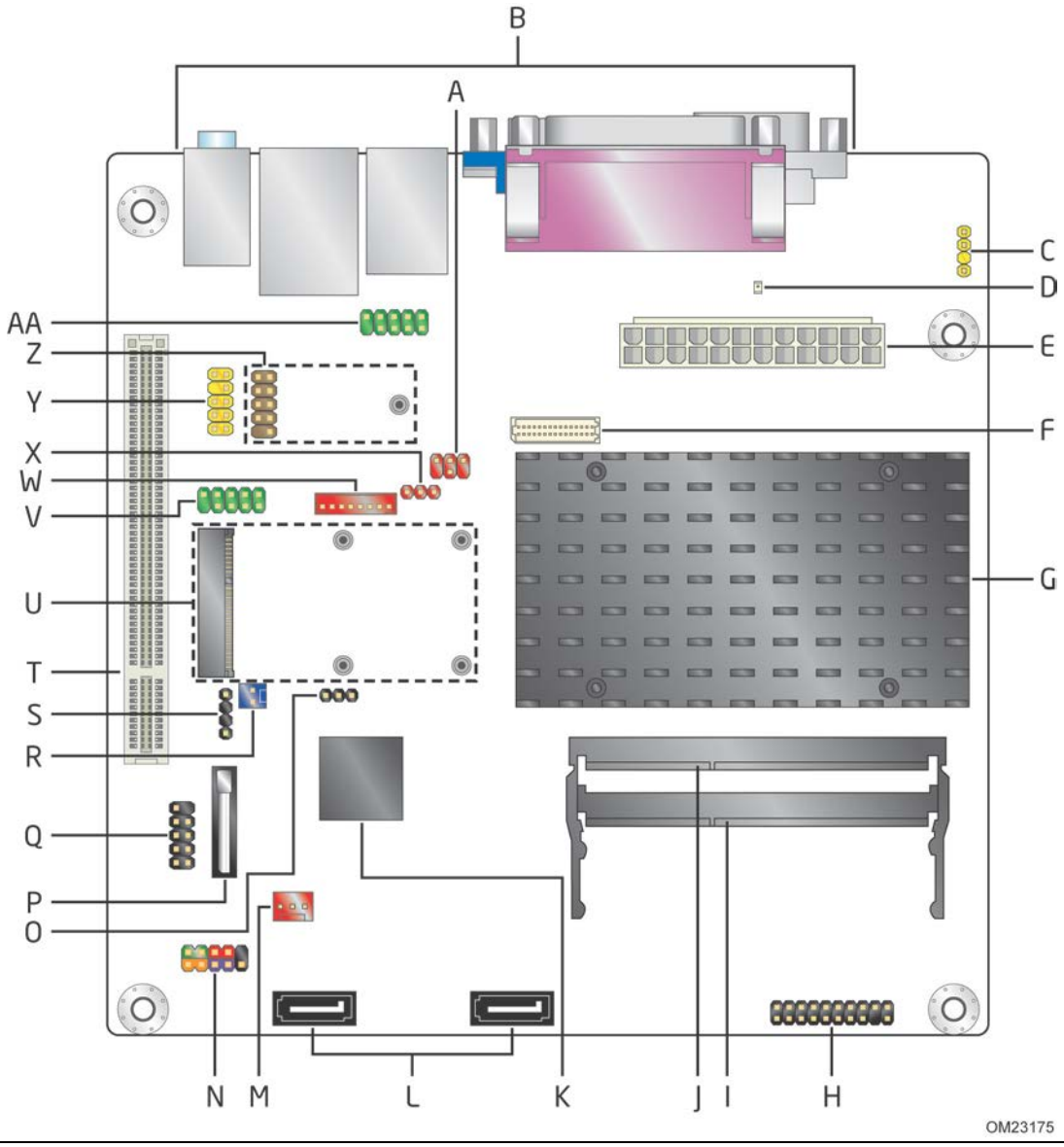


Figure 1. Major Board Components

Table 2 lists the components identified in Figure 1.

Table 3. Board Components Shown in Figure 1

Item/callout from Figure 1	Description
A	LVDS inverter panel voltage selection jumper
B	Back panel connectors
C	S/PDIF header
D	Standby power LED
E	Processor core power connector (2 x 12)
F	LVDS panel connector
G	Intel Atom processor
H	Trusted Platform Module (TPM) header
I	SO-DIMM channel A socket, DIMM 1
J	SO-DIMM channel A socket, DIMM 0
K	Intel NM10 Express Chipset
L	SATA connectors
M	System fan header
N	Front panel header
O	BIOS setup configuration jumper block
P	Battery
Q	Front panel USB 2.0 header
R	Front Panel Wireless Activity LED header
S	Piezo/monotonic speaker header
T	Conventional PCI bus add-in card connector
U	PCI Express Full-/Half-Mini Card slot
V	Serial port header, COMM 2
W	FPD brightness connector
X	LVDS inverter power voltage selection jumper
Y	Front panel audio header
Z	Front panel USB header that supports an Intel Z-U130 USB Solid-State Drive or compatible device (brown-colored))
AA	Serial port header, COMM 1

1.1.3 Block Diagram

Figure 2 is a block diagram of the major functional areas.

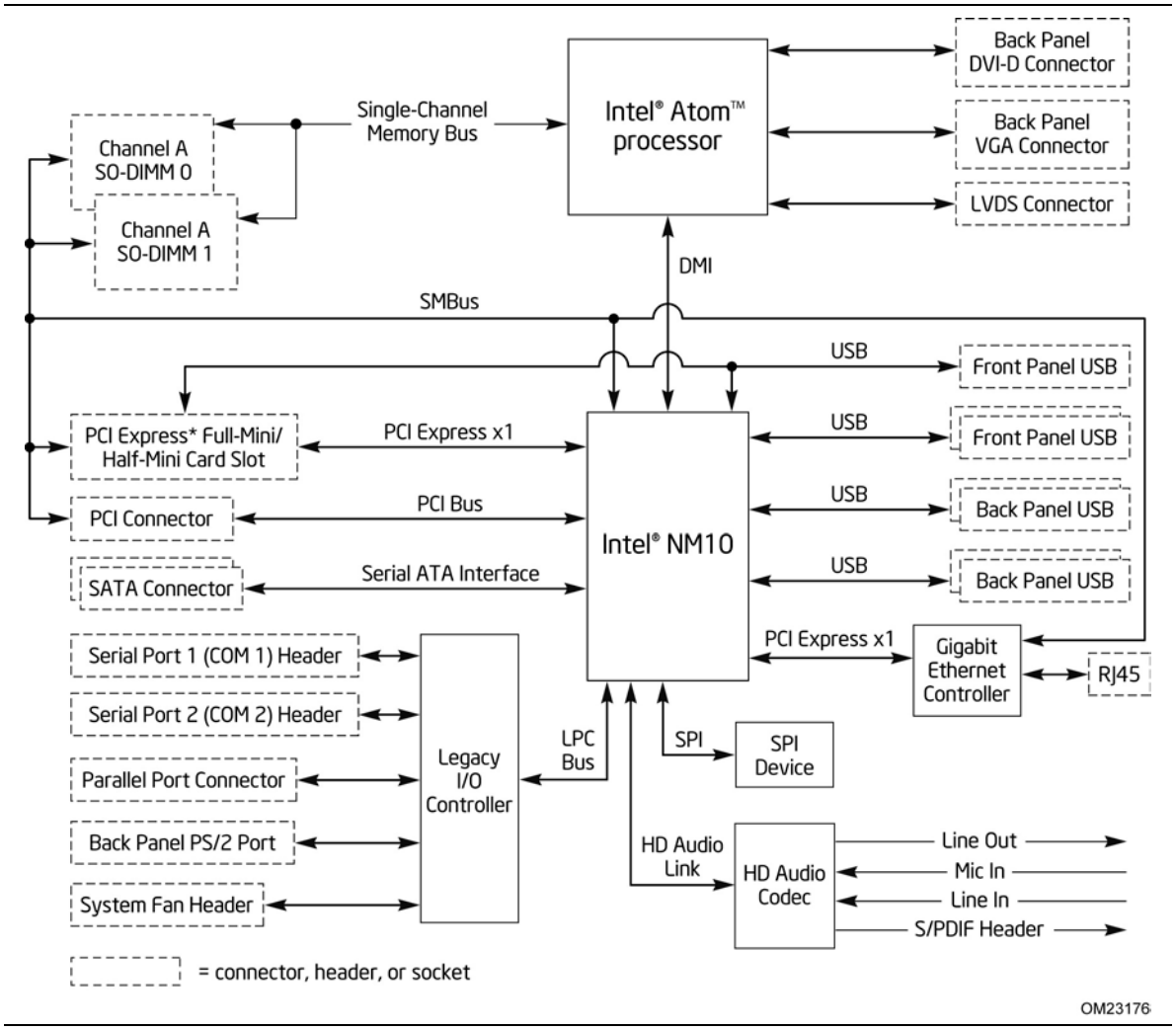


Figure 2. Block Diagram

1.2 Online Support

To find information about...	Visit this World Wide Web site:
Intel Desktop Board D2700MUD	http://www.intel.com/products/motherboard/index.htm
Desktop Board Support	http://www.intel.com/p/en_US/support?iid=hdr+support
Available configurations for the Intel Desktop Board D2700MUD	http://ark.intel.com
Supported processors	http://processormatch.intel.com
Chipset information	http://www.intel.com/products/desktop/chipsets/index.htm
BIOS and driver updates	http://downloadcenter.intel.com
Tested memory	http://www.intel.com/support/motherboards/desktop/sb/CS-025414.htm
Integration information	http://www.intel.com/support/go/buildit

1.3 Processor

The board has a passively-cooled, soldered-down Dual-Core Intel Atom processor with integrated graphics and integrated memory controller.

NOTE

The board is designed to be passively cooled in a properly ventilated chassis. Chassis venting locations are recommended above the processor heatsink area for maximum heat dissipation effectiveness.

For information about	Refer to
Power supply connectors	Section 2.2.2.3, page 51

1.3.1 Intel® D2700 Graphics Subsystem

1.3.1.1 Intel® Graphics Media Accelerator 3650 Graphics Controller (Intel® GMA)

The Intel® GMA 3650 graphics controller features the following:

- 640 MHz core frequency
- High quality texture engine
  - DX9.3* and OpenGL* 3.0 compliant
  - Hardware Pixel Shader 4.1
  - Vertex Shader Model 4.1
- Video
  - Blu-ray* 2.0
  - H.264 & VC1 hardware decoder
  - PAVP 1.1c
  - HDCP1.3
- Display
  - Supports VGA and DVI displays up to 1920 x 1200 at 60 Hz refresh (WUXGA)
  - Supports LVDS displays up to 1440 x 900 (single channel, 24 bpp)
  - Dual independent display support

For information about	Refer to
Obtaining graphics software and utilities	Section 1.2, page 16

1.4 System Memory

The board has two 204-pin DDR3 SO-DIMM sockets and supports the following memory features:

- DDR3 SDRAM SO-DIMMs with gold-plated contacts
- Unbuffered, single-sided or double-sided DIMMs
- 4 GB maximum total system memory
- Minimum total system memory: 256 MB
- Non-ECC DIMMs
- Serial Presence Detect
- DDR3 1066 MHz, DDR3 1333 MHz, DDR3 1600 MHz SO-DIMMs
  (DDR3 1333 MHz and DDR3 1600 MHz memory will run at 1066 MHz)

NOTES

- *Due to passively-cooled thermal constraints, system memory must have an operating temperature rating of 85 °C.*

  The board is designed to be passively cooled in a properly ventilated chassis. Chassis venting locations are recommended above the system memory area for maximum heat dissipation effectiveness.
- *If you are installing only one SO-DIMM, it must be installed in the bottom socket (SO-DIMM 1).*
- *To be fully compliant with all applicable DDR3 SDRAM memory specifications, the board should be populated with SO-DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, performance and reliability may be impacted or the SO-DIMMs may not function under the determined frequency.*

Table 3 lists the supported SO-DIMM configurations.

Table 4. Supported Memory Configurations[1]

Raw Card Version	SO-DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices
B	1 GB	1 Gb	128 M x 8	8
	2 GB	2 Gb	256 M x 8	8
F	2 GB	1 Gb	128 M x 8	16
	4 GB[2]	2 Gb	256 M x 8	16

Notes:

1. System memory configurations are based on availability and are subject to change.
2. Support for one 4 GB SO-DIMM installed in slot 1. Slot 0 must be left empty.

Figure 3 illustrates the memory channel and SO-DIMM configuration.

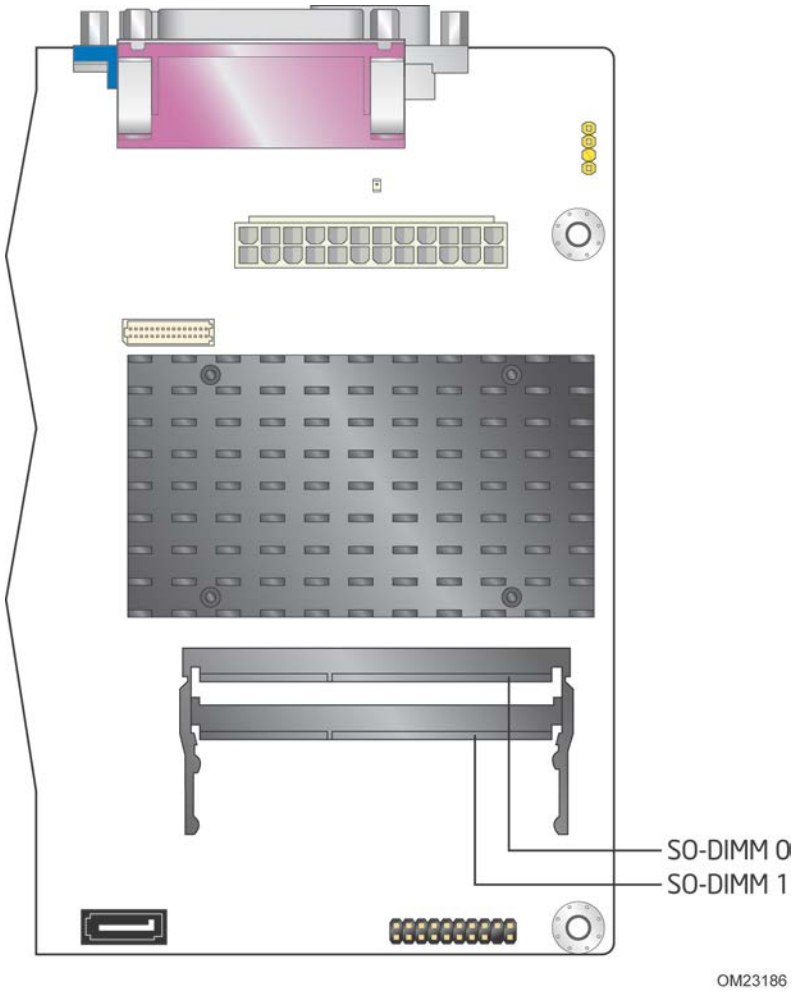


Figure 3. Memory Channel and SO-DIMM Configuration

1.5 Intel® NM10 Express Chipset

The Intel NM10 Express Chipset provides interfaces to the processor and the USB, SATA, LPC, LAN, PCI, and PCI Express interfaces. The Intel NM10 Express Chipset is a centralized controller for the board's I/O paths.

NOTE

The board is designed to be passively cooled in a properly ventilated chassis. Chassis venting locations are recommended above the processor heatsink area for maximum heat dissipation effectiveness.

For information about	Refer to
The Intel NM10 Express chipset	http://www.intel.com/products/desktop/chipsets/index.htm
Resources used by the chipset	Chapter 2

1.5.1.1 Video Memory Allocation

Video memory is allocated from the total available system memory for the efficient balancing of 2-D/3-D graphics performance and overall system performance. Dynamic allocation of system memory to video memory is as follows:

- 256 MB total RAM results in 32 MB video RAM
- 512 MB total RAM results in 64 MB video RAM
- 1 GB total RAM results in 128 MB video RAM
- 2 GB total RAM results in 224 MB video RAM

1.5.1.2 Analog Display (VGA)

The VGA port supports analog displays. The maximum supported resolution is 1920 x 1200 (WUXGA) at a 60 Hz refresh rate. The VGA port is enabled for POST whenever a monitor is attached, regardless of the DVI-D connector status.

1.5.1.3 Digital Visual Interface (DVI-D)

The DVI-D port supports only digital DVI displays. The maximum supported resolution is 1920 x 1200 at 60 Hz refresh. The DVI-D port is compliant with the DVI 1.0 specification.

1.5.1.4 Flat Panel Interface (LVDS)

The flat panel interface (LVDS) supports the following:

- Panel support up to WXGA+ (1440 x 900)
- 25 MHz to 112 MHz single–channel; @18 or 24 bpp
  - TFT panel type
- Panel fitting, panning, and center mode
- CPIS 1.5 compliant
- Spread spectrum clocking
- Panel power sequencing
- Integrated PWM interface for LCD backlight inverter control
- Flat panel brightness control via front panel button input as well as Windows* 7 “Screen brightness” adjustment slider

1.5.1.5 Configuration Modes

For monitors attached to the VGA port, video modes supported by this board are based on the Extended Display Identification Data (EDID) protocol.

Video mode configuration for LVDS displays is supported as follows:

- Automatic panel identification via Extended Display Identification Data (EDID) for panels with onboard EDID support
- Panel selection from common predefined panel types (without onboard EDID)
- Custom EDID payload installation for ultimate parameter flexibility, allowing custom definition of EDID data on panels without onboard EDID
- In addition, BIOS setup provides the following configuration parameters for internal flat panel displays:
- Screen Brightness: allows the end user to set the screen brightness for the display effective through the Power-On Self Test stage (such as while showing the splash screen image and BIOS setup). Windows 7 will ignore this setting in favor of the native “screen brightness” control provided by the operating system.
- Brightness Steps: allows the system integrator to configure the brightness steps for the operating system’s “screen brightness” control (such as the “Screen brightness” adjustment slider under the Windows 7 “Power Options” control panel).
- Flat Panel Configuration Changes Lock: allows the system integrator to “lock” critical settings of the LVDS configuration to avoid end users potentially rendering the display unusable.
- Color Depth: allows the system integrator to select whether the panel is 24 bpp or 18 bpp.
- Inverter Frequency and Polarity: allows the system integrator to set the operating frequency and polarity of the panel inverter board.
- Maximum and Minimum Inverter Current Limit (%): allows the system integrator to set maximum PWM%, as appropriate, according to the power requirements of the internal flat panel display and the selected inverter board.
- Panel Power Sequencing: allows the system integrator to adjust panel sequencing parameters, if necessary.

NOTE

Support for flat panel display configuration complies with the following:

1. *Internal flat panel display connectivity is disabled (and all parameters hidden) by default.*
2. *Internal flat panel display settings are not exposed through Intel® Integrator Toolkit or Intel® Integrator Assistant GUIs.*
3. *Internal flat panel display settings will not be overwritten by loading BIOS setup defaults.*
4. *Internal flat panel display settings will be preserved across BIOS updates.*

1.5.2 USB

The board provides up to seven USB 2.0 ports, supports UHCI and EHCI, and uses UHCI- and EHCI-compatible drivers (four ports routed to the back panel and three ports routed to two front panel USB 2.0 headers). One of the front panel USB headers (brown-colored) supports an Intel Z-U130 USB Solid-State Drive or compatible device.

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

For information about	Refer to
The location of the USB connectors on the back panel	Figure 9, page 41
The location of the front panel USB headers	Figure 11, page 43

1.5.3 SATA Support

The board provides two SATA interface connectors that support one device per connector.

The board's SATA controller offers independent SATA ports with a theoretical maximum transfer rate of 3.0 Gb/s on each port. One device can be installed on each port for a maximum of two SATA devices. A point-to-point interface is used for host to device connections, unlike PATA which supports a master/slave configuration and two devices on each channel.

For compatibility, the underlying SATA functionality is transparent to the operating system. The SATA controller supports IDE and AHCI configuration and can operate in both legacy and native modes. In legacy mode, standard ATA I/O and IRQ resources are assigned (IRQ 14 and 15). In native mode, standard Conventional PCI bus resource steering is used. Native mode is the preferred mode for configurations using the Windows Vista* operating system.

For information about	Refer to
Obtaining AHCI driver	Section 1.2, page 16
The location of the SATA connectors	Figure 11, page 43

1.6 Real-Time Clock Subsystem

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

NOTE

If the battery and AC power fail, custom defaults, if previously saved, will be loaded into CMOS RAM at power-on.

When the voltage drops below a certain level, the BIOS Setup program settings stored in CMOS RAM (for example, the date and time) might not be accurate. Replace the battery with an equivalent one. Figure 1 on page 13 shows the location of the battery.

1.7 Legacy I/O Controller

The Legacy I/O Controller provides the following features:

- Two serial port headers
- One parallel port connector with Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for Conventional PCI bus systems
- PS/2-style keyboard and mouse ports
- Intelligent power management, including a programmable wake-up event interface
- Conventional PCI bus power management support

The BIOS Setup program provides configuration options for the Legacy I/O controller.

For information about	Refer to
The location of the headers	Figure 11, page 43
The serial port headers signal mapping	Table 12, on page 45

1.8 LAN Subsystem

The LAN subsystem consists of the following:

- Intel NM10 Express Chipset
- Intel 82574L Gigabit Ethernet Controller for 10/100/1000 Mb/s Ethernet LAN connectivity
- RJ-45 LAN connector with integrated status LEDs

Additional features of the LAN subsystem include:

- CSMA/CD protocol engine
- LAN connect interface that supports the Ethernet controller
- Conventional PCI bus power management
  - Supports ACPI technology
  - Supports LAN wake capabilities

1.8.1 LAN Subsystem Drivers

LAN drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining LAN drivers	Section 1.2, page 16

1.8.2 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector (shown in Figure 4).

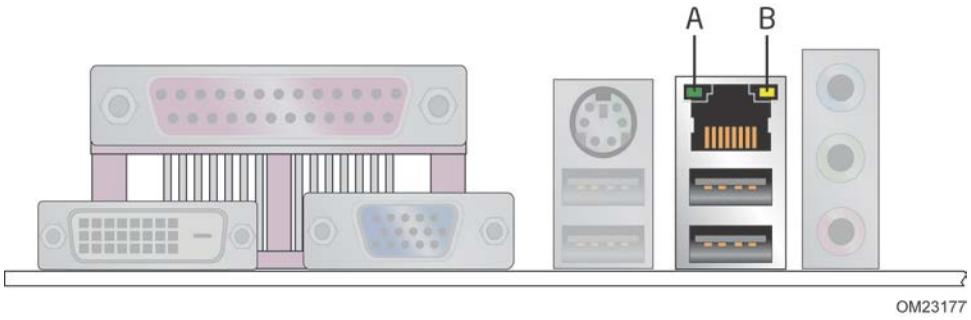


Figure 4. LAN Connector LED Locations

Table 4 describes the LED states when the board is powered up and the Ethernet LAN subsystem is operating.

Table 5. LAN Connector LED States

LED	LED Color	LED State	Condition
Link/Activity (A)	Green	Off	LAN link is not established.
		On	LAN link is established.
		Blinking	LAN activity is occurring.
Link Speed (B)	Green/Yellow	Off	10 Mb/s data rate is selected or negotiated.
		Green	100 Mb/s data rate is selected or negotiated.
		Yellow	1000 Mb/s data rate is selected or negotiated.

1.9 Audio Subsystem

The board supports the Intel® High Definition Audio (Intel® HD Audio) subsystem. The audio subsystem consists of the following:

- Intel NM10 Express Chipset
- Realtek ALC662 audio codec

The audio subsystem has the following features:

- Advanced jack sense for the back panel audio jacks that enables the audio codec to recognize the device that is connected to an audio port. The back panel audio jacks are capable of retasking according to the user's definition, or can be automatically switched depending on the recognized device type.
- Front panel Intel HD Audio and AC '97 audio support.
- 3-port analog audio out stack.
- Windows Vista Basic certification.
- A signal-to-noise (S/N) ratio of 95 dB.

Table 5 lists the supported functions of the front panel and back panel audio jacks.

Table 6. Audio Jack Support

Audio Jack	Micro-phone	Headphones	Line Out (Front Spks)	Line In (Stereo 2)	Mic-In
Front panel – Green		Default			
Front panel – Pink	Default				
Back panel – Blue				Default	
Back panel – Green		(ctrl panel)	Default		
Back panel – Pink					Default

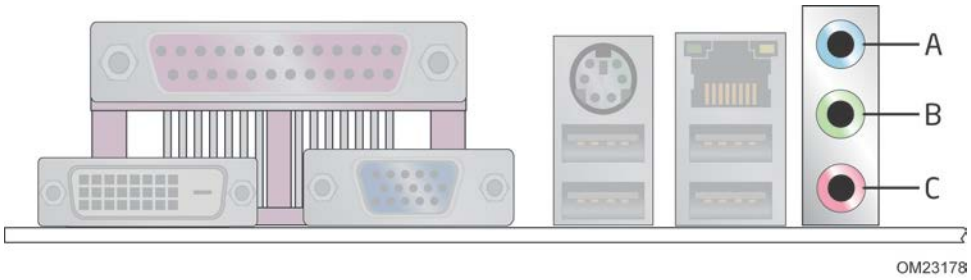
1.9.1 Audio Subsystem Software

Audio software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining audio software and drivers	Section 1.2, page 16

1.9.2 Audio Connectors and Headers

The board contains audio connectors and headers on both the back panel and the component side of the board. The component-side audio headers include front panel audio (a 2 x 5-pin header that provides mic in and line out signals for front panel audio connectors).



Item	Description
A	Line in
B	Line out
C	Mic in

Figure 5. Back Panel Audio Connectors

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.

For information about	Refer to
The locations of the front panel audio header and S/PDIF audio header	Figure 11, page 43
The signal names of the front panel audio header and S/PDIF header	Section 2.2.2.1, page 45

1.10 Hardware Management Subsystem

The hardware management features enable the board to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including the following:

- Thermal monitoring
- Voltage monitoring

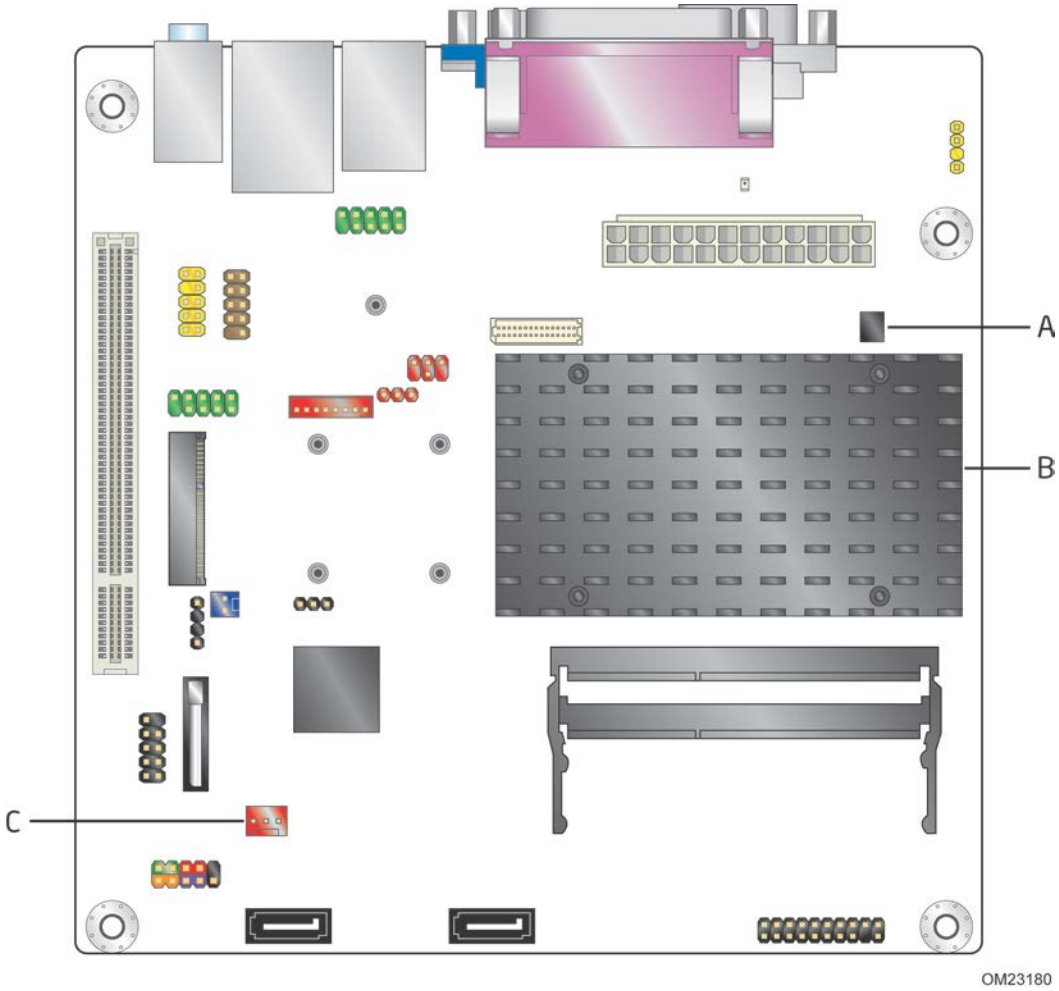
1.10.1 Hardware Monitoring

The hardware monitoring and fan control subsystem is based on the Winbond W83627DHG-P device, which supports the following:

- System ambient temperature monitoring
- System fan speed monitoring
- Power monitoring of +12 V, +5 V, +5 Vstdby, +3.3 V, and +VCCP
- SMBus interface

1.10.2 Thermal Monitoring

Figure 6 shows the locations of the thermal sensors and fan header.



Item	Description
A	Remote thermal sensor
B	DTS, located on the processor die
C	System fan header

Figure 6. Thermal Sensors and Fan Header

1.11 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan header
  - LAN wake capabilities
  - Instantly Available PC technology
  - Wake from USB
  - Wake from PS/2 devices
  - Power Management Event signal (PME#) wake-up support
  - WAKE# signal wake-up support

1.11.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with the board requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 8 on page 32)
- Support for a front panel power and sleep mode switch

Table 6 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 7. Effects of Pressing the Power Switch

If the system is in this state...	...and the power switch is pressed for	...the system enters this state
Off (ACPI G2/G5 – Soft off)	Less than four seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than four seconds	Power-off (ACPI G2/G5 – Soft off)
On (ACPI G0 – working state)	More than four seconds	Fail safe power-off (ACPI G2/G5 – Soft off)
Sleep (ACPI G1 – sleeping state)	Less than four seconds	Wake-up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than four seconds	Power-off (ACPI G2/G5 – Soft off)

1.11.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 7 lists the power states supported by the board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 8. Power States and Targeted System Power

Global States	Sleeping States	Processor States	Device States	Targeted System Power (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state.	Full power > 30 W
G1 – sleeping state	S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G1 – sleeping state	S4 – Suspend to disk. Context saved to disk.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G2/S5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G3 – mechanical off. AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake-up logic, except when provided by battery or external source.	No power to the system. Service can be performed safely.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system's power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

1.11.1.2 Wake-up Devices and Events

Table 8 lists the devices or specific events that can wake the computer from specific states.

Table 9. Wake-up Devices and Events

Devices/events that wake up the system...	...from this sleep state
Power switch	S3, S4, S5 (Note 1)
RTC alarm	S3, S4, S5 (Note 1)
LAN	S3, S4, S5 (Note 1)
USB	S3 (Note 2)
WAKE#	S3, S4, S5 (Note 1)
PME# signal	S3, S4, S5 (Note 1)
Serial port	S3
PS/2 devices	S3, S4, S5 (Notes 1 and 3)

Notes:

1. S4 implies operating system support only.
2. USB ports must be turned off during S4/S5 states.
3. PS/2 wake from S5 should have a selection in the BIOS to enable wake from a combination key (Alt + Print Screen) or the keyboard power button.

NOTE

The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.

1.11.2 Hardware Support

The board provides several power management hardware features, including:

- Power connector
- Fan header
- LAN wake capabilities
- Instantly Available PC technology
- Wake from USB
- Wake from PS/2 devices
- Power Management Event signal (PME#) wake-up support
- WAKE# signal wake-up support
- +5V Standby Power Indicator LED

LAN wake capabilities and Instantly Available PC technology require power from the +5 V standby line.

NOTE

The use of Wake from USB technologies from an ACPI state requires an operating system that provides full ACPI support.

1.11.2.1 Fan Header

The function/operation of the fan header is as follows:

- The fan is on when the board is in the S0 state.
- The fan is off when the board is off or in the S3, S4, or S5 state.
- The system fan header supports closed-loop fan control that can adjust the fan speed and is wired to a fan tachometer input.
- The fan header supports +12 V, 3-wire fans at 1 A maximum.

For information about	Refer to
The locations of the fan header and thermal sensors	Figure 6, page 29
The signal names of the system fan header	Table 17, page 46

1.11.2.2 LAN Wake Capabilities

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem network adapter monitors network traffic at the Media Independent Interface. The board supports LAN wake capabilities with ACPI in the following ways:

- By Ping
- By Magic Packet

Upon detecting the configured wake packet type, the LAN subsystem asserts a wake-up signal that powers up the computer.

1.11.2.3 Instantly Available PC Technology

Instantly Available PC technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the hard drive(s) and fan will power off, the front panel LED will blink). When signaled by a wake-up device or event, the system quickly returns to its last known state. Table 8 on page 32 lists the devices and events that can wake the computer from the S3 state.

The board supports the *PCI Bus Power Management Interface Specification*. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

1.11.2.4 Wake from USB

USB bus activity wakes the computer from an ACPI S3 state.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB and support in the operating system.

1.11.2.5 PME# Signal Wake-up Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S3, S4, or S5 state (with Wake on PME enabled in the BIOS).

1.11.2.6 Wake from PS/2 Devices

PS/2 keyboard activity wakes the computer from an ACPI S3, S4, or S5 state. However, when the computer is in an ACPI S4 or S5 state, the only PS/2 activity that will wake the computer is the Alt + Print Screen or the Power Key available only on some keyboards.

1.11.2.7 WAKE# Signal Wake-up Support

When the WAKE# signal on the PCI Express bus is asserted, the computer wakes from an ACPI S3, S4, or S5 state.

1.11.2.8 Wake from Serial Port

Serial Port activity wakes the computer from an ACPI S3 state.

1.11.2.9 +5 V Standby Power Indicator LED

The +5 V standby power indicator LED shows that power is still present even when the computer appears to be off. Figure 7 shows the location of the standby power indicator LED.

CAUTION

If AC power has been switched off and the standby power indicator is still lit, disconnect the power cord before installing or removing any devices connected to the board. Failure to do so could damage the board and any attached devices.

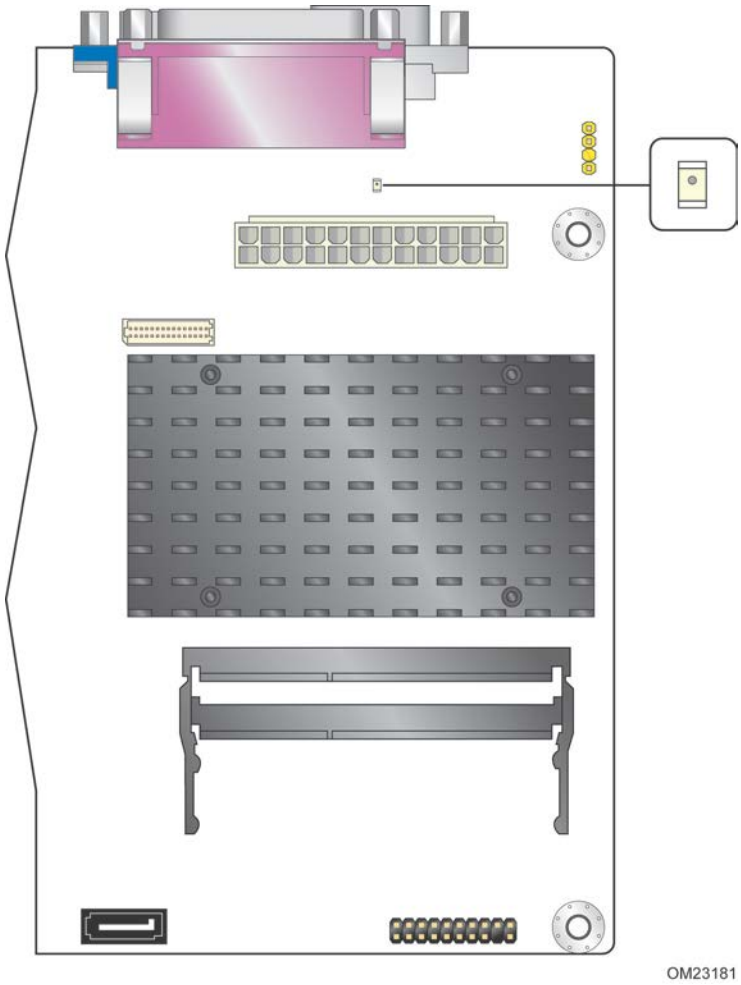


Figure 7. Location of the Standby Power Indicator LED

2 Technical Reference

2.1 Memory Map

2.1.1 Addressable Memory

The board utilizes 4 GB of addressable system memory. Typically the address space that is allocated for Conventional PCI bus add-in cards, PCI Express configuration space, BIOS (SPI Flash), and chipset overhead resides above the top of DRAM (total system memory). On a system that has 4 GB of system memory installed, it is not possible to use all of the installed memory due to system address space being allocated for other system critical functions. These functions include the following:

- BIOS/ SPI Flash (2 MB)
- Local APIC (19 MB)
- Direct Media Interface (40 MB)
- Internal graphics address registers
- Memory-mapped I/O that is dynamically allocated for Conventional PCI add-in cards

The amount of installed memory that can be used will vary based on add-in cards and BIOS settings. Figure 8 shows a schematic of the system memory map. All installed system memory can be used when there is no overlap of system addresses.

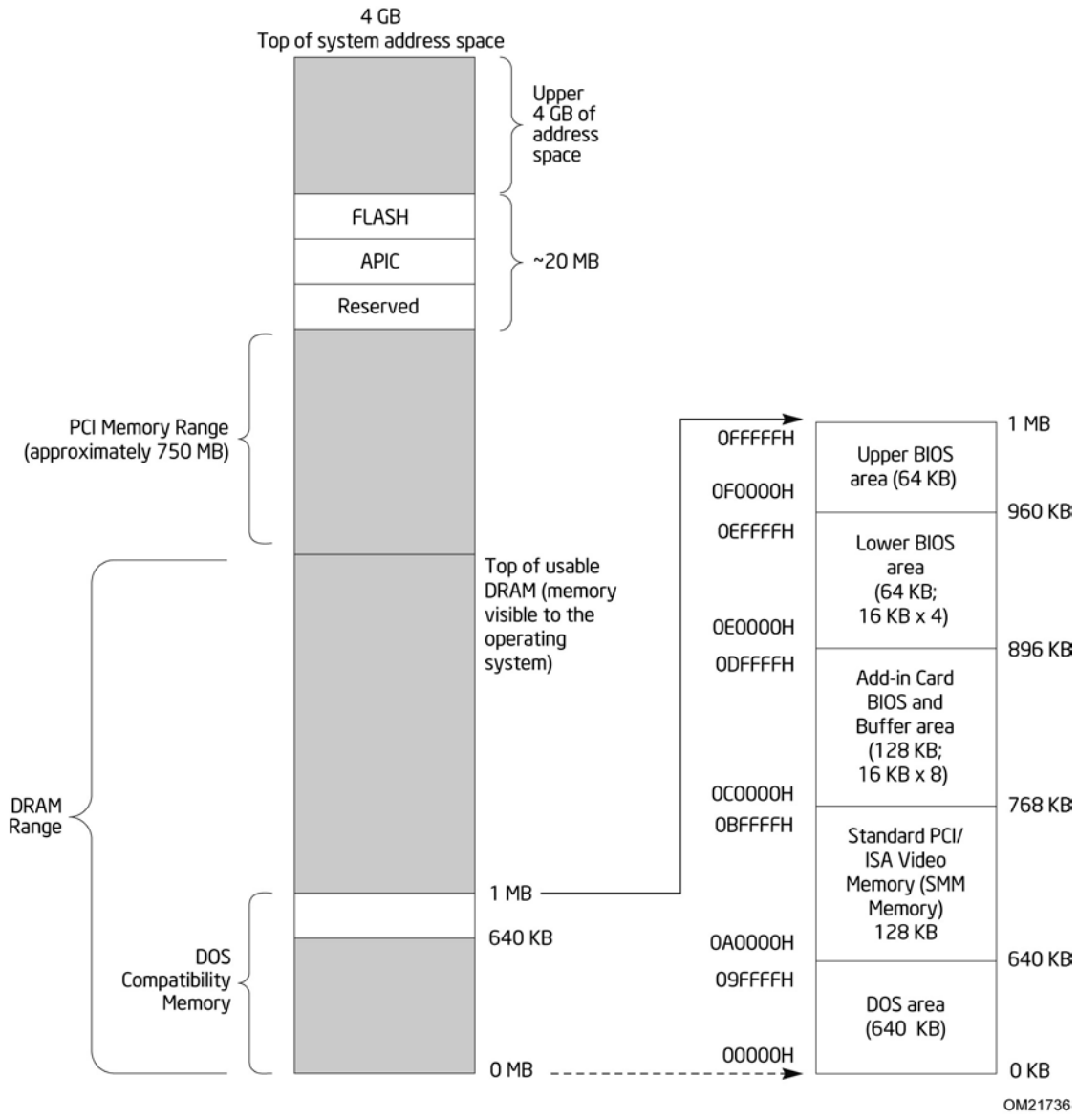


Figure 8. Detailed System Memory Address Map

Table 9 lists the system memory map.

Table 10. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 4194304 K	100000 - FFFFFFFF	4095 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Potential available high DOS memory (open to the PCI bus). Dependent on video adapter used.
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.2 Connectors and Headers

CAUTION

Only the following connectors/headers have overcurrent protection: Back panel and front panel USB, VGA, serial, and PS/2.

The other internal connectors/headers are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors/headers to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the power cable, and the external devices themselves.

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

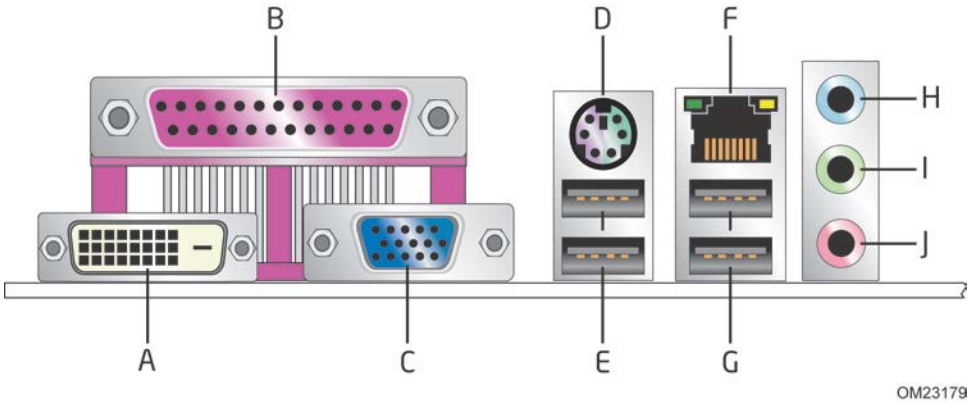
This section describes the board's connectors and headers. The connectors and headers can be divided into these groups:

- Back panel I/O connectors (see page 41)
- Component-side connectors and headers (see page 43)

2.2.1 Back Panel

2.2.1.1 Back Panel Connectors

Figure 9 shows the location of the back panel connectors.



Item	Description
A	DVI-D port
B	Parallel port
C	VGA port
D	PS/2 keyboard/mouse port
E	USB ports
F	LAN port
G	USB ports
H	Line in
I	Line out
J	Mic in

Figure 9. Back Panel Connectors

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.

2.2.1.2 I/O Shield

The I/O shield provided with the board allows access to all back panel connectors and is compatible with standard mini-ITX and microATX chassis. As an added benefit for system configurations with wireless PCI Express Mini Card solutions, the I/O shield also provides pre-cut holes for user installation of up to two external wireless antennas. Figure 10 shows an I/O shield reference diagram.

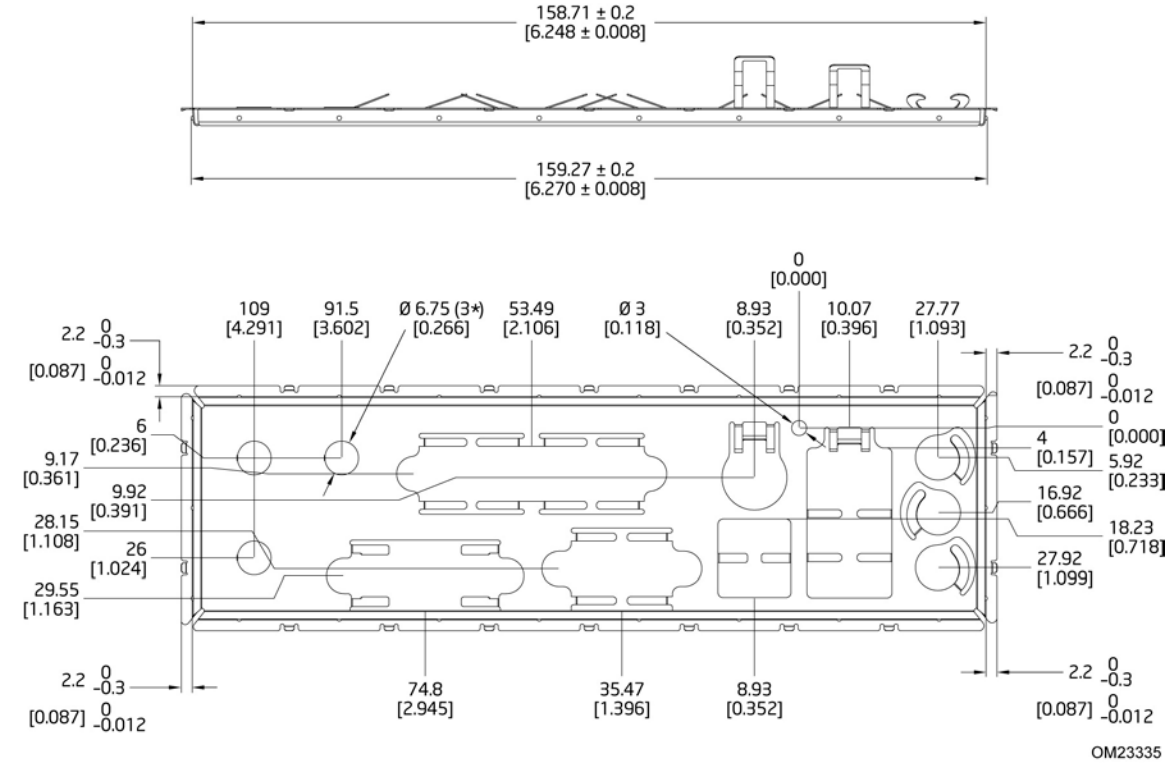


Figure 10. I/O Shield Reference Diagram

2.2.2 Component-side Connectors and Headers

Figure 11 shows the locations of the component-side connectors and headers.

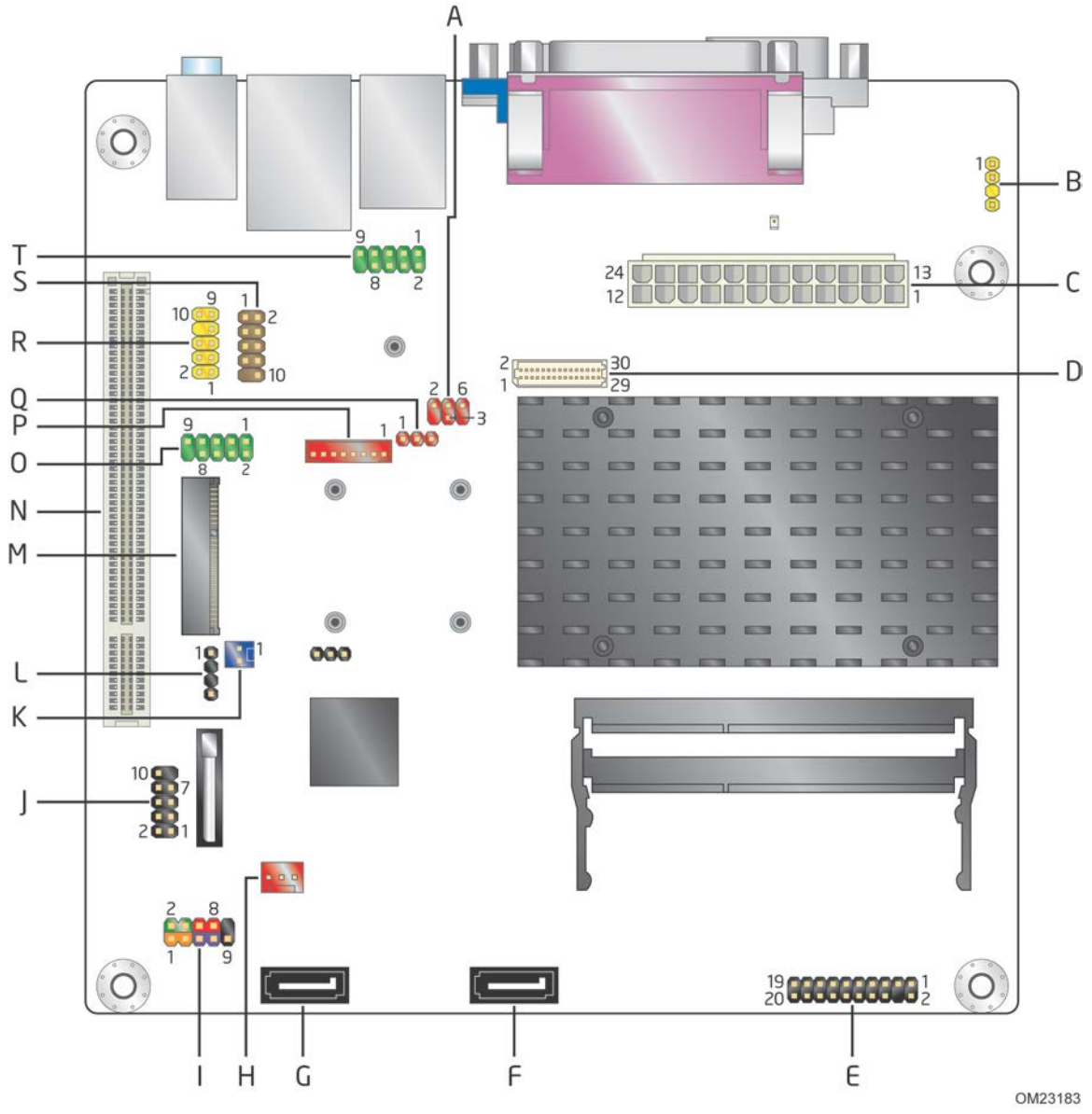


Figure 11. Component-side Connectors and Headers

Table 10 lists the component-side connectors and headers identified in Figure 11.

Table 11. Component-side Connectors and Headers Shown in Figure 11

Item/callout from Figure 11	Description
A	LVDS inverter panel voltage selection jumper
B	S/PDIF header
C	Processor core power connector (2 x 12)
D	LVDS panel connector
E	TPM header
F	SATA connector
G	SATA connector
H	System fan header
I	Front panel header
J	Front panel USB 2.0 header
K	Front panel wireless activity LED header
L	Piezo/monotonic speaker header
M	PCI Express Full-/Half-Mini Card slot
N	Conventional PCI bus add-in card connector
O	Serial port header, COMM 2
P	FPD brightness connector
Q	LVDS inverter power voltage selection jumper
R	Front panel audio header
S	Front panel USB header that supports an Intel Z-U130 USB Solid-State Drive or compatible device (brown-colored)
T	Serial port header, COMM 1

2.2.2.1 Signal Tables for the Connectors and Headers

Table 12. TPM Header

Pin	Signal Name	Pin	Signal Name
1	CK_33M_TPM_DIP	2	Ground
3	LFRAME#	4	Key (no pin)
5	PLTRST#	6	No connection
7	LAD3	8	LAD2
9	+3.3 V	10	LAD1
11	LAD0	12	Ground
13	No connection	14	No connection
15	+3.3 VSB	16	TPM_SERRQ
17	Ground	18	TPM_CLKRUN#
19	LPCPD#	20	No connection

Table 13. Serial Port Headers

Pin	Signal Name	Pin	Signal Name
1	DCD (Data Carrier Detect)	2	RXD# (Receive Data)
3	TXD# (Transmit Data)	4	DTR (Data Terminal Ready)
5	Ground	6	DSR (Data Set Ready)
7	RTS (Request To Send)	8	CTS (Clear To Send)
9	RI (Ring Indicator)	10	Key (no pin)

Table 14. LVDS Data Connector

Pin	Signal Name	Description	Pin	Signal Name	Description
1	LA_CLKN	LVDS Channel A diff clock output - negative	2	NC	
3	LA_CLKP	LVDS Channel A diff clock output - positive	4	NC	
5	EDID_3.3V	Power for EDID ROM	6	EDID_GND	Ground for EDID signaling
7	LA_DATAN0	LVDS Channel A diff data output – negative	8	NC	
9	LA_DATAP0	LVDS Channel A diff data output – positive	10	NC	
11	LA_DATAN1	LVDS Channel A diff data output – negative	12	NC	
13	LA_DATAP1	LVDS Channel A diff data output – positive	14	NC	
15	GND	Ground	16	GND	Ground
17	LA_DATAN2	LVDS Channel A diff data output – negative	18	NC	
19	LA_DATAP2	LVDS Channel A diff data output – positive	20	NC	
21	LA_DATAN3	LVDS Channel A diff data output – negative	22	GND	Ground
23	LA_DATAP3	LVDS Channel A diff data output – positive	24	GND	Ground
25	3.3 V/5 V/12 V	Selectable LCD power output	26	3.3 V/5 V/12 V	Selectable LCD power output
27	3.3 V/5 V/12 V	Selectable LCD power output	28	3.3 V/5 V/12 V	Selectable LCD power output
29	EDID_CLK	EDID/DDC clock signal	30	EDID_DATA	EDID/DDC data signal

Table 15. LVDS Panel Voltage Selection Jumper

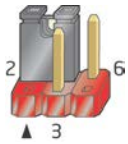
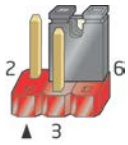
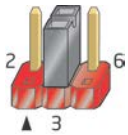
Voltage	Jumper Setting		Configuration
3.3 V	2 and 4		Jumper position for 3.3 V (default)
5 V	6 and 4		Jumper position for 5 V
12 V	3 and 4		Jumper position for 12 V

Table 16. FPD Brightness Connector

Pin	Signal Name	Description
1	BKLT_EN	Backlight enable
2	BKLT_PWM	Backlight control
3	BKLT_PWR (5V/12V)	Backlight inverter power
4	BKLT_PWR (5V/12V)	Backlight inverter power
5	BKLT_GND/Brightness_GND	Ground (shared)
6	BKLT_GND/Brightness_GND	Ground (shared)
7	Brightness_Up	Panel brightness increase
8	Brightness_Down	Panel brightness decrease

Table 17. LVDS Inverter Power Voltage Selection Jumper

Voltage	Jumper Setting		Configuration
5 V	1 and 2		Jumper position for 5 V (default)
12 V	3 and 2		Jumper position for 12 V

Table 18. System Fan Header

Pin	Signal Name
1	Ground
2	+12 V (PWM controlled pulses)
3	Tach

Table 19. SATA Connectors

Pin	Signal Name
1	Ground
2	TXP
3	TXN
4	Ground
5	RXN
6	RXP
7	Ground

Table 20. Front Panel Wireless Activity LED Header

Pin	Signal Name
1	Ground
2	MINICARD_WLAN#

Table 21. Front Panel Audio Header for Intel HD Audio

Pin	Signal Name	Pin	Signal Name
1	[Port 1] Left channel	2	Ground
3	[Port 1] Right channel	4	PRESENCE# (Dongle present)
5	[Port 2] Right channel	6	[Port 1] SENSE_RETURN
7	SENSE_SEND (Jack detection)	8	Key (no pin)
9	[Port 2] Left channel	10	[Port 2] SENSE_RETURN

Table 22. Front Panel Audio Header for AC ’97 Audio

Pin	Signal Name	Pin	Signal Name
1	MIC	2	AUD_GND
3	MIC_BIAS	4	AUD_GND
5	FP_OUT_R	6	FP_RETURN_R
7	AUD_5V	8	KEY (no pin)
9	FP_OUT_L	10	FP_RETURN_L

Table 23. Front Panel USB Header

Pin	Signal Name	Pin	Signal Name
1	+5 VDC	2	+5 VDC
3	D-	4	D-
5	D+	6	D+
7	Ground	8	Ground
9	KEY (no pin)	10	No Connect

Table 24. Front Panel USB Header with Intel Z-U130 USB Solid-State Drive or Compatible Device Support

Pin	Signal Name	Pin	Signal Name
1	+5 VDC	2	NC
3	D-	4	NC
5	D+	6	NC
7	Ground	8	NC
9	KEY (no pin)	10	LED#

2.2.2.2 Add-in Card Connectors

The board has the following add-in card connectors:

- PCI Express Full-/Half-Mini Card slot
- Conventional PCI bus connector (with riser card support for up to two PCI cards)

Note the following considerations for the Conventional PCI bus connector:

- The Conventional PCI bus connector is bus master capable.
- SMBus signals are routed to the Conventional PCI bus connector. This enables Conventional PCI bus add-in boards with SMBus support to access sensor data on the board. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40.
  - The SMBus data line is connected to pin A41.

The Conventional PCI bus connector also supports single-slot and dual-slot riser cards for use of up to two bus master PCI expansion cards. In order to support two PCI bus master expansion cards, the riser card must support the following PCI signal routing:

- Pin A11: additional 33 MHz PCI clock
- Pin B10: additional PCI Request signal (i.e., PREQ#2)
- Pin B14: additional PCI Grant signal (i.e., GNT#2)

NOTE

BIOS IRQ programming for the second PCI slot on PCI riser card:

- *ID_SEL: AD20 (Device 4)*
- *Second PCI slot INT Mapping:*
  - *INT A# (A6) → INT D# of mother board PCI slot.*
  - *INT B# (B7) → INT A# of mother board PCI slot.*
  - *INT C# (A7) → INT B# of mother board PCI slot.*
  - *INT D# (B8) → INT C# of mother board PCI slot.*

NOTE

The Conventional PCI slot on this board does not support the PCI PHOLD[1] function. Due to this limitation (errata), certain PCI cards may experience performance or detection issues when DMA transfer is used as part of the PCI card operation.

[1] *PHOLD is the signal required to hold the bus during DMA transfers.*

2.2.2.3 Power Supply Connector

The board has a 2 x 12 power connector (see Table 24). This board requires a TFX12V or SFX12V power supply.

Table 25. Power Connector

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	13	+3.3 V
2	+3.3 V	14	-12 V
3	Ground	15	Ground
4	+5 V	16	PS-ON# (power supply remote on/off)
5	Ground	17	Ground
6	+5 V	18	Ground
7	Ground	19	Ground
8	PWRGD (Power Good)	20	No connect
9	+5 V (Standby)	21	+5 V
10	+12 V	22	+5 V
11	+12 V	23	+5 V
12	No connect	24	Ground

2.2.2.4 Front Panel Header

This section describes the functions of the front panel header. Table 25 lists the signal names of the front panel header. Figure 12 is a connection diagram for the front panel header.

Table 26. Front Panel Header

Pin	Signal	In/ Out	Description	Pin	Signal	In/ Out	Description
Hard Drive Activity LED				**Power LED**			
1	HD_PWR	Out	Hard disk LED pull-up to +5 V	2	HDR_BLNK_GRN	Out	Front panel green LED
3	HDA#	Out	Hard disk active LED	4	HDR_BLNK_YEL	Out	Front panel yellow LED
Reset Switch				**On/Off Switch**			
5	Ground		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	Ground		Ground
Power				**Not Connected**			
9	+5 V		Power	10	N/C		Not connected

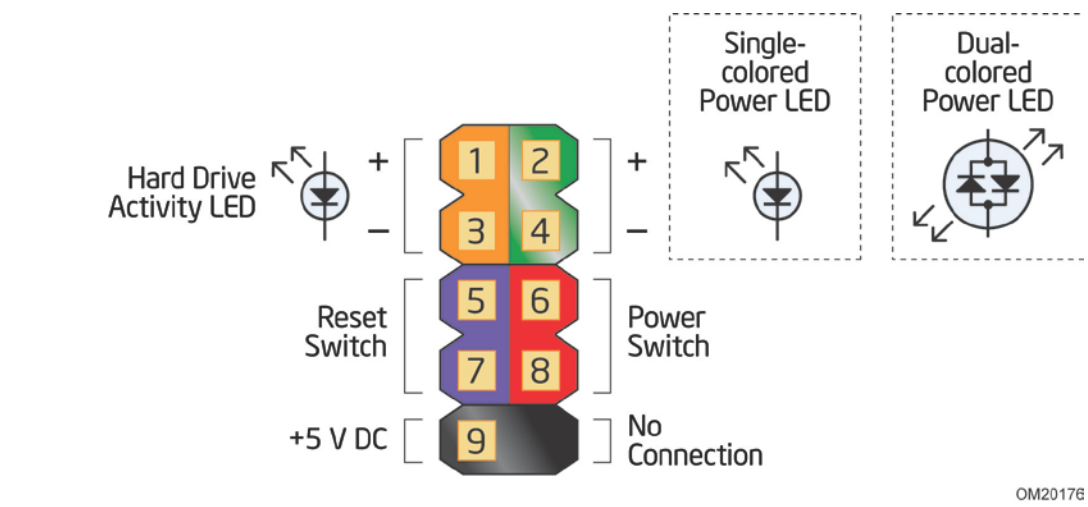


Figure 12. Connection Diagram for Front Panel Header

2.2.2.4.1 Hard Drive Activity LED Header

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive.

2.2.2.4.2 Reset Switch Header

Pins 5 and 7 can be connected to a momentary single pole, single throw (SPST) type switch that is normally open. When the switch is closed, the board resets and runs the POST.

2.2.2.4.3 Power/Sleep LED Header

Pins 2 and 4 can be connected to a single- or dual-color LED. Table 26 shows the default states for a single-color LED.

Table 27. States for a One-Color Power LED

LED State	Description
Off	Power off/hibernate (S5/S4)
Blinking	Sleeping (S3)
Steady Green	Running/Away (S0)

NOTE

The LED states listed in Table 26 are default settings that can be modified through BIOS setup. Systems built with a dual-color front panel power LED can also use alternate color state options.

2.2.2.4.4 Power Switch Header

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply circuitry to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply circuitry will recognize another on/off signal.

2.2.2.5 Front Panel USB Headers

Figure 13 and Figure 14 are connection diagrams for the front panel USB headers.

NOTE

- *The +5 VDC power on the USB headers is fused.*
- *Use only a front panel USB connector that conforms to the USB 2.0 specification for high-speed USB devices.*

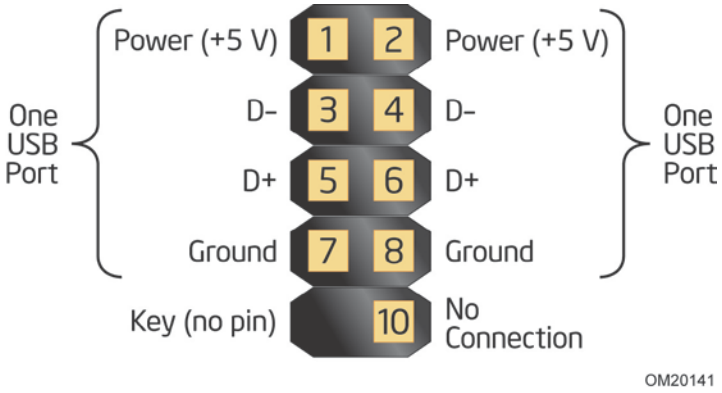


Figure 13. Connection Diagram for Front Panel USB Header

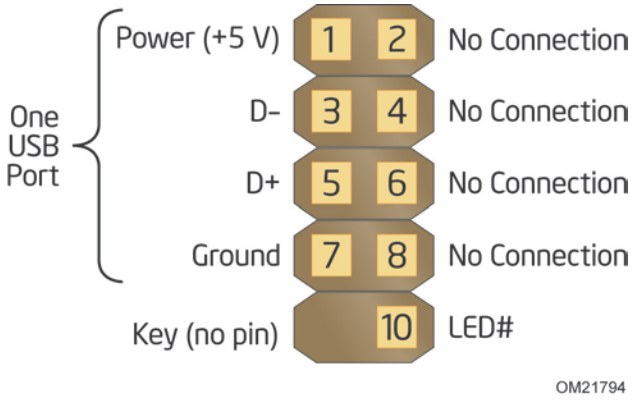


Figure 14. Connection Diagram for Front Panel USB Header with Intel Z-USB Solid-State Drive or Compatible Device Support

2.3 BIOS Configuration Jumper Block

CAUTION

Do not move the jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.

Figure 15 shows the location of the jumper block. The jumper determines the BIOS Setup program's mode. Table 27 lists the jumper settings for the three modes: normal, configure, and recovery.

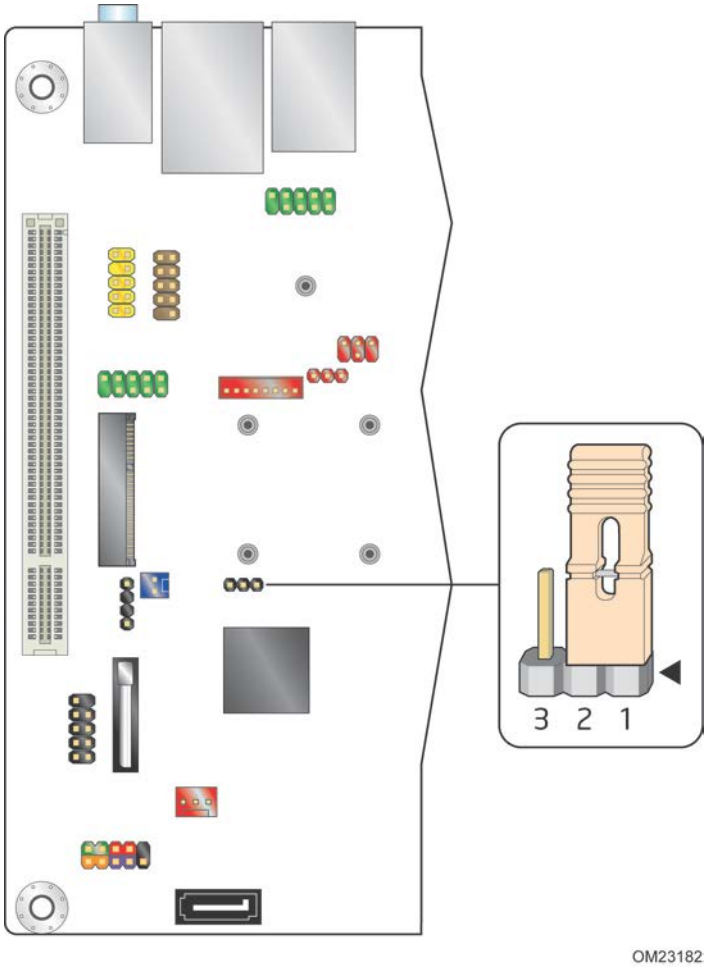


Figure 15. Location of the BIOS Configuration Jumper Block

Table 28. BIOS Configuration Jumper Settings

Function/Mode	Jumper Setting	Configuration
Normal	1-2	The BIOS uses current configuration information and passwords for booting.
Configure	2-3	After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None	The BIOS attempts to recover the BIOS configuration. See Section 3.7 for more information on BIOS recovery.

2.4 Mechanical Considerations

2.4.1 Form Factor

The board is designed to fit into a mini-ITX or microATX form-factor chassis. Figure 16 illustrates the mechanical form factor for the board. Dimensions are given in inches [millimeters]. The outer dimensions are 6.7 inches by 6.7 inches [170 millimeters by 170 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the microATX specification.

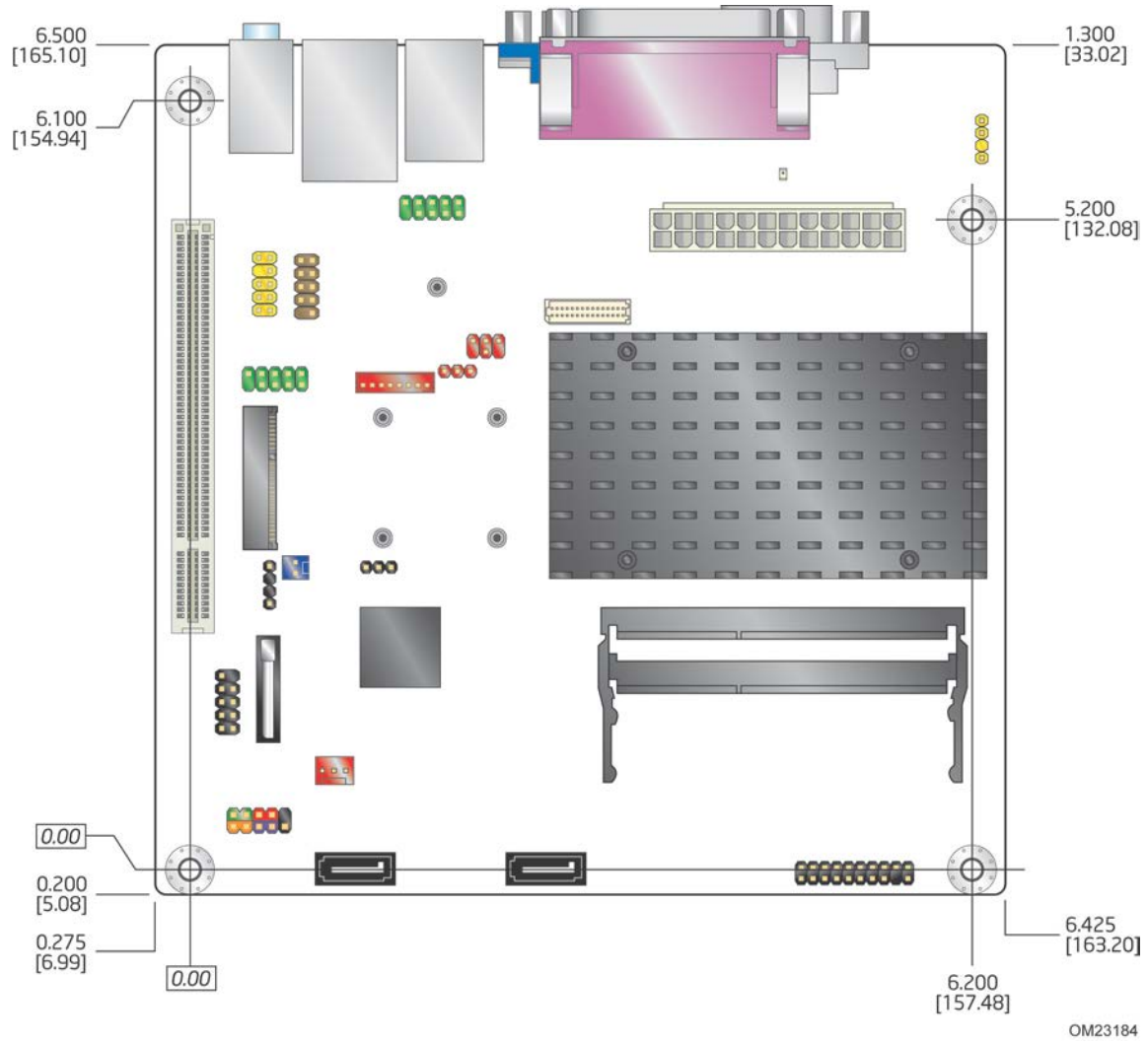


Figure 16. Board Dimensions

2.5 Electrical Considerations

2.5.1 Fan Header Current Capability

Table 28 lists the current capability of the fan header.

Table 29. Fan Header Current Capability

Fan Header	Maximum Available Current
System fan	1.5 A

2.5.2 Add-in Board Considerations

The board is designed to provide 2 A (average) of +5 V current for the Conventional PCI slot. The total +5 V current draw for the Conventional PCI expansion slot (total load) must not exceed 2 A.

2.6 Thermal Considerations

CAUTION

A chassis with a maximum internal ambient temperature of 38 °C at the processor fan inlet is a requirement. Whenever possible, use of a processor heat sink that provides omni-directional airflow to maintain required airflow across the processor voltage regulator area is recommended.

CAUTION

Failure to ensure appropriate airflow may result in reduced performance of both the processor and/or voltage regulator or, in some instances, damage to the board. For a list of chassis that have been tested with Intel Desktop Boards please refer to the following website:

http://www3.intel.com/cd/channel/reseller/asmo-na/eng/tech_reference/53211.htm

All responsibility for determining the adequacy of any thermal or system design remains solely with the system integrator. Intel makes no warranties or representations that merely following the instructions presented in this document will result in a system with adequate thermal performance.

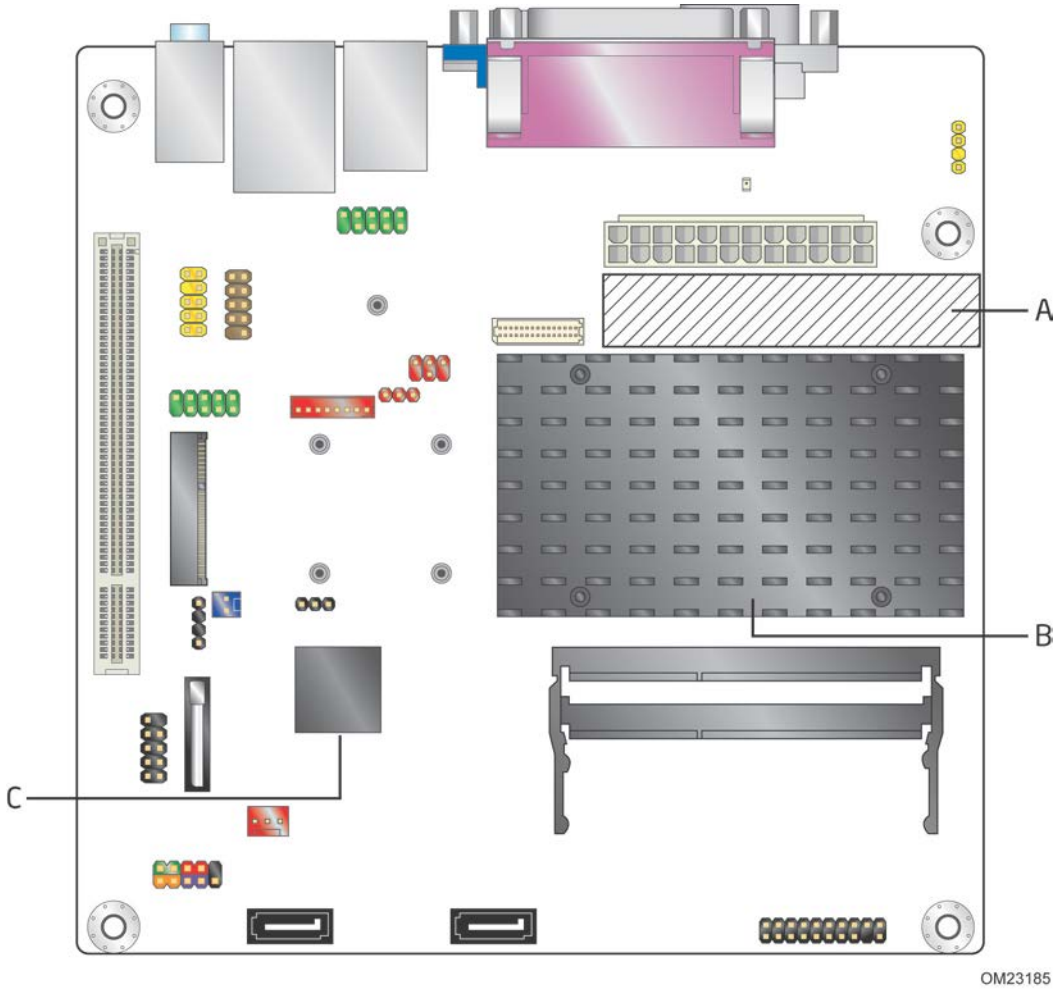
CAUTION

Ensure that the ambient temperature does not exceed the board's maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.9.

CAUTION

Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit. The processor voltage regulator area (shown in Figure 17) can reach a temperature of up to 85 °C in an open chassis.

Figure 17 shows the locations of the localized high temperature zones.



Item	Description
A	Processor voltage regulator area
B	Intel Atom processor
C	Intel NM10 Express Chipset

Figure 17. Localized High Temperature Zones

Table 29 provides maximum case temperatures for the board components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the board.

Table 30. Thermal Considerations for Components

Component	Maximum Case Temperature
Intel Atom processor	100 °C
Processor voltage regulator area	85 °C
Intel NM10 Express Chipset	113 °C
Memory SO-DIMM	85 °C

For information about	Refer to
Processor datasheets and specification updates	Section 1.2, page 16

2.6.1 Passive Heatsink Design in a Passive System Environment

This section highlights important guidelines and related thermal boundary conditions for passive heatsink design in a passive system environment. Passive heatsink describes a thermal solution without a fan attached. Passive system environment describes a chassis with either a power supply fan or a built-in system fan.

This information should be used in conjunction with the Thermal and Mechanical Design Guide (TMDG) published for the Intel Atom processor D2000 series. The TMDG contains detailed package information and thermal mechanical specifications for the processors. The TMDG also contains information on how to enable a completely fanless design provided the right usage scenario and boundary conditions are observed for optimal thermal design. While the TMSDG has a section on thermal design for passive system environments (page 32), the information in this section can also be used to complement the TMDG.

2.6.1.1 Definition of Terms

Term	Description
T_A	The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink.
T_J	Processor junction temperature.
Ψ_{JA}	Junction-to-ambient thermal characterization parameter (psi). A measure of thermal solution performance using total package power. Defined as $(T_J - T_A)/TDP$. Note: Heat source must be specified for Ψ measurements.
TIM	Thermal Interface Material: the thermally conductive compound between the heatsink and the processor die surface. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor die surface to the heatsink.
TDP	Thermal Design Power: a power dissipation target based on worst-case applications. Thermal solutions should be designed to dissipate the thermal design power.
T_A external	The measured external ambient temperature surrounding the chassis. The external ambient temperature should be measured just upstream of the chassis inlet vent.

2.6.1.2 Thermal Specifications Guideline

Terms	Requirements
T_A	≤ 50 °C
T_J	≤ 100 °C
Ψ_{JA}	≤ 3.85 °C/W
TIM	Honeywell PCM45F
TDP	10 W
T_A external	≤ 35 °C

2.6.1.3 Heatsink Design Guideline

Maximum heatsink size (Note)	87 x 52 x 29 mm
Heatsink mass	≤ 63.6 grams
Retention type	Spring loaded fasteners
Heatsink preload	13.2 lb

Note: Refers to the heatsink installed on the board.

2.6.1.4 Chassis Design Guideline

The pin fin heatsink design used on this board will be able to dissipate up to 10 W of processor power in most of the passively enabled system chassis. This board is targeted for 3-7 liters volumetric or larger, desktop/tower orientation, mini-ITX and microATX chassis with a system fan. The recommended fan type is an exhaust fan.

For best thermal performance, it is recommended that the system fan provide reasonable airflow directly over all the major components on the board. The pin fin heatsink is designed to have the best thermal performance when airflow direction is parallel to the heatsink fins.

The processor on the board will generate the highest amount of heat, leading to high ambient temperature within the chassis. The system fan should be located near the board region in order to effectively regulate airflow (see Figure 18). A system fan located further away from the board region, i.e., at the optical disk drive or hard disk drive region, will be less effective in controlling the local ambient temperature. Regardless of where the system fan is located, the maximum local ambient temperature as defined by T_A should be capped at 50 °C. Chassis inlet vents should also provide adequate openings for airflow to pass through. The recommended free-area-ratio of chassis vents should be equal to or greater than 0.53. By using the reference pin fin heatsink, most chassis with a system fan enabled should have local ambient temperature safely below the 50 °C limit.

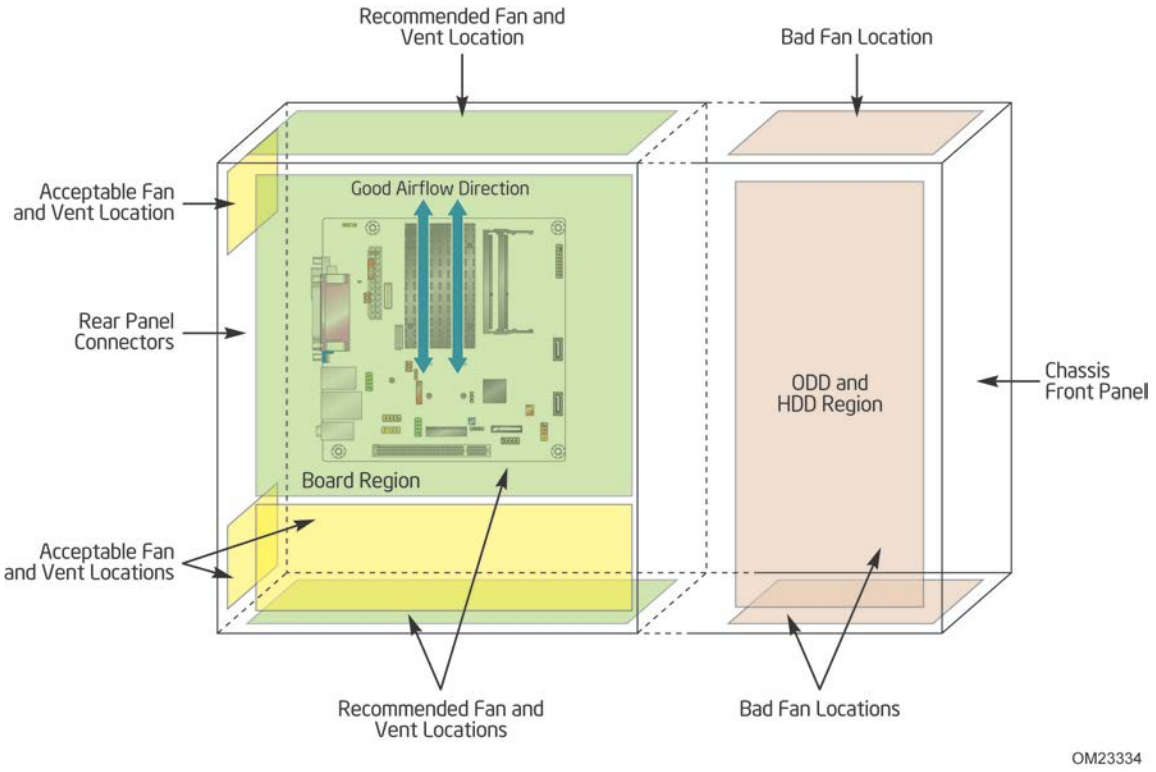


Figure 18. Fan Location Guide for Chassis Selection (Chassis Orientation is Not Restricted)

For all chassis configurations, the heatsink performance parameter, Ψ_{JA} should be less than 3.85 °C/W. The detail thermal measurement metrology is described in the TMSDG. For chassis that fail to meet the thermal specifications guideline highlighted above, an actively cooled heatsink solution should be used.

2.7 Power Consumption

Power measurements were performed to determine bare minimum and likely maximum power requirements from the board, as well as attached devices, in order to facilitate power supply rating estimates for specific system configurations.

2.7.1 Minimum Load Configuration

Minimum load refers to the power demand placed on the power supply when using a bare system configuration with minimal power requirement conditions. Minimum load configuration test results are shown in Table 30. The test configuration was defined as follows:

- 2 GB DDR3/1066 MHz SO-DIMM
- USB keyboard and mouse
- LAN linked at 1000 Mb/s
- DOS booted via network (PXE); system at idle
- All on board peripherals enabled (serial, parallel, audio, …)

Table 31. Minimum Load Configuration Current and Power Results

Output Voltage	3.3 V	5 V	12 V	-12 V	5 VSB
Minimum Load	0.67 A	1.91 A	0.77 A	0.1 A	0.17 A

2.7.2 Maximum Load Configuration

Maximum load refers to the incremental power demands placed on the power supply, augmenting the minimum load configuration into a fully-featured system that stresses power consumption from all subsystems. Maximum load configuration test results are shown in Table 31. The test configuration was defined as follows:

- 4 GB DDR3/1066MHz SO-DIMM
- 14.1-inch LCD via LVDS
- SATA DVD-R/W
  - Load: DVD playback
- 3.5-inch SATA hard disk drive, running Microsoft Windows Vista Home Basic
  - Load: continuous read/write benchmark
- 2.5-inch SATA hard disk drive
  - Load: continuous read/write benchmark
- Intel Z-U130 USB Solid-State Drive or compatible device on the USB flash drive header
  - Load: continuous read/write benchmark
- Wireless card on PCI Express Full-/Half-Mini Card slot, connected via 802.11n protocol
  - Load: continuous read/write benchmark on remote share
- Riser card on conventional PCI slot, populated with PCI LAN card, running file transfer through local network to SATA hard drive

- USB keyboard and mouse
- Back and front panel host-powered USB devices (other than keyboard and mouse)
  - Load: continuous read/write activity on external drive/peripheral
- LAN linked at 1000 Mb/s
  - Load: continuous read/write benchmark on remote share
- All on board peripherals enabled (serial, parallel, audio, …)

Table 32. Maximum Load Configuration Current and Power Results

Output Voltage	3.3 V	5 V	12 V	-12 V	5 VSB
Maximum Load	5 A	7.83 A	2.34 A	0.1 A	0.68 A

2.8 Reliability

The Mean Time Between Failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Telcordia SR-332, Method I Case 1 50% electrical stress, 55 ºC ambient. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The MTBF data was calculated from predicted data at 55 ºC. The Intel Desktop Board D2700MUD has an MTBF of at least 293,676 hours.

2.9 Environmental

Table 32 lists the environmental specifications for the board.

Table 33. Intel Desktop Board D2700MUD Environmental Specifications

Parameter	**Specification**		
Temperature			
Non-Operating	-20 °C to +70 °C		
Operating	0 °C to +50 °C		
Shock			
Unpackaged	50 g trapezoidal waveform		
	Velocity change of 170 inches/second²		
Packaged	Half sine 2 millisecond		
	Product weight (pounds)	Free fall (inches)	Velocity change (inches/s²)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g² Hz sloping up to 0.02 g² Hz		
	20 Hz to 500 Hz: 0.02 g² Hz (flat)		
Packaged	10 Hz to 40 Hz: 0.015 g² Hz (flat)		
	40 Hz to 500 Hz: 0.015 g² Hz sloping down to 0.00015 g² Hz		

3 Overview of BIOS Features

3.1 Introduction

The board uses an Intel BIOS that is stored in the Serial Peripheral Interface Flash Memory (SPI Flash) and can be updated using a disk-based program. The SPI Flash contains the BIOS Setup program, POST, the PCI auto-configuration utility, LAN EEPROM information, and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOSs are identified as MUCDT10N.86A.

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

NOTE

The maintenance menu is displayed only when the board is in configure mode. Section 2.3 on page 55 shows how to put the board in configure mode.

Table 33 lists the BIOS Setup program menu features.

Table 34. BIOS Setup Program Menu Bar

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and displays processor information	Displays processor and memory configuration	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features and power states options	Selects boot options	Saves or discards changes to Setup program options

Table 34 lists the function keys available for menu screens.

Table 35. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (Moves the cursor left or right)
<↑> or <↓>	Selects an item (Moves the cursor up or down)
<Enter>	Executes command or selects the submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

3.2 BIOS Flash Memory Organization

The Serial Peripheral Interface Flash Memory (SPI Flash) includes a 16 Mb (2048 KB) flash memory device.

3.3 Resource Configuration

3.3.1 PCI* Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information. Additional board information can be found in the BIOS under the Additional Information header under the Main BIOS page.

3.5 Legacy USB Support

Legacy USB support enables USB devices to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.
7. Additional USB legacy feature options can be accessed by using Intel Integrator Toolkit.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a USB drive (a flash drive or a USB drive), or an optical drive.
- Intel® Flash Memory Update Utility, which requires booting from DOS. Using this utility, the BIOS can be updated from a file on a hard disk, a USB drive (a flash drive or a USB drive), or an optical drive.
- Intel® F7 switch allows a user to select where the BIOS .bio file is located and perform the update from that location/device. Similar to performing a BIOS Recovery without removing the BIOS configuration jumper.

Both utilities verify that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

For information about	Refer to
BIOS update utilities	http://downloadcenter.intel.com

3.6.1 BIOS Recovery

It is unlikely that anything will interrupt a BIOS update; however, if an interruption occurs, the BIOS could be damaged. Table 35 lists the drives and media types that can and cannot be used for BIOS recovery. The BIOS recovery media does not need to be made bootable.

Table 36. Acceptable Drives/Media Types for BIOS Recovery

Media Type(Note)	Can be used for BIOS recovery?
Optical drive connected to the SATA interface	Yes
USB removable drive (a USB Flash Drive, for example)	Yes
USB diskette drive (with a 1.44 MB diskette)	No
USB hard disk drive	Yes

NOTE: Supported file systems for BIOS recovery:

- *NTFS (sparse, compressed, or encrypted files are not supported)*
- *FAT32*
- *FAT16*
- *FAT12*
- *ISO 9660*

For information about	Refer to
BIOS update instructions	http://www.intel.com/support/motherboards/desktop/sb/CS-022312.htm

3.6.2 Custom Splash Screen

During POST, an Intel® splash screen is displayed by default. This splash screen can be augmented with a custom splash screen. The Intel® Integrator's Toolkit that is available from Intel can be used to create a custom splash screen.

NOTE

If you add a custom splash screen, it will share space with the Intel branded logo.

For information about	Refer to
Intel Integrator Toolkit	http://developer.intel.com/design/motherbd/software/itk/

3.7 Boot Options

In the BIOS Setup program, the user can choose to boot from a hard drive, optical drive, removable drive, or the network. The default setting is for the optical drive to be the first boot device, the hard drive second, removable drive third, and the network fourth.

3.7.1 Optical Drive Boot

Booting from the optical drive is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, the optical drive is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the optical drive, the system will attempt to boot from the next defined drive.

3.7.2 Network Boot

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces booting from the LAN. To use this key during POST, the User Access Level in the BIOS Setup program's Security menu must be set to Full.

3.7.3 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

3.7.4 Changing the Default Boot Device During POST

Pressing the <F10> key during POST causes a boot device menu to be displayed. This menu displays the list of available boot devices (as set in the BIOS setup program's Boot Device Priority submenu). Table 36 lists the boot device menu options.

Table 37. Boot Device Menu Options

Boot Device Menu Function Keys	Description
<↑> or <↓>	Selects a default boot device
<Enter>	Exits the menu, saves changes, and boots from the selected device
<Esc>	Exits the menu without saving changes

3.8 Adjusting Boot Speed

These factors affect system boot speed:

- Selecting and configuring peripherals properly
- Optimized BIOS boot parameters
- Enabling the new Fast Boot feature

3.8.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters such as "power-up to data ready" in less than eight seconds that minimizes hard drive startup delays.
- Select a CD-ROM drive with a fast initialization rate. This rate can influence POST execution time.
- Eliminate unnecessary add-in adapter features, such as logo displays, screen repaints, or mode changes in POST. These features may add time to the boot process.
- Try different monitors. Some monitors initialize and communicate with the BIOS more quickly, which enables the system to boot more quickly.

3.8.2 BIOS Boot Optimizations

Use of the following BIOS Setup program settings reduces the POST execution time.

- In the Boot Menu, set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- In the Peripheral Configuration submenu, disable the LAN device if it will not be used. This can reduce up to four seconds of option ROM boot time.

NOTE

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.

This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from zero to 30 seconds by 5 second increments (using the Hard Disk Pre-Delay feature of the Advanced Menu in the Drive Configuration Submenu of the BIOS Setup program).

3.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.
- For enhanced security, use different passwords for the supervisor and user passwords.
- Valid password characters are A-Z, a-z, and 0-9. Passwords may be up to 16 characters in length.

Table 37 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 38. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

4 Board Status and Error Messages

4.1 BIOS Beep Codes

The BIOS uses audible beep codes to signal status messages and error messages indicating recoverable errors that occur during the POST. The beep codes are listed in Table 38. These beep codes can be heard through a speaker attached to the board's line out audio jack (see Figure 5, B on page 27).

Table 39. BIOS Beep Codes

Type	Pattern	Frequency
BIOS update in progress	None	
Video error (Note)	On-off (1.0 second each) two times, then 2.5-second pause (off), entire pattern repeats (beeps and pause) once and the BIOS will continue to boot.	932 Hz When no VGA option ROM is found.
Memory error	On-off (1.0 second each) three times, then 2.5-second pause (off), entire pattern repeats (beeps and pause) until the system is powered off.	932 Hz
Thermal trip warning	Alternate high and low beeps (1.0 second each) for eight beeps, followed by system shut down.	High beep 2000 Hz Low beep 1500 Hz

Note: Disabled per default BIOS setup option.

4.2 Front-panel Power LED Blink Codes

Whenever a recoverable error occurs during POST, the BIOS causes the board's front panel power LED to blink an error message describing the problem (see Table 39).

Table 40. Front-panel Power LED Blink Codes

Type	Pattern	Note
BIOS update in progress	Off when the update begins, then on for 0.5 seconds, then off for 0.5 seconds. The pattern repeats until the BIOS update is complete.	
Video error (Note)	On-off (1.0 second each) two times, then 2.5-second pause (off), entire pattern repeats (blink and pause) until the system is powered off.	When no VGA option ROM is found.
Memory error	On-off (1.0 second each) three times, then 2.5-second pause (off), entire pattern repeats (blinks and pause) until the system is powered off.	
Thermal trip warning	Each beep will be accompanied by the following blink pattern: .25 seconds on, .25 seconds off, .25 seconds on, .25 seconds off. This will result in a total of 16 blinks.	

Note: Disabled per default BIOS setup option.

4.3 BIOS Error Messages

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem. Table 40 lists the error messages and provides a brief description of each.

Table 41. BIOS Error Messages

Error Message	Explanation
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed, then memory may be bad.
No Boot Device Available	System did not find a device to boot.

4.4 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires a PCI bus add-in card, often called a POST card. The POST card can decode the port and display the contents on a medium such as a seven-segment display.

NOTE

The POST card must be installed in the PCI bus connector.

The following tables provide information about the POST codes generated by the BIOS:

- Table 41 lists the Port 80h POST code ranges
- Table 42 lists the Port 80h POST codes themselves
- Table 43 lists the Port 80h POST sequence

NOTE

In the tables listed above, all POST codes and range values are listed in hexadecimal.

Table 42. Port 80h POST Code Ranges

Range	Subsystem
0x00 – 0x05	Entering SX states S0 to S5.
0x10, 0x20, 0x30	Resuming from SX states (0x10 – 0x20 – S2, 0x30 – S3, etc.)
0x11 – 0x1F	PEI phase pre MRC execution
0x21 – 0x29	MRC memory detection
0x2A – 0x2F	PEI phase post MRC execution
0x31 – 0x35	Recovery
0x36 – 0x3F	Platform DXE driver
0x41 – 0x4F	CPU Initialization (PEI, DXE, SMM)
0x50 – 0x5F	I/O Buses: PCI, USB, ATA etc. 0x5F is an unrecoverable error. Start with PCI.
0x60 – 0x6F	BDS
0x70 – 0x7F	Output devices: All output consoles.
0x80 – 0x8F	For future use
0x90 – 0x9F	Input devices: Keyboard/Mouse.
0xA0 – 0xAF	For future use
0xB0 – 0xBF	Boot Devices: Includes fixed media and removable media. Not that critical since consoles should be up at this point.
0xC0 – 0xCF	For future use
0xD0 – 0xDF	For future use

Table 43. Port 80h POST Codes

Port 80 Code	Progress Code Enumeration
	ACPI S States
0x00,0x01,0x02,0x03,0x04,0x05	Entering S0, S2, S3, S4, or S5 state
0x10,0x20,0x30	Resuming from S2, S3, S4, or S5 state
	PEI before MRC
	PEI Platform driver
0x11	Set boot mode, GPIO init
0x12	Early chipset register programming
0x13	Basic chipset initialization
0x14	LAN init
0x15	Exit early platform init driver
	PEI SMBUS
0x16	SMBUS driver init
0x17	Entry to SMBUS execute read/write
0x18	Exit SMBUS execute read/write
	Memory
0x21	MRC entry point
0x24	Detecting presence of memory DIMMs
0x25	Override Detected DIMM settings
0x27	Configuring memory.
0x28	Testing memory
	PEIMs/Recovery
0x31	Crisis Recovery has initiated
0x33	Loading recovery capsule
0x34	Start recovery capsule / valid capsule is found
	CPU Initialization
	CPU PEI Phase
0x41	Begin CPU PEI Init
0x42	XMM instruction enabling
0x43	End CPU PEI Init
	CPU PEI SMM Phase
0x44	Begin CPU SMM Init smm relocate bases
0x45	Smm relocate bases for APs
0x46	End CPU SMM Init

continued

Table 43. Port 80h POST Codes (continued)

Port 80 Code	Progress Code Enumeration
	CPU DXE Phase
0x47	CPU DXE Phase begin
0x48	Refresh memory space attributes according to MTRRs
0x49	Load the microcode if needed
0x4A	Initialize strings to HII database
0x4B	Initialize MP support
0x4C	CPU DXE Phase End
	CPU DXE SMM Phase
0x4D	CPU DXE SMM Phase begin
0x4E	Relocate SM bases for all APs
0x4F	CPU DXE SMM Phase end
	I/O BUSES
0x50	Enumerating PCI buses
0x51	Allocating resources to PCI bus
0x52	Hot Plug PCI controller initialization
	USB
0x58	Resetting USB bus
0x59	Reserved for USB
	ATA/ATAPI/SATA
0x5A	Resetting PATA/SATA bus and all devices
0x5B	Reserved for ATA
	BDS
0x60	BDS driver entry point initialize
0x61	BDS service routine entry point (can be called multiple times)
0x62	BDS Step2
0x63	BDS Step3
0x64	BDS Step4
0x65	BDS Step5
0x66	BDS Step6
0x67	BDS Step7
0x68	BDS Step8
0x69	BDS Step9
0x6A	BDS Step10
0x6B	BDS Step11
0x6C	BDS Step12
0x6D	BDS Step13
0x6E	BDS Step14
0x6F	BDS return to DXE core (should not get here)

continued

Table 43. Port 80h POST Codes (continued)

Port 80 Code	Progress Code Enumeration
	Keyboard (PS/2 or USB)
0x90	Resetting keyboard
0x91	Disabling the keyboard
0x92	Detecting the presence of the keyboard
0x93	Enabling the keyboard
0x94	Clearing keyboard input buffer
0x95	Instructing keyboard controller to run Self Test (PS/2 only)
	Mouse (PS/2 or USB)
0x98	Resetting mouse
0x99	Detecting mouse
0x9A	Detecting presence of mouse
0x9B	Enabling mouse
	Fixed Media
0xB0	Resetting fixed media
0xB1	Disabling fixed media
0xB2	Detecting presence of a fixed media (IDE hard drive detection etc.)
0xB3	Enabling/configuring a fixed media
	Removable Media
0xB8	Resetting removable media
0xB9	Disabling removable media
0xBA	Detecting presence of a removable media (IDE, CDROM detection etc.)
0xBC	Enabling/configuring a removable media
	DXE Core
0xE4	Entered DXE phase
	BDS
0xE7	Waiting for user input
0xE8	Checking password
0xE9	Entering BIOS setup
0xEB	Calling Legacy Option ROMs
	Runtime Phase/EFI OS Boot
0xF8	EFI boot service ExitBootServices ( ) has been called
0xF9	EFI runtime service SetVirtualAddressMap ( ) has been called

Table 44. Typical Port 80h POST Sequence

POST Code	Description
24	Detecting presence of memory DIMMs
27	Configuring memory
28	Testing memory
33	Loading recovery capsule
E4	Entered DXE phase
50	Enumerating PCI buses
51	Allocating resourced to PCI bus
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
95	Keyboard Self Test
EB	Calling Video BIOS
58	Resetting USB bus
5A	Resetting PATA/SATA bus and all devices
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
5A	Resetting PATA/SATA bus and all devices
28	Testing memory
90	Resetting keyboard
94	Clearing keyboard input buffer
E7	Waiting for user input
00	Ready to boot
A3	Legacy USB driver disconnect

5 Regulatory Compliance and Battery Disposal Information

5.1 Regulatory Compliance

This section contains the following regulatory compliance information for Intel Desktop Board D2700MUD:

- Safety standards
- European Union Declaration of Conformity statement
- Product Ecology statements
- Electromagnetic Compatibility (EMC) standards
- Product certification markings

5.1.1 Safety Standards

Intel Desktop Board D2700MUD complies with the safety standards stated in Table 44 when correctly installed in a compatible host system.

Table 45. Safety Standards

Standard	Title
CSA/UL 60950-1	Information Technology Equipment – Safety - Part 1: General Requirements (USA and Canada)
EN 60950-1	Information Technology Equipment – Safety - Part 1: General Requirements (European Union)
IEC 60950-1	Information Technology Equipment – Safety - Part 1: General Requirements (International)

5.1.2 European Union Declaration of Conformity Statement

We, Intel Corporation, declare under our sole responsibility that the product Intel® Desktop Board D2700MUD is in conformity with all applicable essential requirements necessary for CE marking, following the provisions of the European Council Directive 2004/108/EC (EMC Directive), 2006/95/EC (Low Voltage Directive), and 2002/95/EC (ROHS Directive).

The product is properly CE marked demonstrating this conformity and is for distribution within all member states of the EU with no restrictions.

CE

This product follows the provisions of the European Directives 2004/108/EC, 2006/95/EC, and 2002/95/EC.

Čeština Tento výrobek odpovídá požadavkům evropských směrnic 2004/108/EC, 2006/95/EC a 2002/95/EC.

Dansk Dette produkt er i overensstemmelse med det europæiske direktiv 2004/108/EC, 2006/95/EC & 2002/95/EC.

Dutch Dit product is in navolging van de bepalingen van Europees Directief 2004/108/EC, 2006/95/EC & 2002/95/EC.

Eesti Antud toode vastab Euroopa direktiivides 2004/108/EC, ja 2006/95/EC ja 2002/95/EC kehtestatud nõuetele.

Suomi Tämä tuote noudattaa EU-direktiivin 2004/108/EC, 2006/95/EC & 2002/95/EC määräyksiä.

Français Ce produit est conforme aux exigences de la Directive Européenne 2004/108/EC, 2006/95/EC & 2002/95/EC.

Deutsch Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 2004/108/EC, 2006/95/EC & 2002/95/EC.

Ελληνικά Το παρόν προϊόν ακολουθεί τις διατάξεις των Ευρωπαϊκών Οδηγιών 2004/108/EC, 2006/95/EC και 2002/95/EC.

Magyar E termék megfelel a 2004/108/EC, 2006/95/EC és 2002/95/EC Európai Irányelv előírásainak.

Icelandic Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 2004/108/EC, 2006/95/EC, & 2002/95/EC.

Italiano Questo prodotto è conforme alla Direttiva Europea 2004/108/EC, 2006/95/EC & 2002/95/EC.

Latviešu Šis produkts atbilst Eiropas Direktīvu 2004/108/EC, 2006/95/EC un 2002/95/EC noteikumiem.

Lietuvių Šis produktas atitinka Europos direktyvų 2004/108/EC, 2006/95/EC, ir 2002/95/EC nuostatas.

Malti Dan il-prodott hu konformi mal-provvedimenti tad-Direttivi Ewropej 2004/108/EC, 2006/95/EC u 2002/95/EC.

Norsk Dette produktet er i henhold til bestemmelsene i det europeiske direktivet 2004/108/EC, 2006/95/EC & 2002/95/EC.

Polski Niniejszy produkt jest zgodny z postanowieniami Dyrektyw Unii Europejskiej 2004/108/EC, 206/95/EC i 2002/95/EC.

Portuguese Este produto cumpre com as normas da Diretiva Européia 2004/108/EC, 2006/95/EC & 2002/95/EC.

Español Este producto cumple con las normas del Directivo Europeo 2004/108/EC, 2006/95/EC & 2002/95/EC.

Slovensky Tento produkt je v súlade s ustanoveniami európskych direktív 2004/108/EC, 2006/95/EC a 2002/95/EC.

Slovenščina Izdelek je skladen z določbami evropskih direktiv 2004/108/EC, 2006/95/EC in 2002/95/EC.

Svenska Denna produkt har tillverkats i enlighet med EG-direktiv 2004/108/EC, 2006/95/EC & 2002/95/EC.

Türkçe Bu ürün, Avrupa Birliği'nin 2004/108/EC, 2006/95/EC ve 2002/95/EC yönergelerine uyar.

5.1.3 Product Ecology Statements

The following information is provided to address worldwide product ecology concerns and regulations.

5.1.3.1 Disposal Considerations

This product contains the following materials that may be regulated upon disposal: lead solder on the printed wiring board assembly.

5.1.3.2 Recycling Considerations

As part of its commitment to environmental responsibility, Intel has implemented the Intel Product Recycling Program to allow retail consumers of Intel's branded products to return used products to selected locations for proper recycling.

Please consult the http://www.intel.com/intel/other/ehs/product_ecology for the details of this program, including the scope of covered products, available locations, shipping instructions, terms and conditions, etc.

中文

作为其对环境责任之承诺的部分，英特尔已实施 Intel Product Recycling Program （英特尔产品回收计划），以允许英特尔品牌产品的零售消费者将使用过的产品退还至指定地点作恰当的重复使用处理。

请参考http://www.intel.com/intel/other/ehs/product_ecology 了解此计划的详情，包括涉及产品之范围、回收地点、运送指导、条款和条件等。

Deutsch

Als Teil von Intels Engagement für den Umweltschutz hat das Unternehmen das Intel Produkt-Recyclingprogramm implementiert, das Einzelhandelskunden von Intel Markenprodukten ermöglicht, gebrauchte Produkte an ausgewählte Standorte für ordnungsgemäßes Recycling zurückzugeben.

Details zu diesem Programm, einschließlich der darin eingeschlossenen Produkte, verfügbaren Standorte, Versandanweisungen, Bedingungen usw., finden Sie auf der http://www.intel.com/intel/other/ehs/product_ecology

Español

Como parte de su compromiso de responsabilidad medioambiental, Intel ha implantado el programa de reciclaje de productos Intel, que permite que los consumidores al detalle de los productos Intel devuelvan los productos usados en los lugares seleccionados para su correspondiente reciclado.

Consulte la http://www.intel.com/intel/other/ehs/product_ecology para ver los detalles del programa, que incluye los productos que abarca, los lugares disponibles, instrucciones de envío, términos y condiciones, etc.

Français

Dans le cadre de son engagement pour la protection de l'environnement, Intel a mis en œuvre le programme Intel Product Recycling Program (Programme de recyclage des produits Intel) pour permettre aux consommateurs de produits Intel de recycler les produits usés en les retournant à des adresses spécifiées.

Visitez la page Web http://www.intel.com/intel/other/ehs/product_ecology pour en savoir plus sur ce programme, à savoir les produits concernés, les adresses disponibles, les instructions d'expédition, les conditions générales, etc.

日本語

インテルでは、環境保護活動の一環として、使い終えたインテル ブランド製品を指定の場所へ返送していただき、リサイクルを適切に行えるよう、インテル製品リサイクル プログラムを発足させました。

対象製品、返送先、返送方法、ご利用規約など、このプログラムの詳細情報は、
http://www.intel.com/intel/other/ehs/product_ecology（英語）をご覧ください。

Malay

Sebagai sebahagian daripada komitmennya terhadap tanggungjawab persekitaran, Intel telah melaksanakan Program Kitar Semula Produk untuk membenarkan pengguna-pengguna runcit produk jenama Intel memulangkan produk terguna ke lokasi-lokasi terpilih untuk dikitarkan semula dengan betul.

Sila rujuk http://www.intel.com/intel/other/ehs/product_ecology untuk mendapatkan butir-butir program ini, termasuklah skop produk yang dirangkumi, lokasi-lokasi tersedia, arahan penghantaran, terma & syarat, dsb.

Portuguese

Como parte deste compromisso com o respeito ao ambiente, a Intel implementou o Programa de Reciclagem de Produtos para que os consumidores finais possam enviar produtos Intel usados para locais selecionados, onde esses produtos são reciclados de maneira adequada.

Consulte o site http://www.intel.com/intel/other/ehs/product_ecology (em Inglês) para obter os detalhes sobre este programa, inclusive o escopo dos produtos cobertos, os locais disponíveis, as instruções de envio, os termos e condições, etc.

Russian

В качестве части своих обязательств к окружающей среде, в Intel создана программа утилизации продукции Intel (Product Recycling Program) для предоставления конечным пользователям марок продукции Intel возможности возврата используемой продукции в специализированные пункты для должной утилизации.

Пожалуйста, обратитесь на веб-сайт http://www.intel.com/intel/other/ehs/product_ecology за информацией об этой программе, принимаемых продуктах, местах приема, инструкциях об отправке, положениях и условиях и т.д.

Türkçe

Intel, çevre sorumluluğuna bağımlılığının bir parçası olarak, perakende tüketicilerin Intel markalı kullanılmış ürünlerini belirlenmiş merkezlere iade edip uygun şekilde geri dönüştürmesini amaçlayan Intel Ürünleri Geri Dönüşüm Programı'nı uygulamaya koymuştur.

Bu programın ürün kapsamı, ürün iade merkezleri, nakliye talimatları, kayıtlar ve şartlar v.s dahil bütün ayrıntılarını ögrenmek için lütfen http://www.intel.com/intel/other/ehs/product_ecology

Web sayfasına gidin.

5.1.4 EMC Regulations

Intel Desktop Board D2700MUD complies with the EMC regulations stated in Table 45 when correctly installed in a compatible host system.

Table 46. EMC Regulations

Regulation	Title
FCC 47 CFR Part 15, Subpart B	Title 47 of the Code of Federal Regulations, Part 15, Subpart B, Radio Frequency Devices. (USA)
ICES-003	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)
EN55022	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union)
EN55024	Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union)
EN55022	Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand)
CISPR 22	Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International)
CISPR 24	Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurement. (International)
VCCI V-3, V-4	Voluntary Control for Interference by Information Technology Equipment. (Japan)
KN-22, KN-24	Korean Communications Commission – Framework Act on Telecommunications and Radio Waves Act (South Korea)
CNS 13438	Bureau of Standards, Metrology, and Inspection (Taiwan)

FCC Declaration of Conformity

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation, 5200 N.E. Elam Young Parkway, Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications to the equipment not expressly approved by Intel Corporation could void the user's authority to operate the equipment.

Tested to comply with FCC standards for home or office use.

Canadian Department of Communications Compliance Statement

This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

Le présent appareil numerique német pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la classe B prescrites dans le Réglement sur le broullage radioélectrique édicté par le ministére des Communications du Canada.

Japan VCCI Statement

Japan VCCI Statement translation: This is a Class B product based on the standard of the Voluntary Control Council for Interference from Information Technology Equipment (VCCI). If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＢ情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。
取扱説明書に従って正しい取り扱いをして下さい。

Korea Class B Statement

Korea Class B Statement translation: This equipment is for home use, and has acquired electromagnetic conformity registration, so it can be used not only in residential areas, but also other areas.

이 기기는 가정용(B급) 전자파적합기기로서 주 로 가정에서 사용하는 것을 목적으로 하며, 모 든 지역에서 사용할 수 있습니다.

5.1.5 ENERGY STAR* 5.0, e-Standby, and ErP Compliance

Intel Desktop Board D2700MUD meets the ENERGY STAR requirements listed in Table 46 when used in corresponding system configurations.

Table 47. ENERGY STAR Requirements

ENERGY STAR Specification	Computer Type	Required States	Capability Adjustments	Typical Electricity Consumption (TEC) Criteria
v4.0	Desktop Computer	Idle State (Cat A) Sleep Mode Standby Level	With and without Wake On LAN (Sleep, Standby)	N/A
v4.0	Integrated Computer			
v5.0	Desktop Computer	Off Mode Sleep Mode Idle State Active State	With and without additional internal storage	Cat A under “desktop conventional” and “desktop proxying” operational mode weightings
v5.0	Integrated Desktop Computer			
v5.0	Thin Client	Off Mode Sleep Mode Idle State (Cat B)	With and without Wake On LAN (Sleep, Standby)	N/A

The Desktop Boards also meet the following international requirements:

- Republic of Korea e-Standby program
- European Union Energy-related Products (ErP) directive

For information about	Refer to
ENERGY STAR requirements and recommended configurations	http://www.intel.com/go/energystar
Electronic Product Environmental Assessment Tool (EPEAT)	http://www.epeat.net/
Korea e-Standby Program	http://www.kemco.or.kr/new_eng/pg02/pg02100300.asp
European Union Energy-related Products Directive 2009 (ErP)	http://ec.europa.eu/enterprise/policies/sustainable-business/sustainable-product-policy/ecodesign/index_en.htm

5.1.6 Regulatory Compliance Marks (Board Level)

Intel Desktop Board D2700MUD has the regulatory compliance marks shown in Table 47.

Table 48. Regulatory Compliance Marks

Description	Mark
UL joint US/Canada Recognized Component mark. Includes adjacent UL file number for Intel Desktop Boards: E210882.	
FCC Declaration of Conformity logo mark for Class B equipment.	
CE mark. Declaring compliance to the European Union (EU) EMC directive, Low Voltage directive, and RoHS directive.	
Australian Communications Authority (ACA) and New Zealand Radio Spectrum Management (NZ RSM) C-tick mark. Includes adjacent Intel supplier code number, N-232.	
Japan VCCI (Voluntary Control Council for Interference) mark.	
Korea Certification mark. Includes an adjacent KCC (Korean Communications Commission) certification number: KCC-REM-CPU-D2700MUD.	
Taiwan BSMI (Bureau of Standards, Metrology and Inspections) mark. Includes adjacent Intel company number, D33025.	
Printed wiring board manufacturer's recognition mark. Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (solder side).	V-0
China RoHS/Environmentally Friendly Use Period Logo: This is an example of the symbol used on Intel Desktop Boards and associated collateral. The color of the mark may vary depending upon the application. The Environmental Friendly Usage Period (EFUP) for Intel Desktop Boards has been determined to be 10 years.	

5.2 Battery Disposal Information

CAUTION

Risk of explosion if the battery is replaced with an incorrect type. Batteries should be recycled where possible. Disposal of used batteries must be in accordance with local environmental regulations.

PRÉCAUTION

Risque d'explosion si la pile usagée est remplacée par une pile de type incorrect. Les piles usagées doivent être recyclées dans la mesure du possible. La mise au rebut des piles usagées doit respecter les réglementations locales en vigueur en matière de protection de l'environnement.

FORHOLDSREGEL

Eksplosionsfare, hvis batteriet erstattes med et batteri af en forkert type. Batterier bør om muligt genbruges. Bortskaffelse af brugte batterier bør foregå i overensstemmelse med gældende miljølovgivning.

OBS!

Det kan oppstå eksplosjonsfare hvis batteriet skiftes ut med feil type. Brukte batterier bør kastes i henhold til gjeldende miljølovgivning.

VIKTIGT!

Risk för explosion om batteriet ersätts med felaktig batterityp. Batterier ska kasseras enligt de lokala miljövårdsbestämmelserna.

VARO

Räjähdysvaara, jos pariston tyyppi on väärä. Paristot on kierrätettävä, jos se on maghdollista. Käytetyt paristot on hävitettävä paikallisten ympäristömääräysten mukaisesti.

VORSICHT

Bei falschem Einsetzen einer neuen Batterie besteht Explosionsgefahr. Die Batterie darf nur durch denselben oder einen entsprechenden, vom Hersteller empfohlenen Batterietyp ersetzt werden. Entsorgen Sie verbrauchte Batterien den Anweisungen des Herstellers entsprechend.

AVVERTIMENTO

Esiste il pericolo di un esplosione se la pila non viene sostituita in modo corretto. Utilizzare solo pile uguali o di tipo equivalente a quelle consigliate dal produttore. Per disfarsi delle pile usate, seguire le istruzioni del produttore.

PRECAUCIÓN

Existe peligro de explosión si la pila no se cambia de forma adecuada. Utilice solamente pilas iguales o del mismo tipo que las recomendadas por el fabricante del equipo. Para deshacerse de las pilas usadas, siga igualmente las instrucciones del fabricante.

WAARSCHUWING

Er bestaat ontploffingsgevaar als de batterij wordt vervangen door een onjuist type batterij. Batterijen moeten zoveel mogelijk worden gerecycled. Houd u bij het weggooien van gebruikte batterijen aan de plaatselijke milieuwetgeving.

ATENÇÃO

Haverá risco de explosão se a bateria for substituída por um tipo de bateria incorreto. As baterias devem ser recicladas nos locais apropriados. A eliminação de baterias usadas deve ser feita de acordo com as regulamentações ambientais da região.

AŚCIAROŽZNAŚĆ

Існуе рызыка выбуху, калі заменены акумулятар неправільнага тыпу. Акумулятары павінны, па магчымасці, перепрацоўвацца. Пазбаўляцца ад старых акумулятараў патрэбна згодна з мясцовым заканадаўствам па экалогіі.

UPOZORNÌNÍ

V případě výměny baterie za nesprávný druh může dojít k výbuchu. Je-li to možné, baterie by měly být recyklovány. Baterie je třeba zlikvidovat v souladu s místními předpisy o životním prostředí.

Προσοχή

Υπάρχει κίνδυνος για έκρηξη σε περίπτωση που η μπαταρία αντικατασταθεί από μία λανθασμένου τύπου. Οι μπαταρίες θα πρέπει να ανακυκλώνονται όταν κάτι τέτοιο είναι δυνατό. Η απόρριψη των χρησιμοποιημένων μπαταριών πρέπει να γίνεται σύμφωνα με τους κατά τόπο περιβαλλοντικούς κανονισμούς.

VIGYÁZAT

Ha a telepet nem a megfelelő típusú telepre cseréli, az felrobbanhat. A telepeket lehetőség szerint újra kell hasznosítani. A használt telepeket a helyi környezetvédelmi előírásoknak megfelelően kell kiselejtezni.

注意

異なる種類の電池を使用すると、爆発の危険があります。リサイクルが可能な地域であれば、電池をリサイクルしてください。使用後の電池を廃棄する際には、地域の環境規制に従ってください。

AWAS

Risiko letupan wujud jika bateri digantikan dengan jenis yang tidak betul. Bateri sepatutnya dikitar semula jika boleh. Pelupusan bateri terpakai mestilah mematuhi peraturan alam sekitar tempatan.

OSTRZEŻENIE

Istnieje niebezpieczeństwo wybuchu w przypadku zastosowania niewłaściwego typu baterii. Zużyte baterie należy w miarę możliwości utylizować zgodnie z odpowiednimi przepisami ochrony środowiska.

PRECAUŢIE

Risc de explozie, dacă bateria este înlocuită cu un tip de baterie necorespunzător. Bateriile trebuie reciclate, dacă este posibil. Depozitarea bateriilor uzate trebuie să respecte reglementările locale privind protecţia mediului.

ВНИМАНИЕ

При использовании батареи несоответствующего типа существует риск ее взрыва. Батареи должны быть утилизированы по возможности. Утилизация батарей должна проводится по правилам, соответствующим местным требованиям.

UPOZORNENIE

Ak batériu vymeníte za nesprávny typ, hrozí nebezpečenstvo jej výbuchu.
Batérie by sa mali podľa možnosti vždy recyklovať. Likvidácia použitých batérií sa musí vykonávať v súlade s miestnymi predpismi na ochranu životného prostredia.

POZOR

Zamenjava baterije z baterijo drugačnega tipa lahko povzroči eksplozijo.
Če je mogoče, baterije reciklirajte. Rabljene baterije zavrzite v skladu z lokalnimi okoljevarstvenimi predpisi.

คำเตือน

ระวังการระเบิดที่เกิดจากเปลี่ยนแบตเตอรี่ผิดประเภท หากเป็นไปได้ ควรนำแบตเตอรี่ไปรีไซเคิล การทิ้งแบตเตอรี่ใช้แล้วต้องเป็นไปตามกฎข้อบังคับด้านสิ่งแวดล้อมของท้องถิ่น.

UYARI

Yanlış türde pil takıldığında patlama riski vardır. Piller mümkün olduğunda geri dönüştürülmelidir. Kullanılmış piller, yerel çevre yasalarına uygun olarak atılmalıdır.

ОСТОРОГА

Використовуйте батареї правильного типу, інакше існуватиме ризик вибуху. Якщо можливо, використані батареї слід утилізувати. Утилізація використаних батарей має бути виконана згідно місцевих норм, що регулюють охорону довкілля.

UPOZORNĚNÍ

V případě výměny baterie za nesprávný druh může dojít k výbuchu. Je-li to možné, baterie by měly být recyklovány. Baterie je třeba zlikvidovat v souladu s místními předpisy o životním prostředí.

ETTEVAATUST

Kui patarei asendatakse uue ebasobivat tüüpi patareiga, võib tekkida plahvatusoht. Tühjad patareid tuleb võimaluse korral viia vastavasse kogumispunkti. Tühjade patareide äraviskamisel tuleb järgida kohalikke keskkonnakaitse alaseid reegleid.

FIGYELMEZTETÉS

Ha az elemet nem a megfelelő típusúra cseréli, felrobbanhat. Az elemeket lehetőség szerint újra kell hasznosítani. A használt elemeket a helyi környezetvédelmi előírásoknak megfelelően kell kiselejtezni.

UZMANĪBU

Pastāv eksplozijas risks, ja baterijas tiek nomainītas ar nepareiza veida baterijām. Ja iespējams, baterijas vajadzētu nodot attiecīgos pieņemšanas punktos. Bateriju izmešanai atkritumos jānotiek saskaņā ar vietējiem vides aizsardzības noteikumiem.

DĖMESIO

Naudojant netinkamo tipo baterijas įrenginys gali sprogti. Kai tik įmanoma, baterijas reikia naudoti pakartotinai. Panaudotas baterijas išmesti būtina pagal vietinius aplinkos apsaugos nuostatus.

ATTENZJONI

Riskju ta' splużjoni jekk il-batterija tinbidel b'tip ta' batterija mhux korrett. Il-batteriji għandhom jiġu riċiklati fejn hu possibbli. Ir-rimi ta' batteriji użati għandu jsir skond ir-regolamenti ambjentali lokali.

OSTRZEŻENIE

Ryzyko wybuchu w przypadku wymiany na baterie niewłaściwego typu. W miarę możliwości baterie należy poddać recyklingowi. Zużytych baterii należy pozbywać się zgodnie z lokalnie obowiązującymi przepisami w zakresie ochrony środowiska.