CHENNAI INSTITUTE OF TECHNOLOGY
(Autonomous)

CMOS Circuit Design and Low-Power Techniques at 32 nm using Synopsys

INTRODUCTION:

VLSI design forms the backbone of the modern semiconductor industry, enabling the development of high-performance and low-power integrated circuits used in consumer electronics, automotive systems, and AI applications. The RTL to GDS flow is a critical industrial process that transforms design specifications into manufacturable silicon. A clear understanding of MOSFET fundamentals and transistor-level circuit design is essential for anyone aspiring to build a career in VLSI. This workshop provides a concise and structured introduction to the complete RTL to GDS flow along with the basics of custom circuit design. Participants will gain conceptual clarity on MOSFET operation and CMOS logic, followed by practical exposure to Synopsys Custom Compiler for circuit design and HSPICE for simulation and waveform analysis.

ABSTRACT:

This workshop introduces participants to the fundamentals of VLSI design, starting with an overview of the RTL-to-GDS flow used in ASIC development. It explains MOSFET operating principles using simple analogies and demonstrates how digital circuits are constructed at the transistor level using CMOS logic. Participants will gain hands-on experience in designing basic CMOS circuits using **Synopsys Custom Compiler** and performing HSPICE simulations to study voltage waveforms, timing behaviour, and power trends.

The workshop also briefly introduces low-power design concepts, highlighting how power consumption is controlled in modern semiconductor chips. By the end of the workshop, attendees will understand how

abstract digital designs are translated into physically implemented silicon while meeting timing, area, and power constraints, providing a strong foundation for further learning in VLSI design.

DISCUSSION IN WORKSHOP:

Total Duration: 120 Minutes

Software Required: Synopsys Custom Compiler, HSPICE

TOPIC	DETAILS
1. Introduction to VLSI & ASIC Design	Overview of VLSI industry, ASIC vs FPGA, and importance of RTL to GDS flow.
2.RTL to GDS Flow Basics	Explanation of RTL design, synthesis, placement, routing, DRC, LVS, and GDS generation.
3.MOSFET Fundamentals & Analogy	MOSFET structure, working principle, NMOS vs PMOS.
4.Digital Circuits using MOSFET	CMOS inverter, NAND and NOR gate operation at transistor level.
5.Custom Compiler & HSPICE Simulation	Hands-on demonstration of CMOS inverter schematic design and HSPICE waveform simulation.
6.Low Power Design (Basics)	Dynamic Vs Leakage Power; Clock Gating, Multi-Voltage With Level Shifters, Power Gating With Isolation, Retention Flops (Save/Restore).

PREREQUISITES:

This workshop is beginner-friendly and designed for students from electronics and related disciplines. **No prior VLSI experience is required**. However, a basic understanding of digital logic concepts will be helpful.

All required Synopsys tools and licensed software will be provided on the systems arranged by the organizers. Participants are **not required** to bring their own laptops or install any software.