CHENNAI INSTITUTE OF TECHNOLOGY
(Autonomous)

Cadence 90nm Technology

INTRODUCTION:

Very Large Scale Integration (VLSI) plays a crucial role in the design of modern electronic systems, enabling the integration of millions of transistors on a single chip. Cadence EDA tools are widely used in the semiconductor industry for designing, simulating, and verifying integrated circuits. The 90 nm CMOS technology node represents an important milestone in VLSI design, offering a balance between performance, power consumption, and design complexity, and is extensively used for academic learning and research purposes.

This workshop aims to provide participants with hands-on exposure to Cadence Virtuoso using 90 nm technology. The program introduces the complete custom IC design flow, including schematic design and circuit simulation using industry-standard environments. Participants will gain practical understanding of process design kits (PDKs), design rules, and simulation techniques essential for CMOS circuit development. This workshop is designed to strengthen students' foundational knowledge in VLSI design and prepare them for advanced research and industry-oriented applications.

ABSTRACT:

This workshop provides a focused introduction to VLSI design using Cadence EDA tools with 90 nm CMOS technology. It begins with an overview of the VLSI design flow and familiarizes participants with the Cadence design environment used in industry and academia. The workshop then covers the fundamentals of 90 nm technology, including technology files, process design kits (PDKs), and basic design rules. Participants will gain hands-on experience in schematic design by creating CMOS circuits using Cadence Virtuoso, followed by circuit simulation involving DC and transient analyses through the Analog Design Environment (ADE). The program emphasizes practical learning through guided hands-on sessions, allowing participants to implement designs and clarify doubts through interactive discussions. This workshop aims to strengthen foundational VLSI knowledge and practical skills essential for advanced IC design and research.

Total duration: 120 minutes

Software Required: Cadence Virtuoso Design Suite (Pre-installed in the laboratory systems)

Session Details

Session	Details
1. Introduction to VLSI & Cadence	Introduction to VLSI concepts and an overview of the complete custom IC design flow, along with familiarization of Cadence EDA tools used in industry and academia.
2. 90 nm Technology Overview	Explanation of 90 nm CMOS technology, including technology files, process design kit (PDK) structure, and fundamental design rules essential for circuit implementation.
3. Schematic Design	Hands-on creation of CMOS circuit schematics using Cadence Virtuoso, focusing on correct connectivity, device sizing, and design methodology.
4. Simulation	Performing DC and transient analyses using the Cadence Analog Design Environment (ADE) to verify circuit functionality and analyze performance parameters.
5. Hands-on Practice & Q&A	Guided practical session allowing participants to implement designs independently, followed by interactive discussion for doubt clarification and troubleshooting.

Prerequisites:

1. Basic understanding of **semiconductor devices** and **CMOS fundamentals**
2. Familiarity with **digital and analog electronics** concepts
3. Introductory knowledge of **VLSI design principles** (preferred)
4. Basic awareness of **Linux operating system commands**
5. Willingness to participate in **hands-on laboratory sessions**