

E

D

C

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6

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1

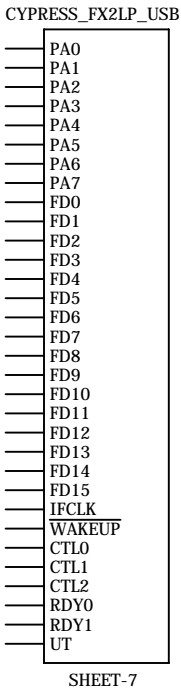
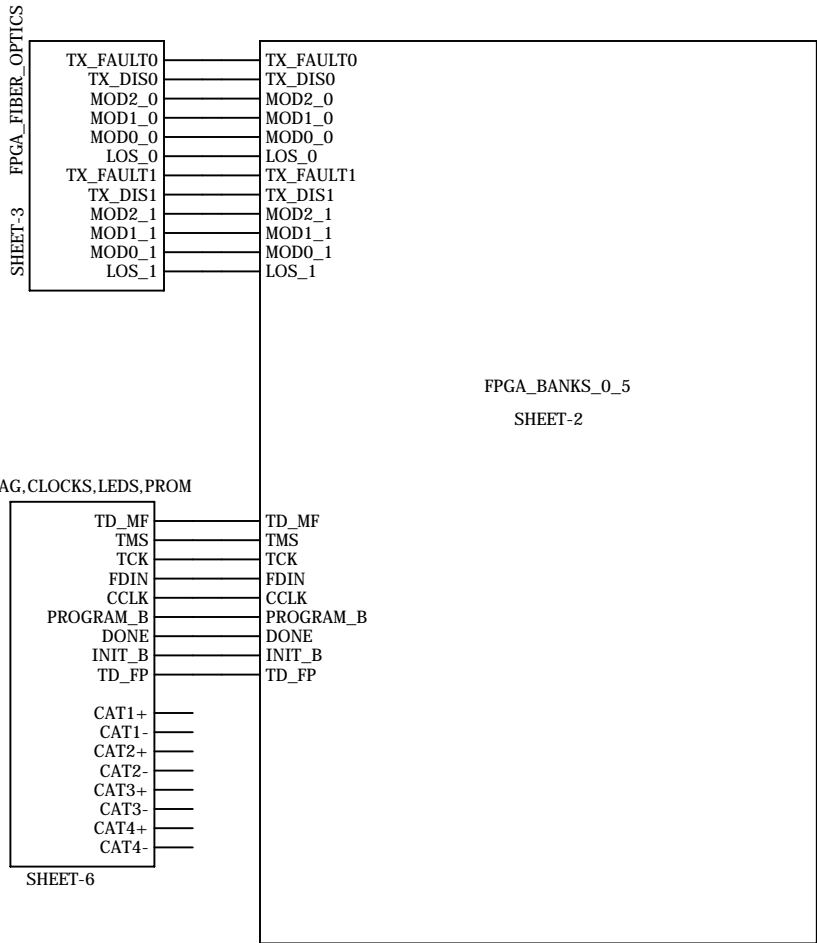
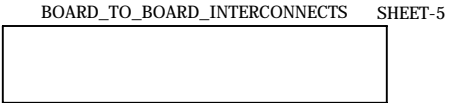
E

D

C

B

A



Assembly instructions:

install 2mm 2 pin jumper header 156_DIS and 250_DIS

install GND test points

notes updated 2012-05-16

added size/package notes to schematic

notes updated 2012-10-05

added notes about bank voltages and N18/M18/L10/K10/J2/M10

2013-10-09

pcb: changed 2 pin molex connector to use bigger holes

2013-10-10

sch: changed thermal wall holes to be the skinny type

2013-10-25:

forgot pullup on $\overline{\text{shdn}}$ net for regulators

holes for power connector too small

changed note on what switch #4 does

2013-10-31:

be careful wiring up the 2 pin power connector; pin 1 on the schematic doesn't correspond to pin 1 on the connector

2014-01-09

FPGA is XC6SLX150T-3FGG676I (RoHS; speed grade 3; industrial temp)

2014-02-12:

noticed that DIP sw for disconnecting cypress eeprom should probably be on other side of pull-up resistor

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A3
IDLAB design #:	IDL_13_037
circuit design:	LJR, MZA, GSV, KAN
PCB design:	LJR, MZA
sheet #:	1 of 7
sheet description:	block diagram
date last modified:	2014-02-12

A

A

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A3
IDLAB design #:	IDL_13_037
circuit design:	LJR, MZA, GSV, KAN
PCB design:	LJR, MZA
sheet #:	2 of 7
sheet description:	FPGA banks 0-5
date last modified:	2014-02-12

6

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E

D

C

B

A

E

D

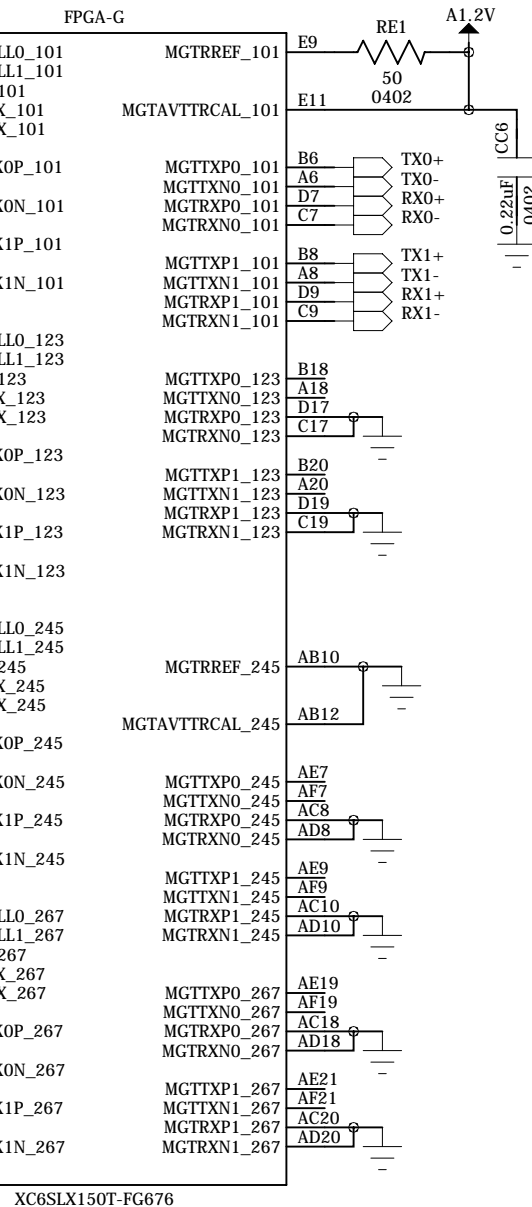
C

B

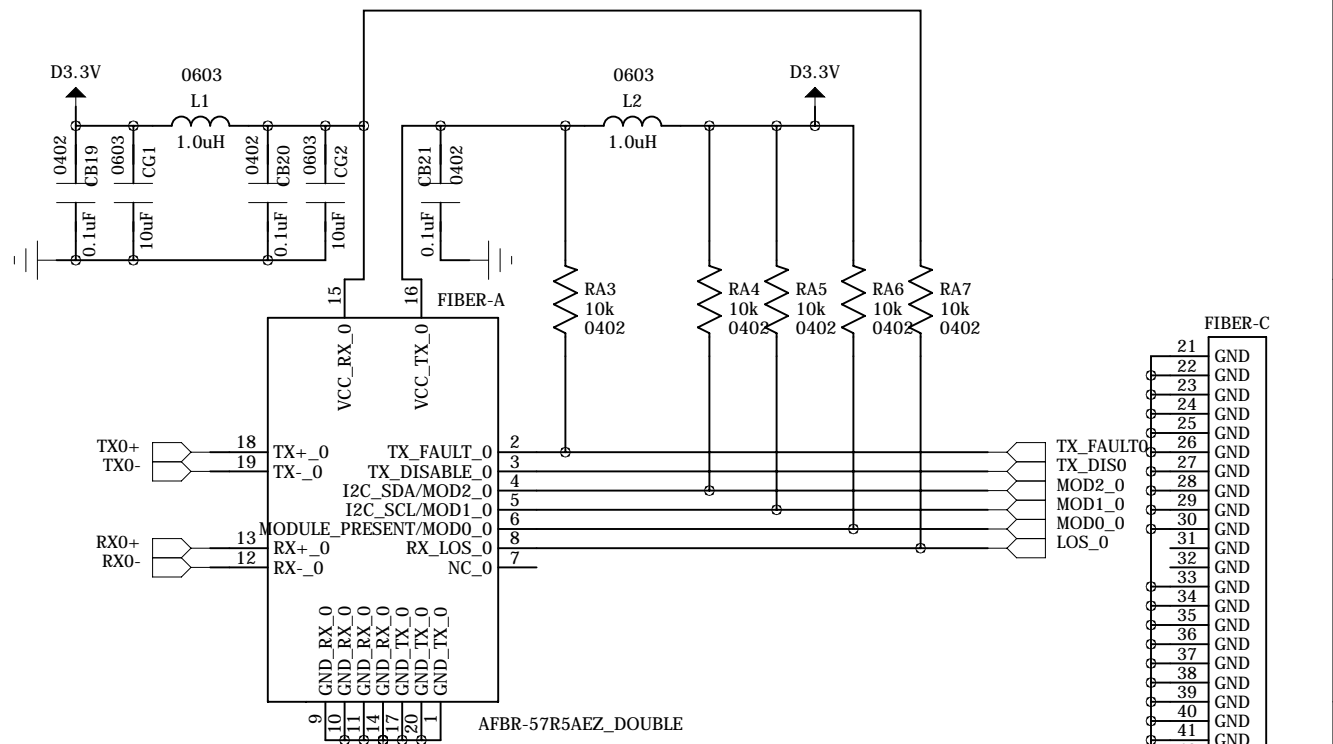
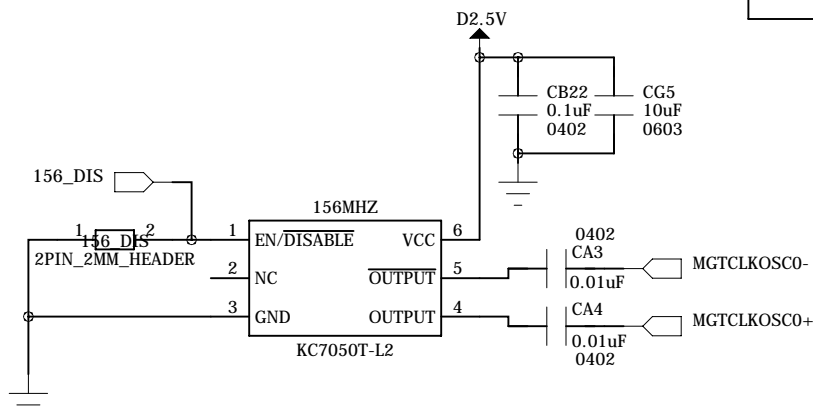
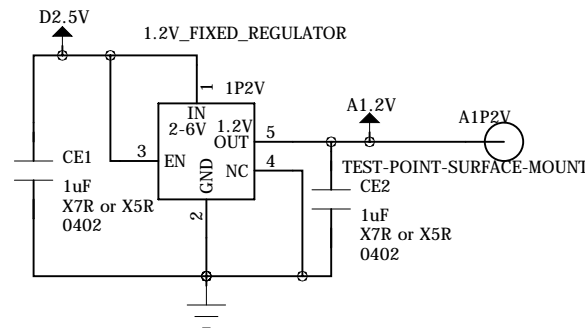
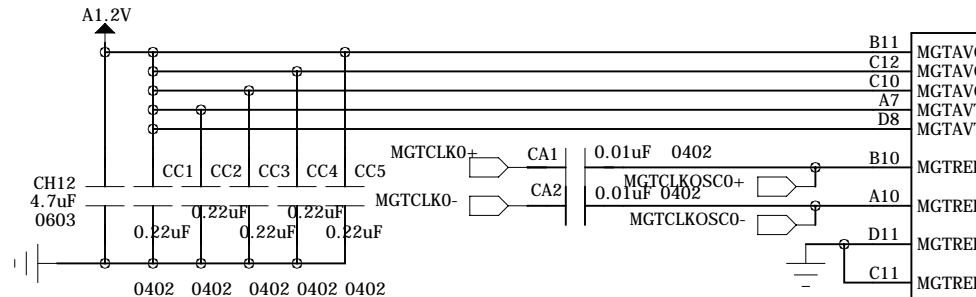
A

110.1mA per lane (ds162 page 12)

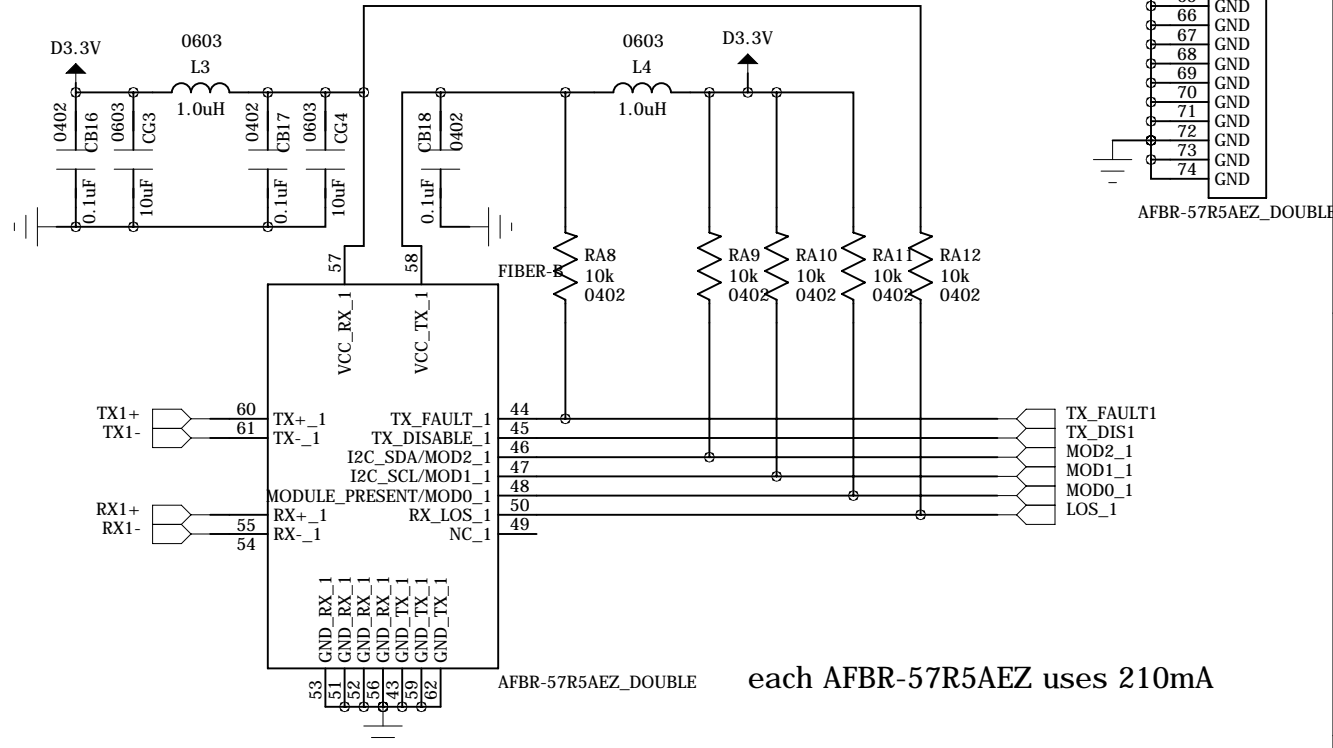
FPGA-G



XC6SLX150T-FG676



I2C addresses = 1010000, 1010001



I2C addresses = 1010000, 1010001

each AFBR-57R5AEZ uses 210mA

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High Energy Physics Group
Instrumentation Development Lab

title: SCROD
revision: A3
IDLAB design #: IDL_13_037
circuit design: LJR, MZA, GSV, KAN
PCB design: LJR, MZA

sheet #: 3 of 7
sheet description: fiber transceiver, fiber clock
date last modified: 2014-02-12

E

D

C

B

A

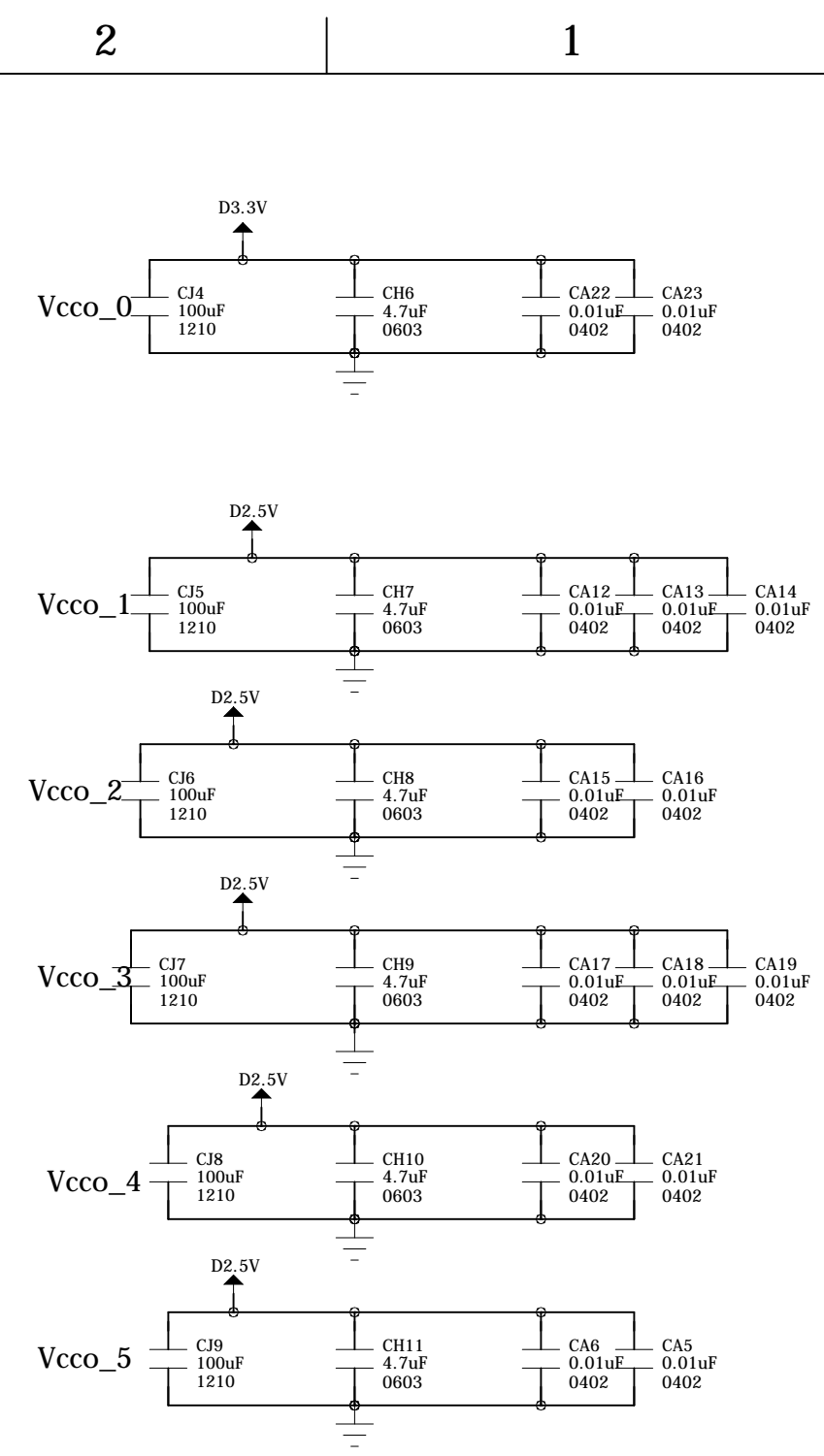
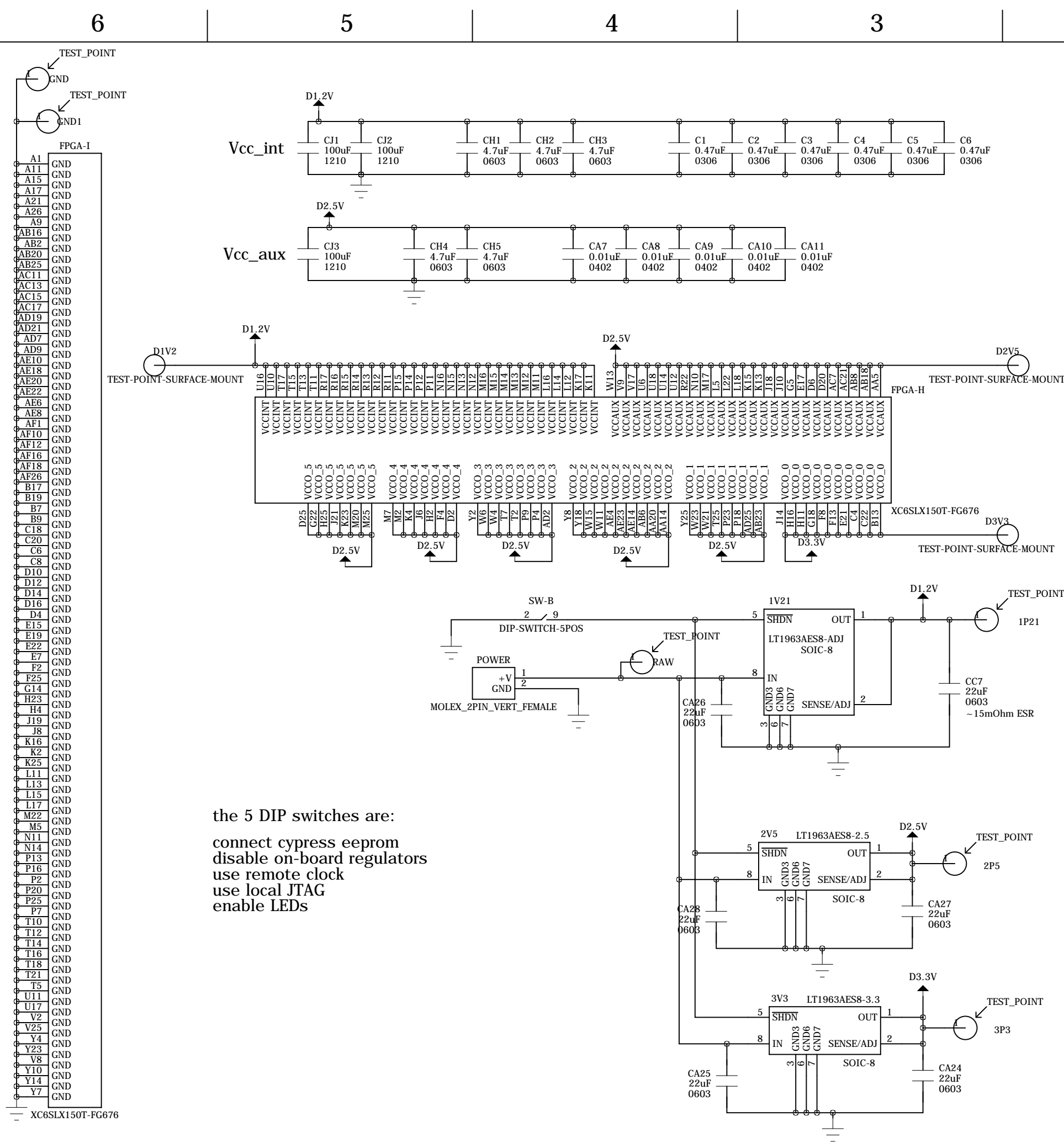
E

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A



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A3
IDLAB design #:	IDL_13_037
circuit design:	LJR, MZA, GSV, KAN
PCB design:	LJR, MZA
sheet #:	4 of 7
sheet description:	FPGA power, FPGA caps
date last modified:	2014-02-12

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A3
IDLAB design #:	IDL_13_037
circuit design:	LJR, MZA, GSV, KAN
PCB design:	LJR, MZA
sheet #:	5 of 7
sheet description:	board-to-board interconnects
date last modified:	2014-02-12

E

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E

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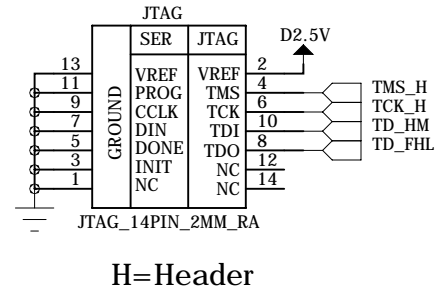
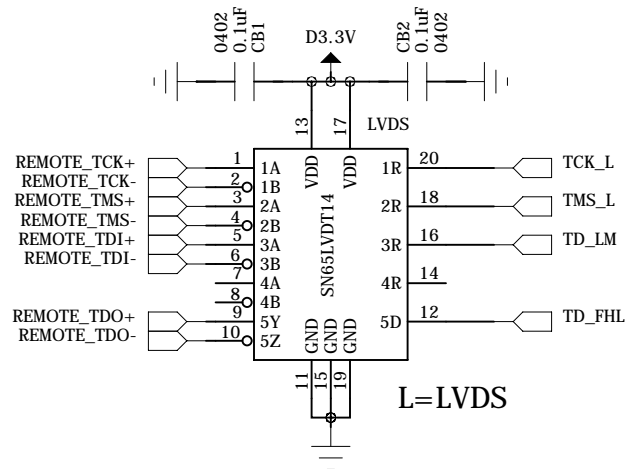
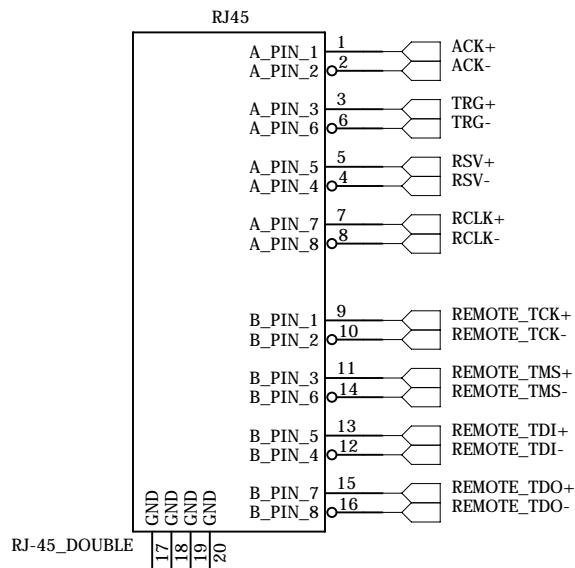
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4

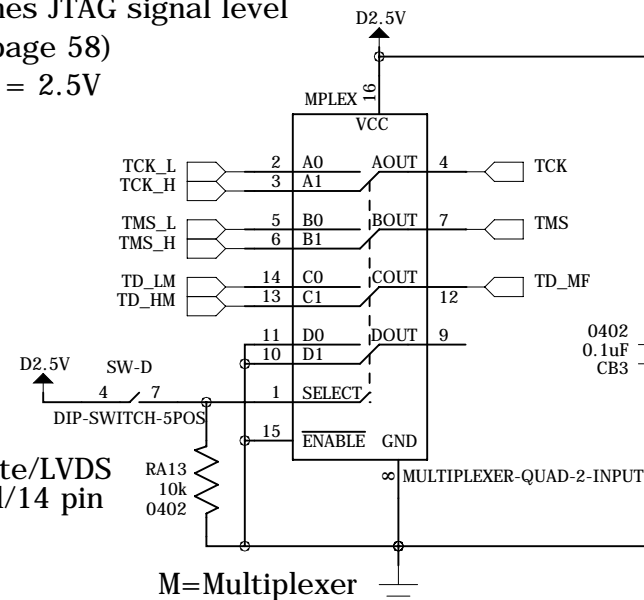
3

2

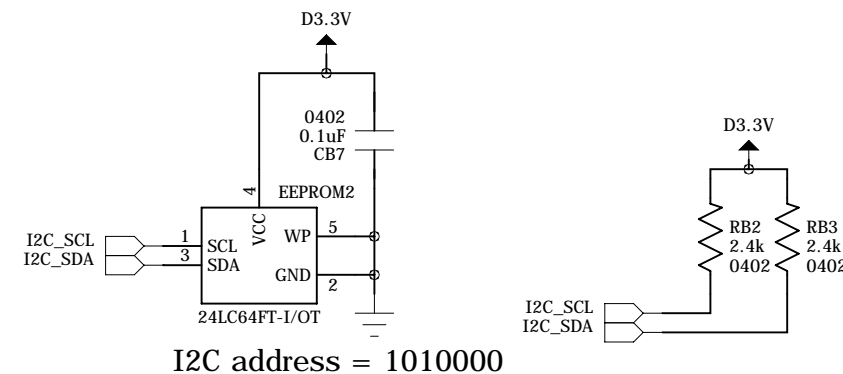
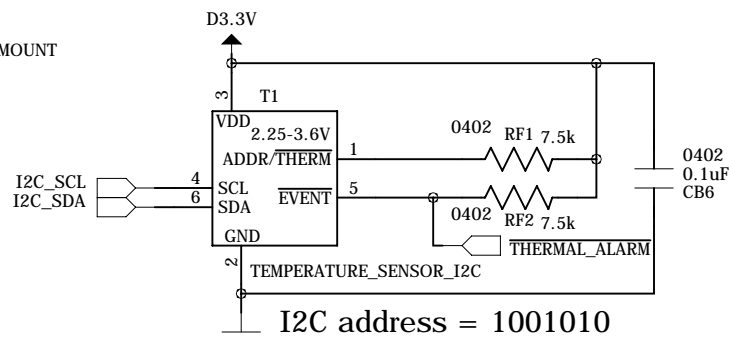
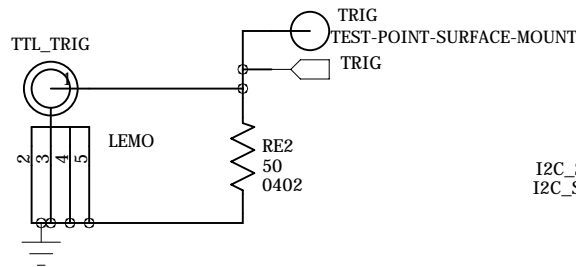
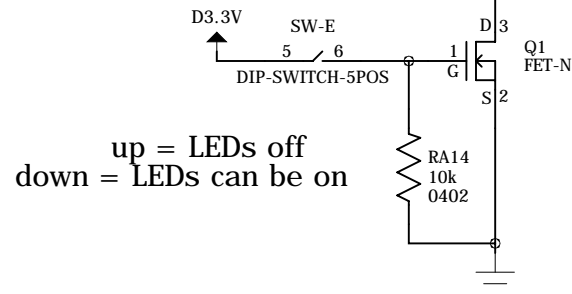
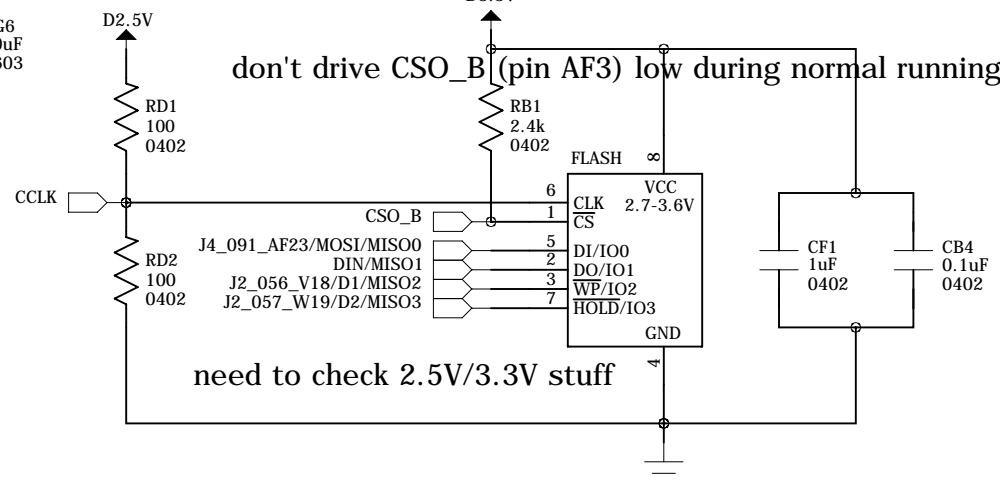
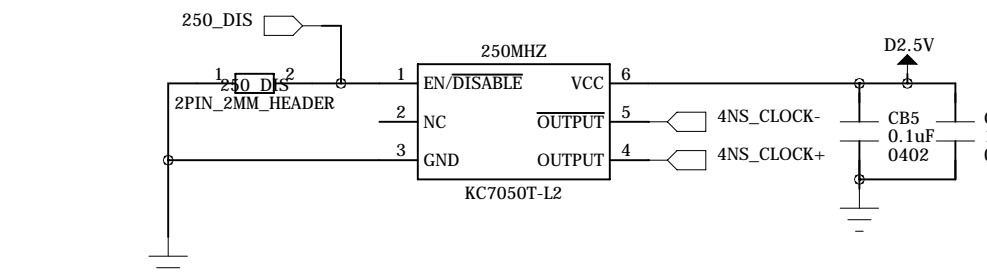
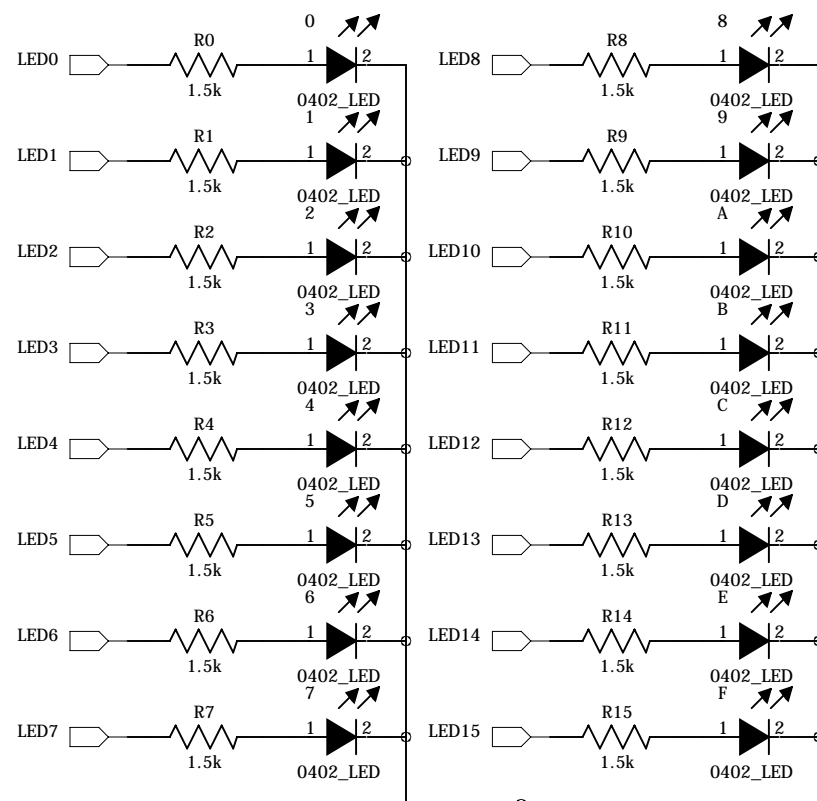
1



VCCAUX determines JTAG signal level
(ug380 page 58)
VCCAUX = 2.5V



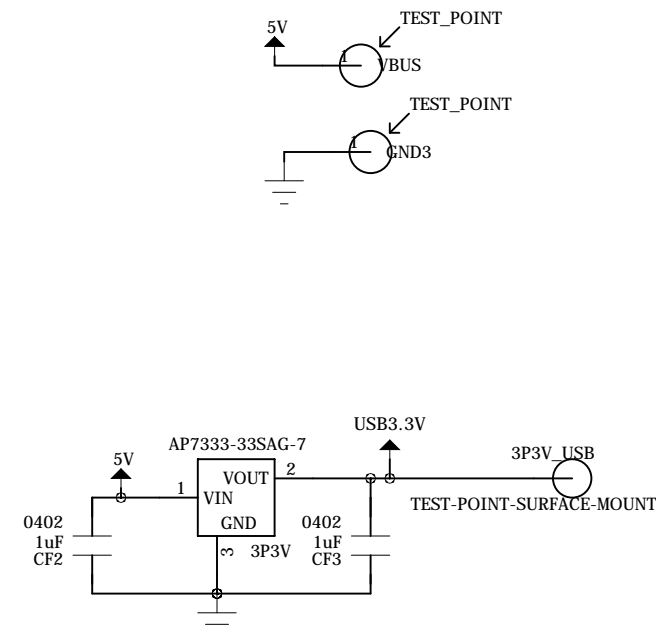
up = remote/LVDS
down = local/14 pin



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Instrumentation Development Lab

title: SCROD
revision: A3
IDLAB design #: IDL_13_037
circuit design: LJR, MZA, GSV, KAN
PCB design: LJR, MZA

sheet #: 6 of 7
sheet description: JTAG, CLOCK, LEDs, PROM
date last modified: 2014-02-12



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A3
IDLAB design #:	IDL_13_037
circuit design:	LJR, MZA, GSV, KAN
PCB design:	LJR, MZA
sheet #:	7 of 7
sheet description:	Cypress FX2LP USB
date last modified:	2014-02-12