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CSE 371
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HW5

Problem 1

a)

$$t_{pCQ} + t_{PD} + t_{setup} \leq t_{period}$$

$$70ps + 300ps + 60ps \leq t_{period}$$

$$430ps \leq t_{period}$$

$$\boxed{2.325581395 \text{ GHz} \leq f_{clk}}$$

b) $f_{clk} = 2GHz \rightarrow t_{period} = 500ps$

$$t_{pCQ} + t_{PD} + t_{setup} + t_{skew} \leq t_{period}$$

$$70ps + 300ps + 60ps + t_{skew} \leq 500ps$$

$$\boxed{t_{skew} \leq 70ps}$$

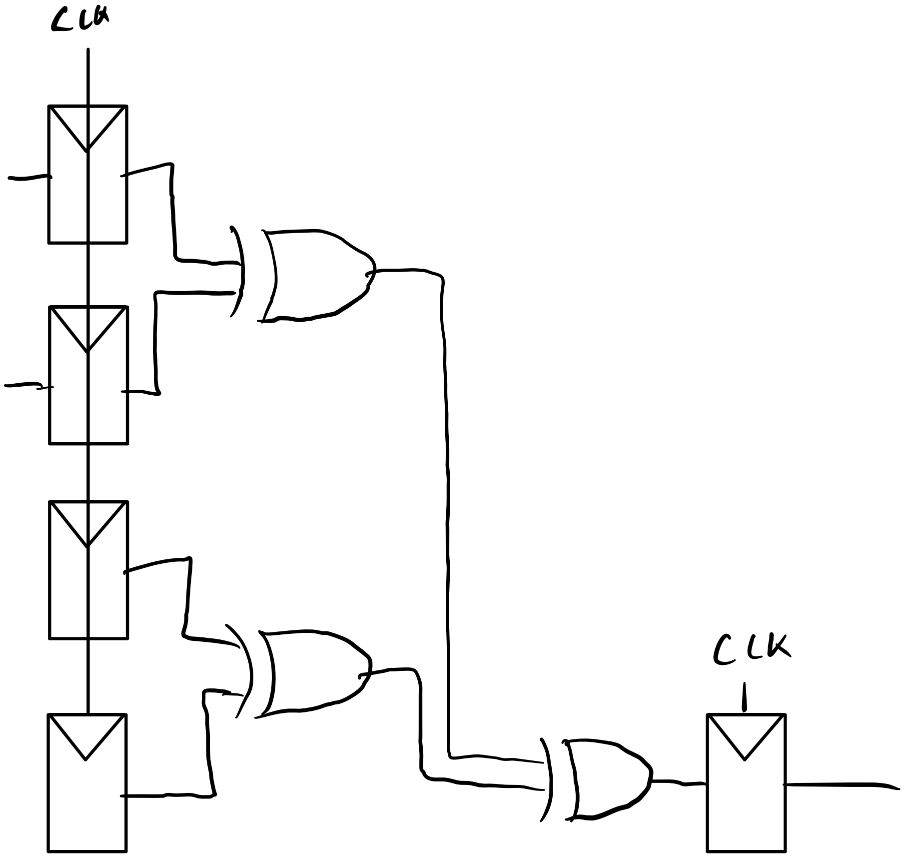
c)

$$t_{ccq} + t_{cd} \geq t_{skew} + t_{hold}$$

$$50ps + 165ps \geq t_{skew} + 20ps$$

$$\boxed{195ps \geq t_{skew}}$$

d)



$$t_{pcq} + t_{pd} + t_{setup} \leq t_{period}$$

$$70ps + 200ps + 60ps \leq t_{period}$$

$$330ps \leq t_{period}$$

Max freq. w/o skew → $\boxed{3.030303030\,GHz \leq f_{clk}}$

$$t_{CLQ} + t_{CD} \geq t_{skew} + t_{hold}$$

$$50ps + 110ps \geq t_{skew} + 20ps$$

Max clk skew before hold time violation

$$\boxed{140ps \geq t_{skew}}$$

Problem 2

$f_{clk} = 1\,GHz$ $\quad N = 0.5$

$\tau = 100ps$ $\quad T_0 = 110ps$

$t_{setup} = 70ps$

$$MTBF = 50 \text{ years} = \frac{1}{N} \cdot \frac{1}{P(\text{failure})}$$

$$1.5768 \cdot 10^9 = \frac{1}{0.5} \cdot \frac{1}{P(\text{failure})}$$

$$\boxed{P(\text{failure}) \approx 3.171 \cdot 10^{-10}}$$

$$P(\text{failure}) = \left(\frac{T_0}{T_c}\right) e^{-(T_c - t_{setup})/\tau}$$

$$3.171 \cdot 10^{-10} = \left(\frac{110}{T_c}\right) e^{-\left((T_c - 70)/100\right)}$$

$$T_c \approx 1968.71\,ps$$

$$1968.71_{ps} \cdot 1\,GHz = \boxed{1.96871 \text{ cycles}}$$

Problem 3

a) $P(\text{stuck after } t \text{ seconds}) = e^{-t/20}$

$P(\text{resolved after } t \text{ seconds}) = 1 - e^{-t/20}$

$0.99 = 1 - e^{-t/20}$

$\boxed{t \approx 92.1034 \text{ seconds}}$

b) $P(\text{stuck after } 180s) = e^{-180/20}$

$\boxed{\approx 0.0001234}$

Problem 4

Alyssa is right because even on the asynchronous reset for the first flip-flop, D2 will always be metastable for some amount of time, meaning the flip-flop will repeatedly get reset - decreasing the window where D can actually be sampled.

Problem 5

18) Mult0~921|resulta[2]

Since the setup timing requirements are not being met, we can slow down the frequency of the clock to meet the timing constraints.

19) No, the worst delay comes from Mult0~8|clk[0]

This makes sense because the min DAT is traced for hold slack while max DAT is traced for setup slack. Thus, it is likely that different paths were found for each analysis.

22) The fastest frequency is 59.67 MHz.

33)

a) Fast 110mV 0C Model

b) Increasing Voltage speed from slow → fast increases setup slack, so it must slow the speed of the circuit.

c) Increasing temperature from 0C → 85C increased setup slack for the "slow" models, but decreased for the "fast" models. From these results, the answer is inconclusive.

34)

a) Fast 110 mV 85C Model

b) Increasing Voltage speed from slow → fast increases hold slack, so it must slow the speed of the circuit.

c) Increasing temperature from 0C → 85C increased the hold slack, so it must slow the speed of the circuit.

Time Spent - 3 hours

Difficulty - Moderate