Lab 5

Sequential Logic

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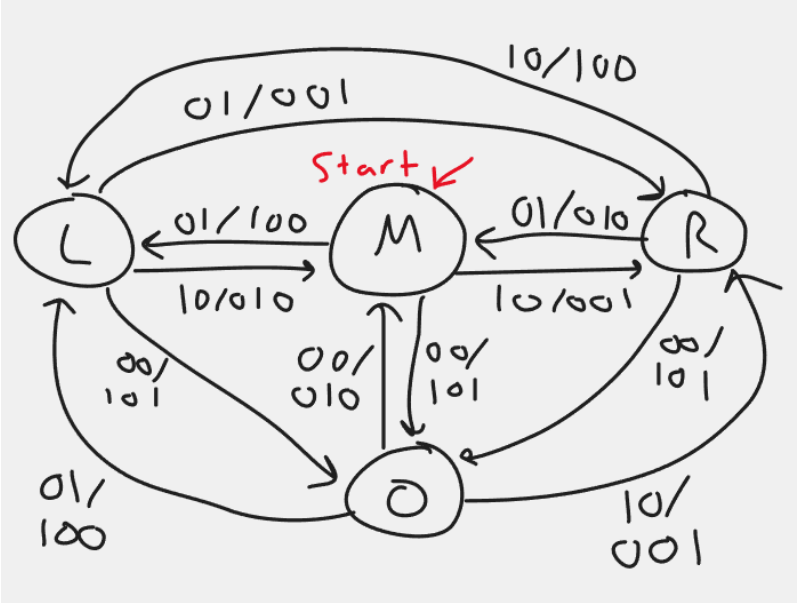
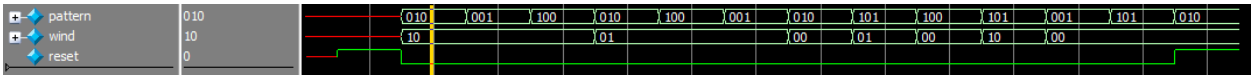
A drawing of your Finite State Machine.



A drawing of the Finite State Machine used for this lab. Transitions are shown as `XY/ABC` where `XY` gives the input to cause the transition, and `ABC` gives the output of the FSM.

A screenshot of the ModelSim simulations you will demonstrate in-person.

Runway Lights Circuit Simulation



This screenshot shows output for all of the possible state transitions in this circuit's FSM. The positive clock edge occurs at each of the horizontal gray lines, and the output signal, "pattern" for that sampled input occurs halfway between the clock's period.

A screenshot of the "Resource Utilization by Entity" page, showing your design's computed size.

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
1	⌄ |lab5	29 (0)	29 (0)	0	0	26	0	|lab5	lab5	work
1	|clock_divider:cdiv|	26 (26)	26 (26)	0	0	0	0	|lab5|clock_divider:cdiv	clock_divider	work
2	|seatac:indicator|	3 (3)	3 (3)	0	0	0	0	|lab5|seatac:indicator	seatac	work

Resource utilization for the Lab 5 top-level module. [clock_divider:cdiv] is the clock dividing module used by this design, and [seatac:indicator] is the instance of the runway lights circuit implementation.

Time Estimation

This lab took approximately 4 hours, in total, to complete.