Lab 7

Useful Components

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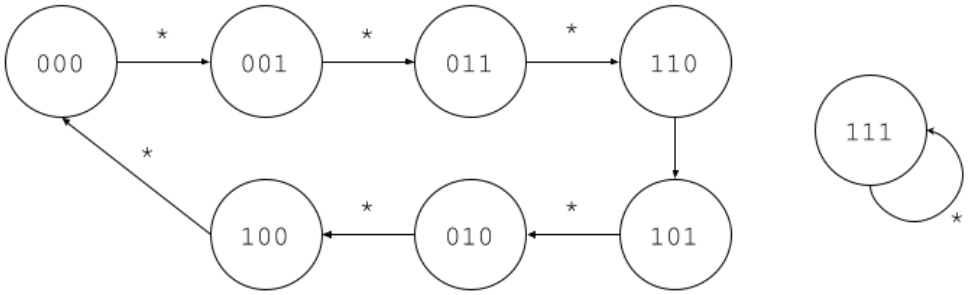
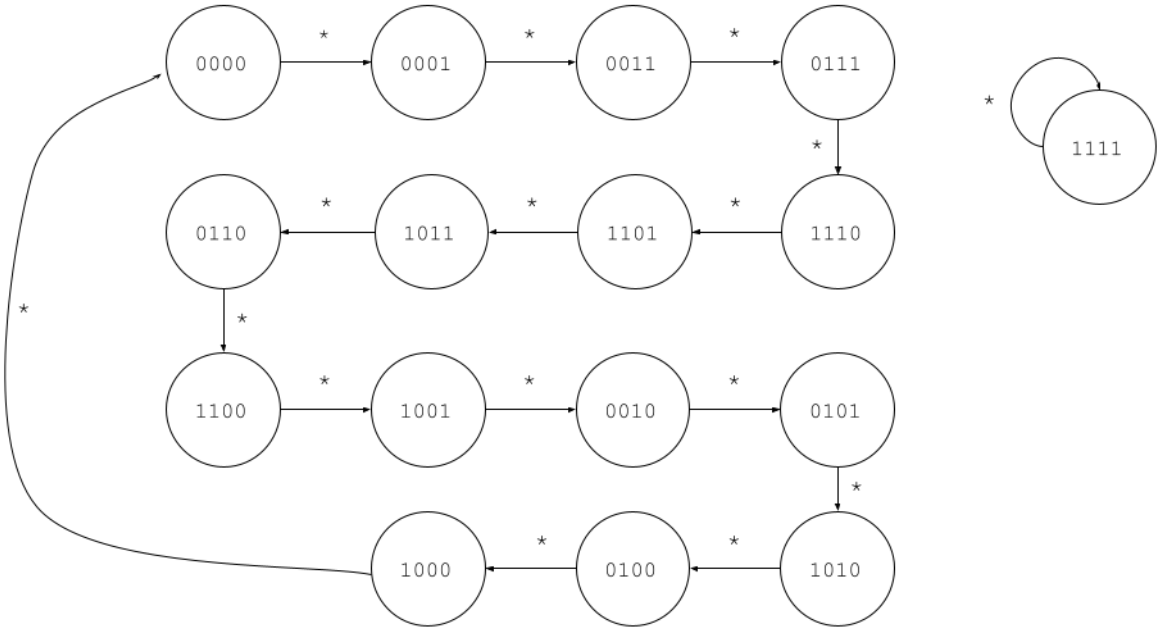
State diagrams derived from the 3-bit and 4-bit LFSRs.

3-bit LFSR State Diagram



The state diagram for the 3-bit LFSR, which uses the XNOR of the 2 most significant bits to produce the next least significant bit. Each state transition labeled with a "*" is followed on each clock edge. The starting state for this state machine is "000".

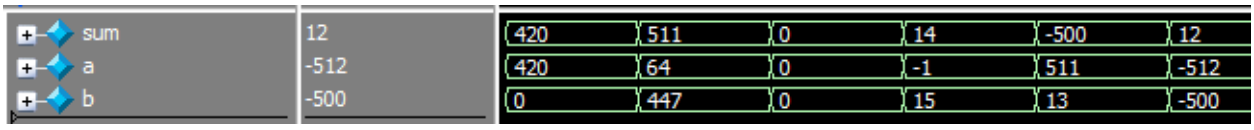
4-bit LFSR State Diagram



The state diagram for the 4-bit LFSR, which uses the XNOR of the 2 most significant bits to produce the next least significant bit. Each state transition labeled with a "*" is followed on each clock edge. The starting state for this state machine is "0000".

Simulation of your working 10-bit adder that covers the 6 situations described.

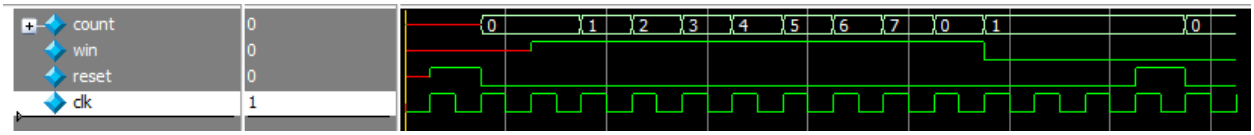
10-bit Adder Simulation



The simulation for the 10-bit adder, demonstrating (in order): (1) an addition where one input is 0, (2) an addition whose result is 511, (3) an addition whose result is 0, (4) an example of unsigned overflow (-1 [signed] is equivalent to 1023 [unsigned]), (5) an example of positive signed overflow, and (6) an example of negative signed overflow.

Simulation of your working 3-bit counter.

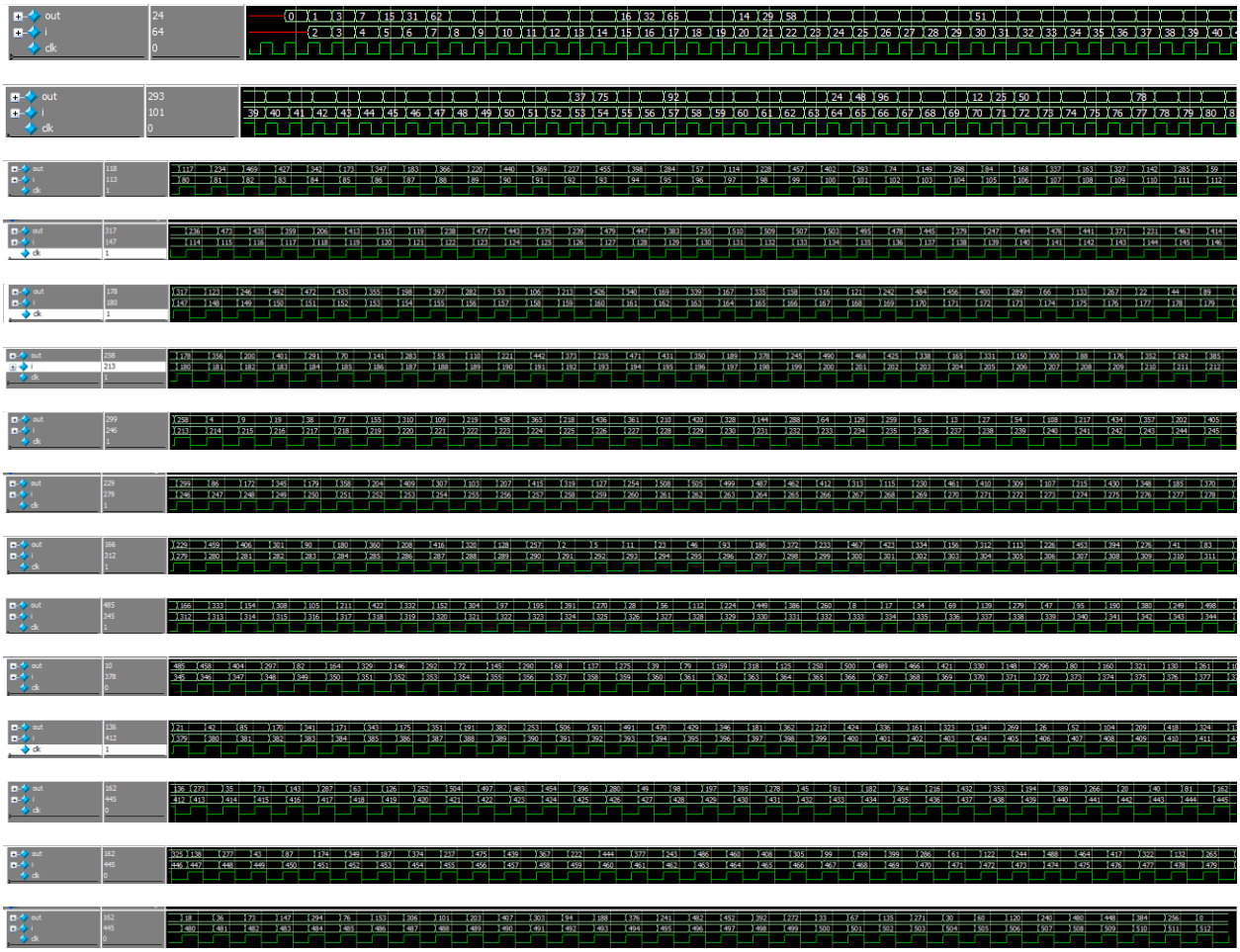
3-bit Counter Simulation



The simulation for the 3-bit counter showing that every clock cycle where a “win” input is received, the count increases by 1, and that the count stays the same when a “win” input is not received.

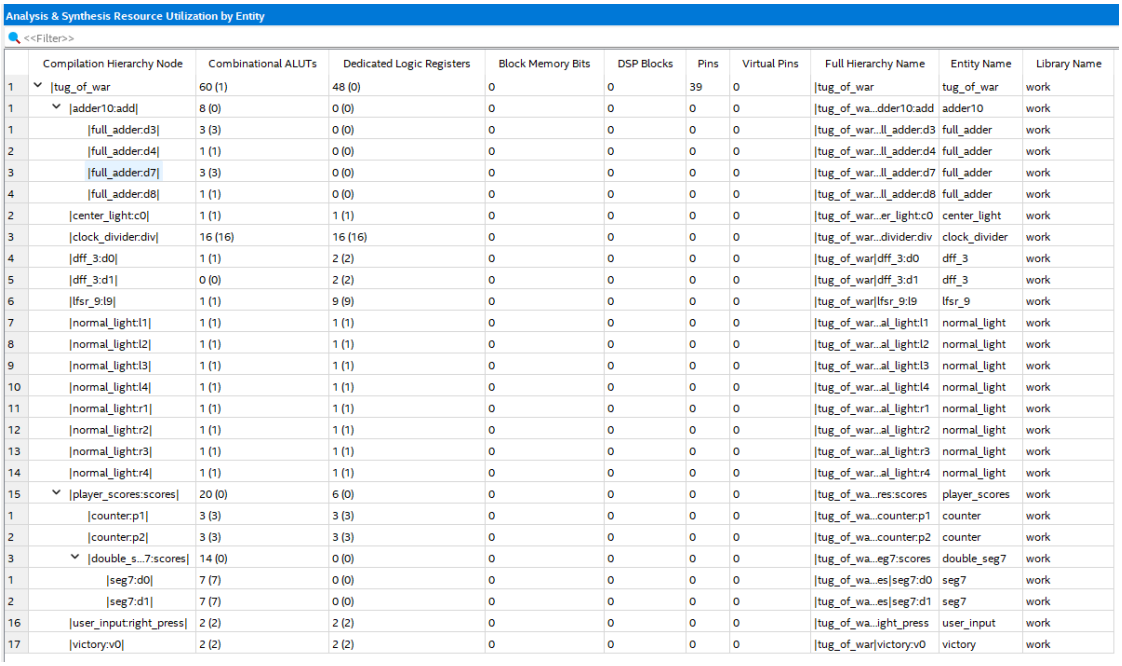
Simulation of your working 9-bit LFSR with the state cycle length indicated.

9-bit LFSR Simulation



The simulation for the 9-bit LFSR. The “out” signal shows the output of the LFSR, and the “i” counter shows the number of states visited by the LFSR. The initial state of the LFSR is 9’b0, and the simulation is set to stop once it loops back to the initial state. Notice that in the bottom screenshot, the simulation reaches 511 unique states before coming back to the initial 9’b0 state and stopping.

A screenshot of the "Resource Utilization by Entity" page, showing your design's computed size.



Analysis & Synthesis Resource Utilization by Entity

<<Filter>>

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
1	|tug_of_war	60 (1)	48 (0)	0	0	39	0	|tug_of_war	tug_of_war	work
1	|adder10:add|	8 (0)	0 (0)	0	0	0	0	|tug_of_wa...dder10:add	adder10	work
1	|full_adder:d3|	3 (3)	0 (0)	0	0	0	0	|tug_of_war...ll_adder:d3	full_adder	work
2	|full_adder:d4|	1 (1)	0 (0)	0	0	0	0	|tug_of_war...ll_adder:d4	full_adder	work
3	|full_adder:d7|	3 (3)	0 (0)	0	0	0	0	|tug_of_war...ll_adder:d7	full_adder	work
4	|full_adder:d8|	1 (1)	0 (0)	0	0	0	0	|tug_of_war...ll_adder:d8	full_adder	work
2	|center_light:c0|	1 (1)	1 (1)	0	0	0	0	|tug_of_war...er_light:c0	center_light	work
3	|clock_divider:div|	16 (16)	16 (16)	0	0	0	0	|tug_of_war...divider:div	clock_divider	work
4	|dff_3:d0|	1 (1)	2 (2)	0	0	0	0	|tug_of_war|dff_3:d0	dff_3	work
5	|dff_3:d1|	0 (0)	2 (2)	0	0	0	0	|tug_of_war|dff_3:d1	dff_3	work
6	|lfsr_9:l9|	1 (1)	9 (9)	0	0	0	0	|tug_of_war|lfsr_9:l9	lfsr_9	work
7	|normal_light:l1|	1 (1)	1 (1)	0	0	0	0	|tug_of_war...al_light:l1	normal_light	work
8	|normal_light:l2|	1 (1)	1 (1)	0	0	0	0	|tug_of_war...al_light:l2	normal_light	work
9	|normal_light:l3|	1 (1)	1 (1)	0	0	0	0	|tug_of_war...al_light:l3	normal_light	work
10	|normal_light:l4|	1 (1)	1 (1)	0	0	0	0	|tug_of_war...al_light:l4	normal_light	work
11	|normal_light:r1|	1 (1)	1 (1)	0	0	0	0	|tug_of_war...al_light:r1	normal_light	work
12	|normal_light:r2|	1 (1)	1 (1)	0	0	0	0	|tug_of_war...al_light:r2	normal_light	work
13	|normal_light:r3|	1 (1)	1 (1)	0	0	0	0	|tug_of_war...al_light:r3	normal_light	work
14	|normal_light:r4|	1 (1)	1 (1)	0	0	0	0	|tug_of_war...al_light:r4	normal_light	work
15	|player_scores:scores|	20 (0)	6 (0)	0	0	0	0	|tug_of_wa...res:scores	player_scores	work
1	|counter:p1|	3 (3)	3 (3)	0	0	0	0	|tug_of_wa...counter:p1	counter	work
2	|counter:p2|	3 (3)	3 (3)	0	0	0	0	|tug_of_wa...counter:p2	counter	work
3	|double_s...7:scores|	14 (0)	0 (0)	0	0	0	0	|tug_of_wa...eg7:scores	double_seg7	work
1	|seg7:d0|	7 (7)	0 (0)	0	0	0	0	|tug_of_wa...es|seg7:d0	seg7	work
2	|seg7:d1|	7 (7)	0 (0)	0	0	0	0	|tug_of_wa...es|seg7:d1	seg7	work
16	|user_input:right_press|	2 (2)	2 (2)	0	0	0	0	|tug_of_wa...ight_press	user_input	work
17	|victory:v0|	2 (2)	2 (2)	0	0	0	0	|tug_of_war|victory:v0	victory	work

Resource utilization for the `tug_of_war` top-level module.

Time Estimation

This lab took approximately 7 hours, in total, to complete.