香港中文大學
The Chinese University of Hong Kong

CENG2400 Embedded System Design
Lecture 07: Analog Interfacing

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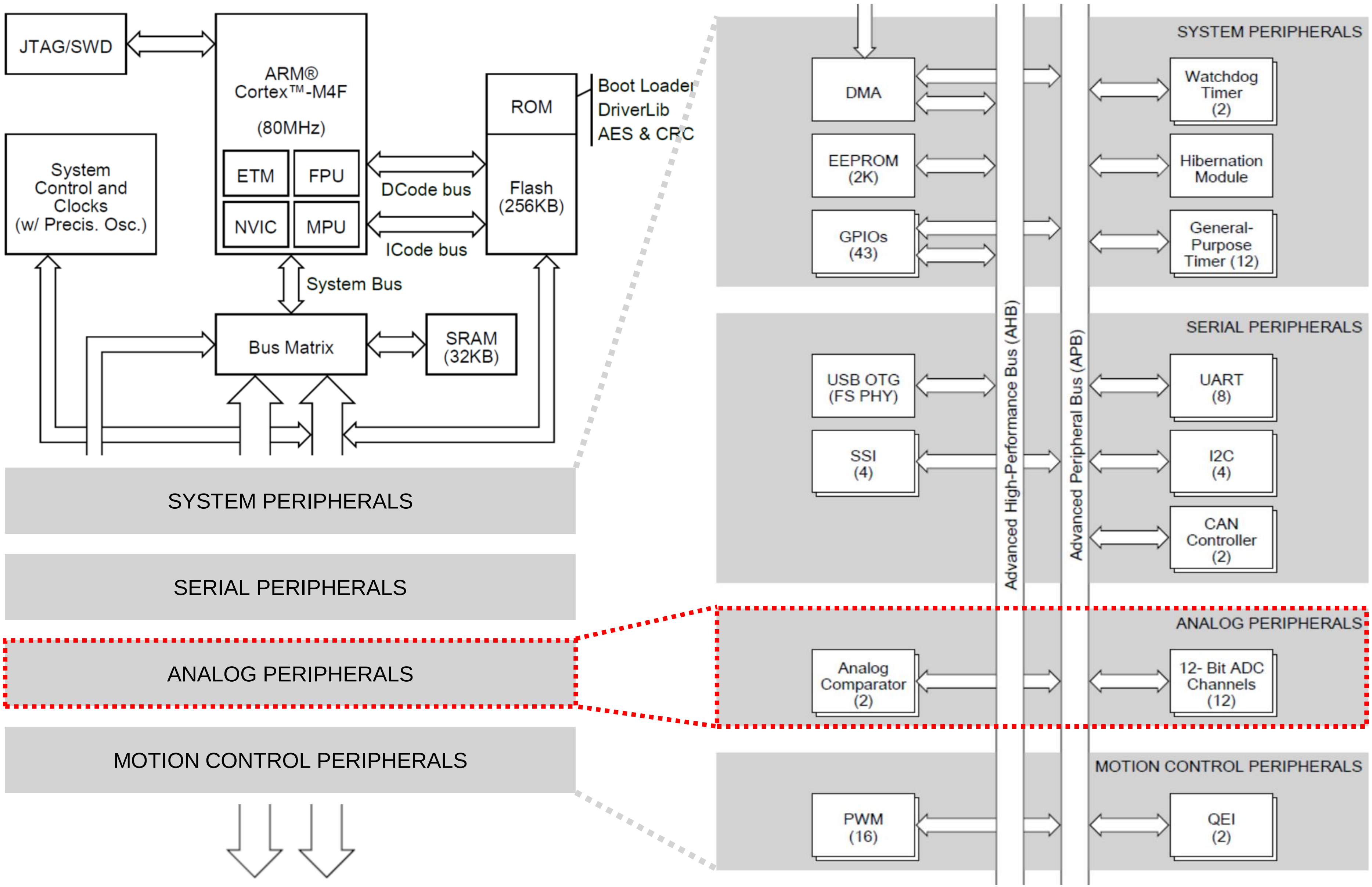
Thanks to Prof. Q. Xu and Drs. K. H. Wong, Philip Leong, Y.S. Moon, O. Mencer, N. Dulay, P. Cheung for some of the slides used in this course!

Recall: Tiva™ TM4C123GH6PM (MCU)

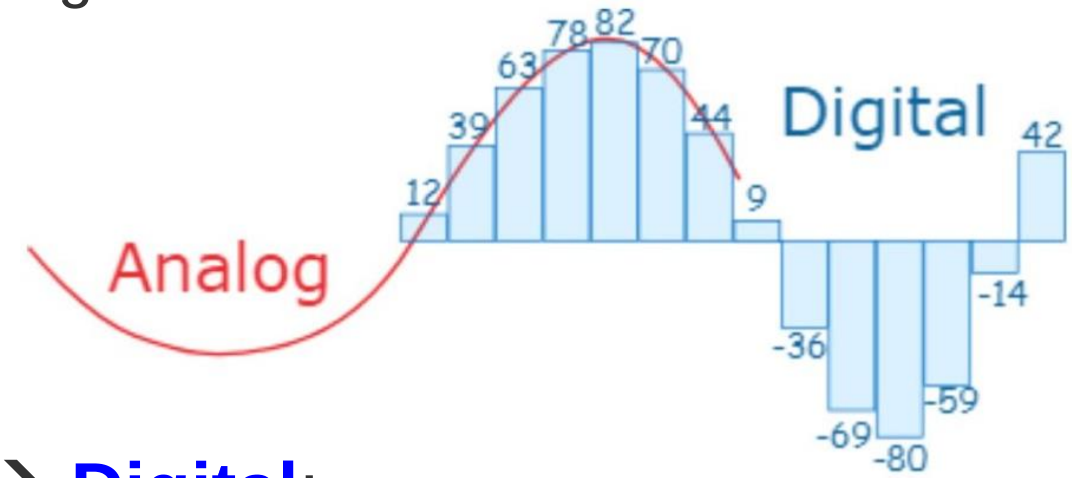


Outline

- **Basics**
  - Quantization
  - Sampling
- **Digital → Analog**
  - Digital-to-Analog Conversion (DAC)
- **Analog → Digital**
  - Analog Comparator
  - Analog-to-Digital Conversion (ADC)
- **Preview: Lab06**

Why Analog ←→ Digital?

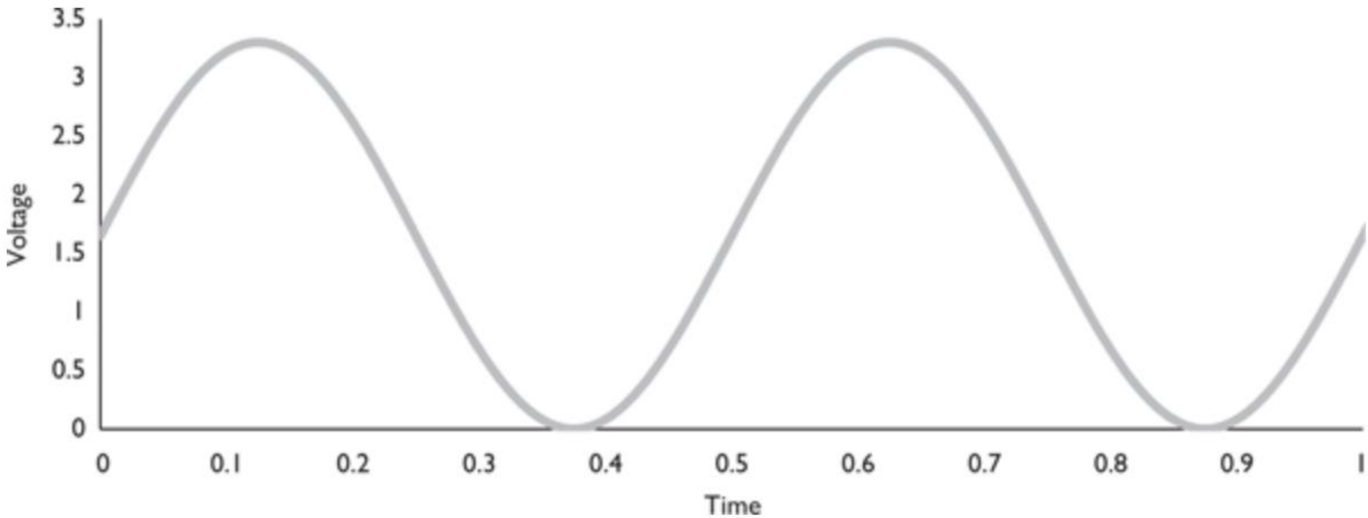
- **Digital → Analog**:
  - To drive headphones or speakers, the MCU must convert the digital values representing the sound signal into analog voltage signals.



- **Analog → Digital**:
  - Embedded systems often need to measure values of physical parameters (e.g., temperature, light intensity, etc.)
  - These parameters are usually continuous (analog) and not in a discrete (digital) form which computers can process.

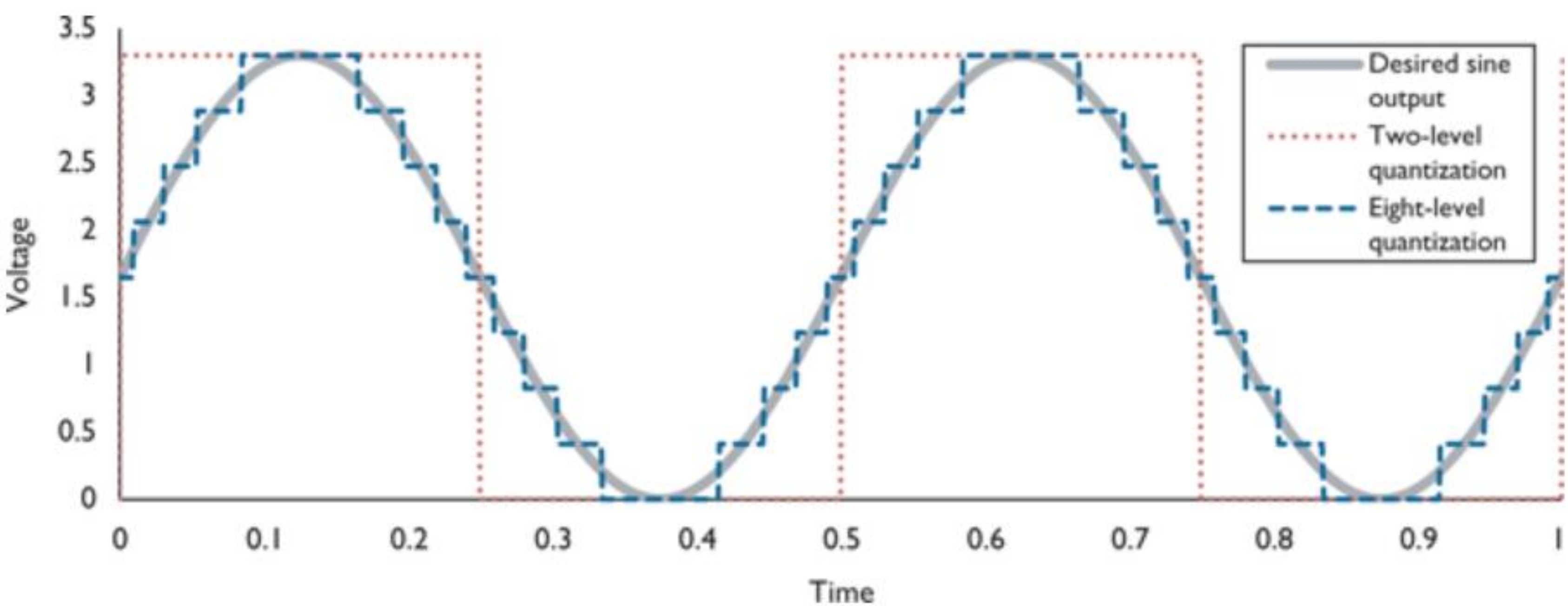
Concepts

- Interfacing with analog involves two major steps:
  ① **Quantization:** There are a limited number of voltages to represent an analog value.
  ② **Sampling:** The MCU operates on an input/output only at a limited rate.
- Example: How to represent a sine waveform digitally?
  – Sine wave has analog value varying continuously over time.



Quantization (1/2)

- **Quantization:** Process of selecting a discrete digital value to represent an analog value.
  - Each quantized output value represents a range of possible analog input values.
  - The number of discrete values available for use defines the resolution of the quantization.



Quantization (2/2)

- An example of **two-bit quantization**:

Input Voltage	Quantized Value: Decimal	Quantized Value: Binary	
	3	11	Out of range
V_{+ref} = 1 V			
	3	11	
0.75 V			
	2	10	
0.5 V			
	1	01	
0.25 V			
	0	00	
V_{-ref} = 0 V			
	0	00	Out of range

Transfer Function

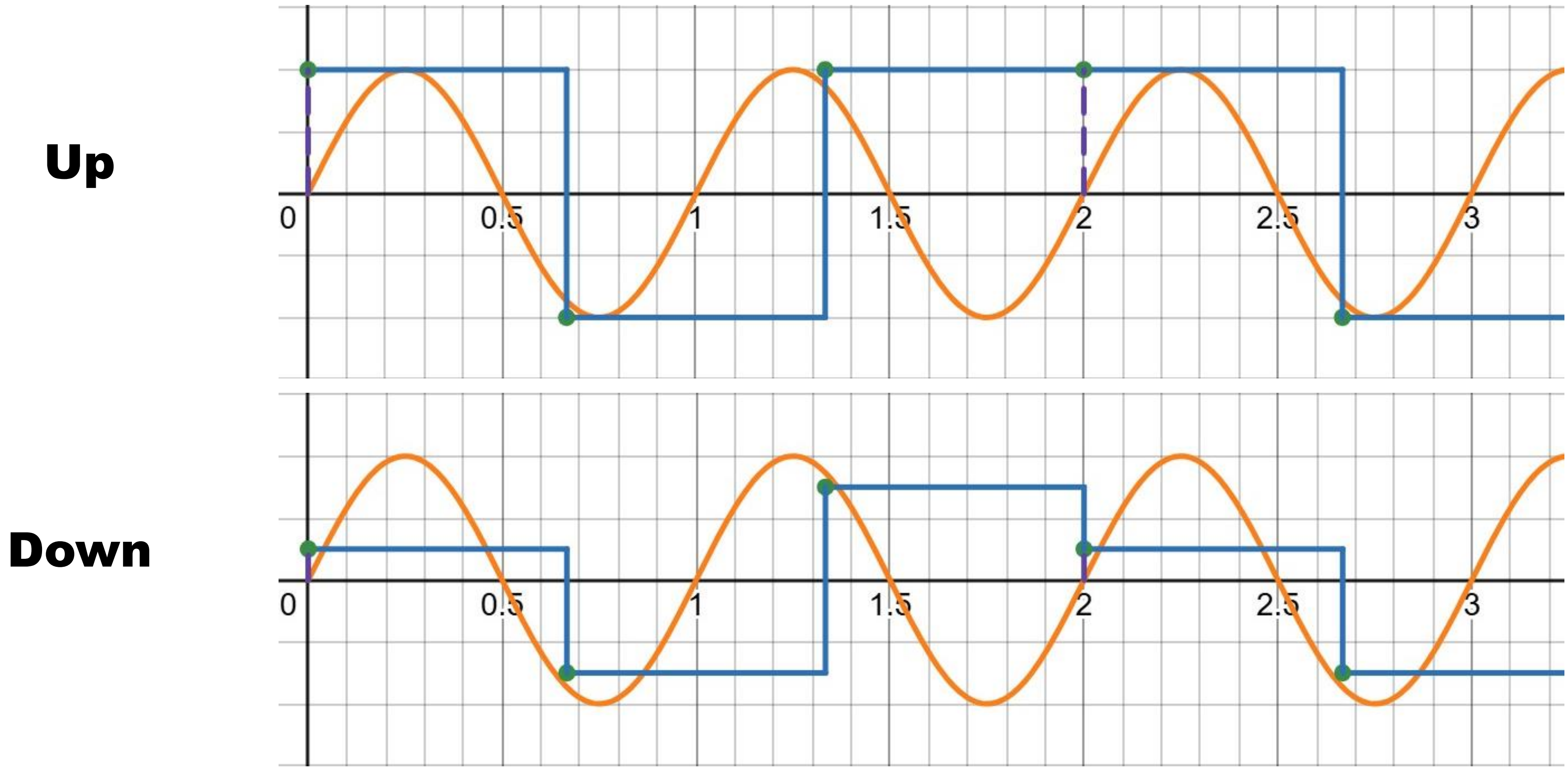
$$n = round\left(\frac{V_{in} - V_{-ref}}{V_{+ref} - V_{-ref}} \times 2^{B}\right)$$

- V_{in}: the input (analog) voltage
- B: the number of bits used to hold the output value
- n: the output (digital) value

  – V_{+ref} and V_{-ref} define the boundaries of the conversion.
  – A transfer function defines the quantization mathematically.

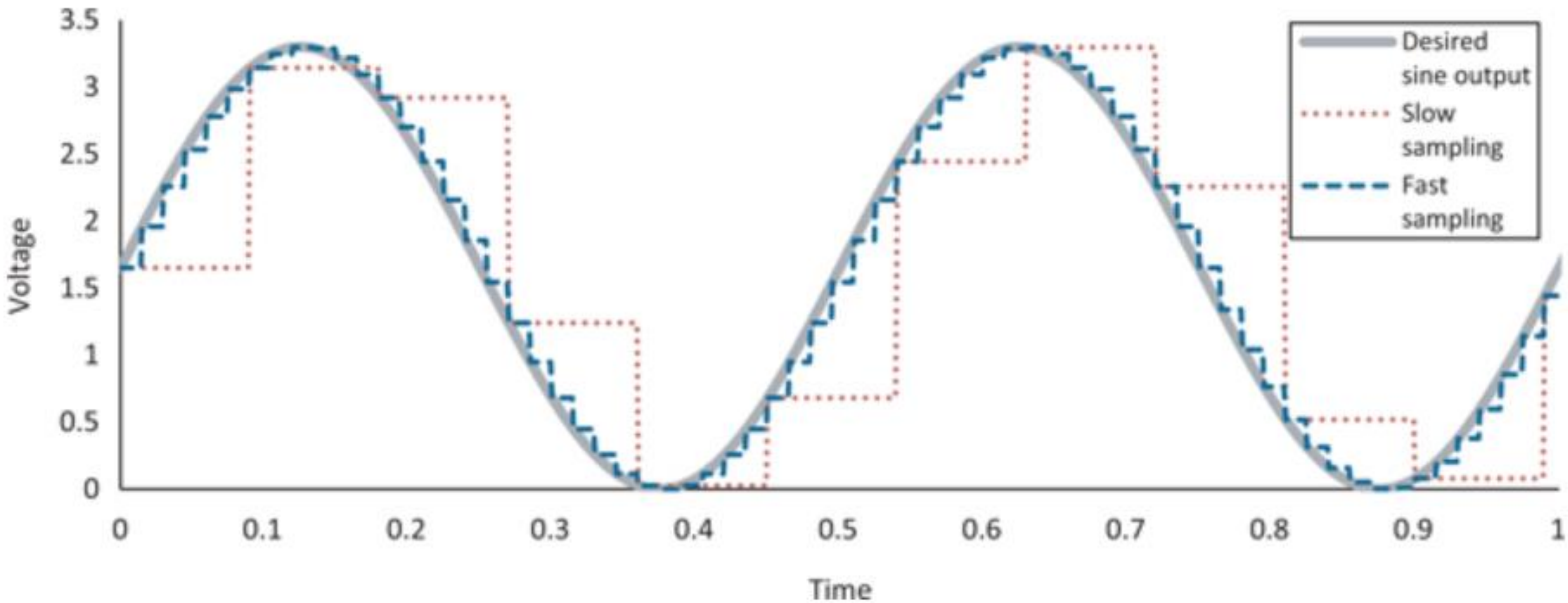
Class Exercise 7.1

- Suppose the period is 1 second and the sample rate is at 1.5 Hz. What would the waveform look like with two-level and eight-level quantization, respectively?



Sampling

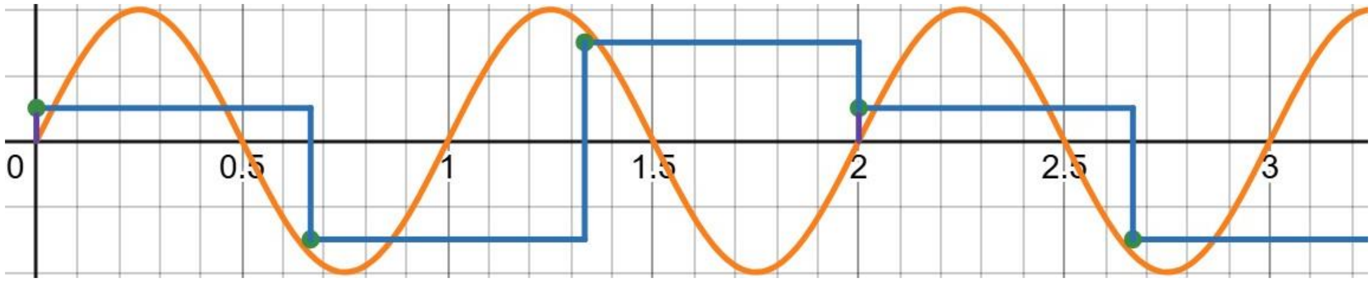
- **Sampling:** Process of converting a continuous-time signal to a series of discrete-time samples.
  - Any information between the samples is lost.
    - Low frequency (slow sampling) results in a poor approximation.
  - Each sample may be an analog value (one of an infinite number of possible values) until it is **quantized**.



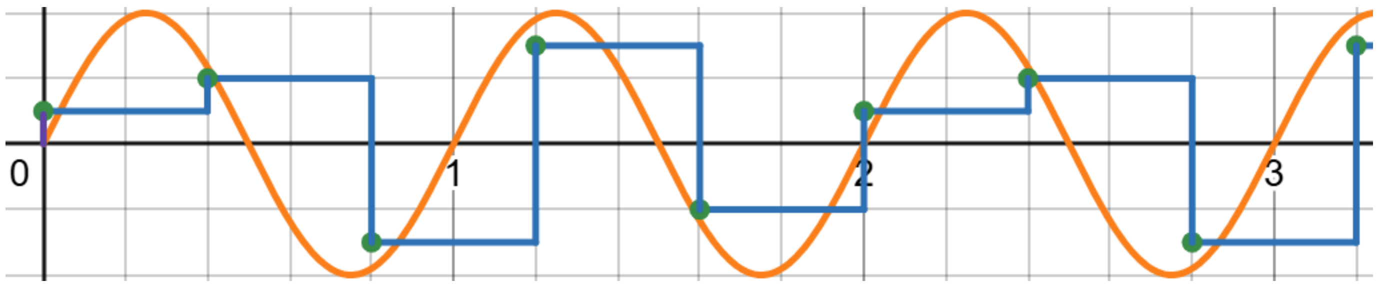
Class Exercise 7.2

- Suppose the period is 1 second and consider the eight-level quantization. What would the waveform look like if the sample rate is at 5 Hz?

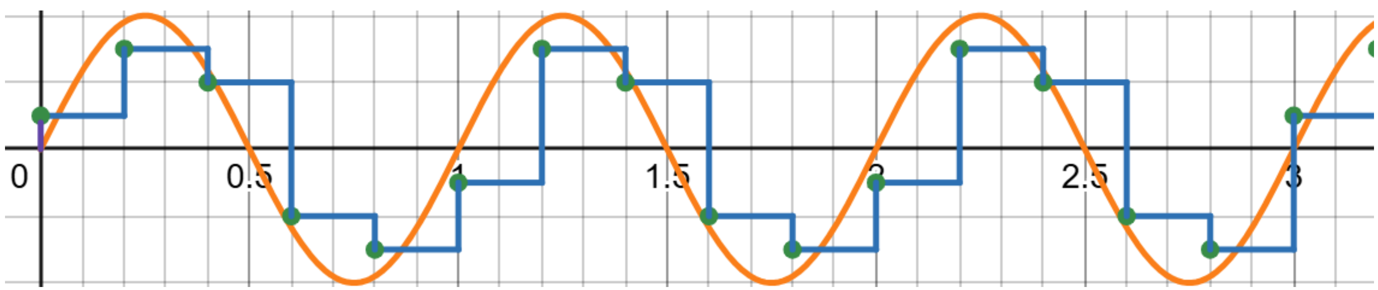
A)



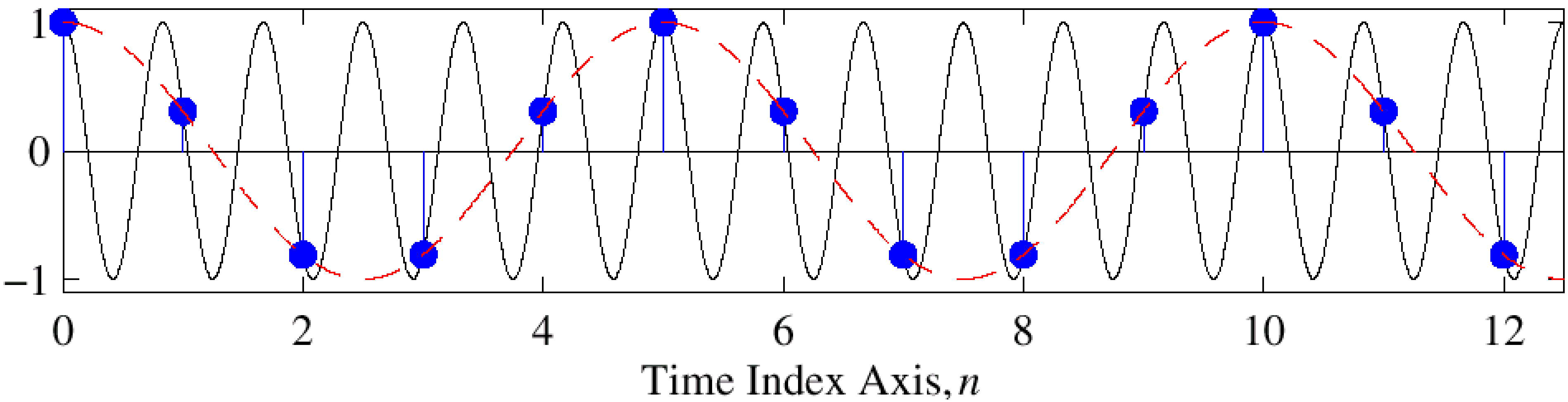
B)



C)



How often to sample?

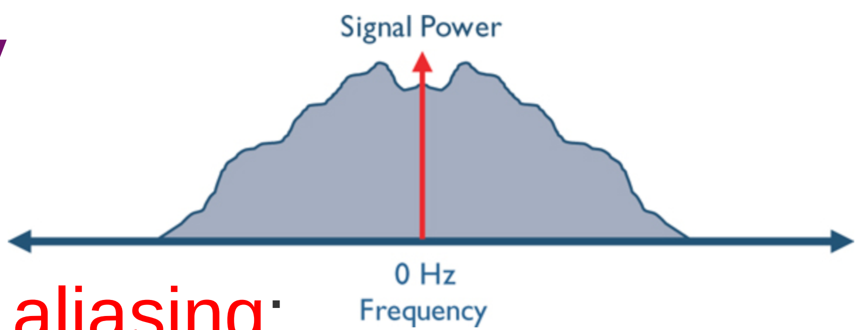


- Two different cosine signals can be drawn through the same samples:

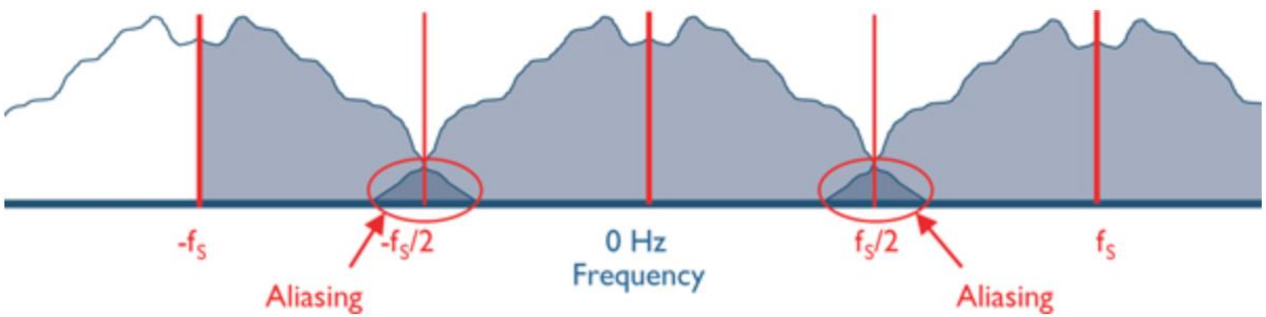
$$\cos(0.4\pi n) = \cos(2\pi n + 0.4\pi n) = \cos(2.4\pi n)$$

Where does distortion come from?

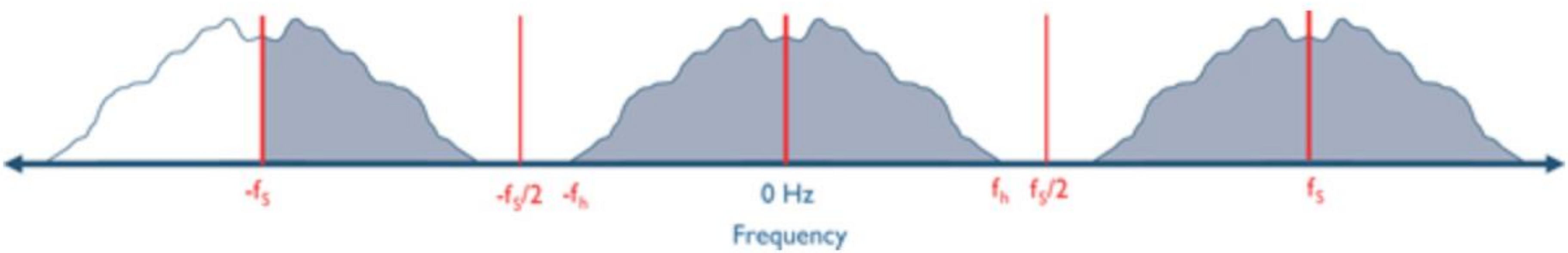
- Let’s consider the frequency spectrum of a signal:



- Sampling too slowly causes aliasing:



- Sampling at least twice the highest frequency component eliminates aliasing (**Nyquist Criterion**).



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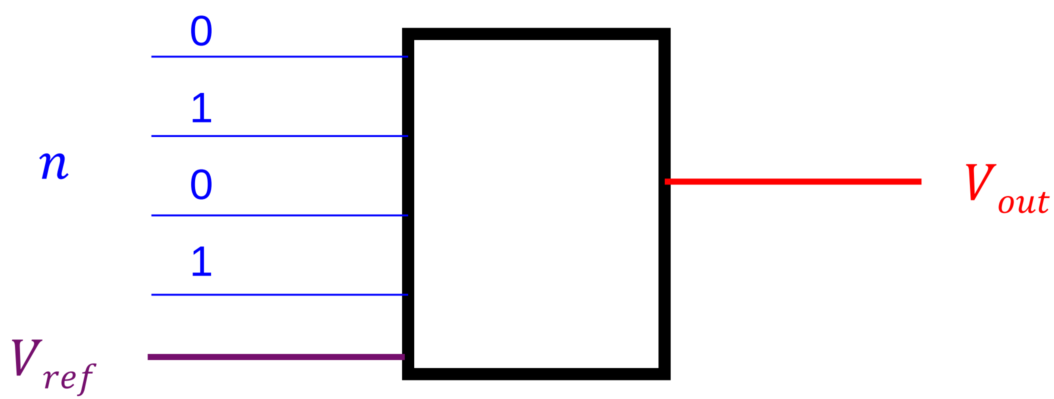
- **Preview: Lab06**

Digital-to-Analog Conversion (DAC)

- A **digital-to-analog converter (DAC)** generates an analog output signal based on the digital input value.
  - *Note: The output signal may be a voltage or a current.*

D/A Converter



Transfer Function

$$V_{out} = V_{ref} \times \frac{n}{2^B} \quad \textbf{or} \quad V_{ref} \times \frac{n+1}{2^B}$$

- n: the input (digital) code
- V_{ref}: the reference (analog) voltage
- V_{out}: the output (analog) voltage
- B: the number of bits of resolution

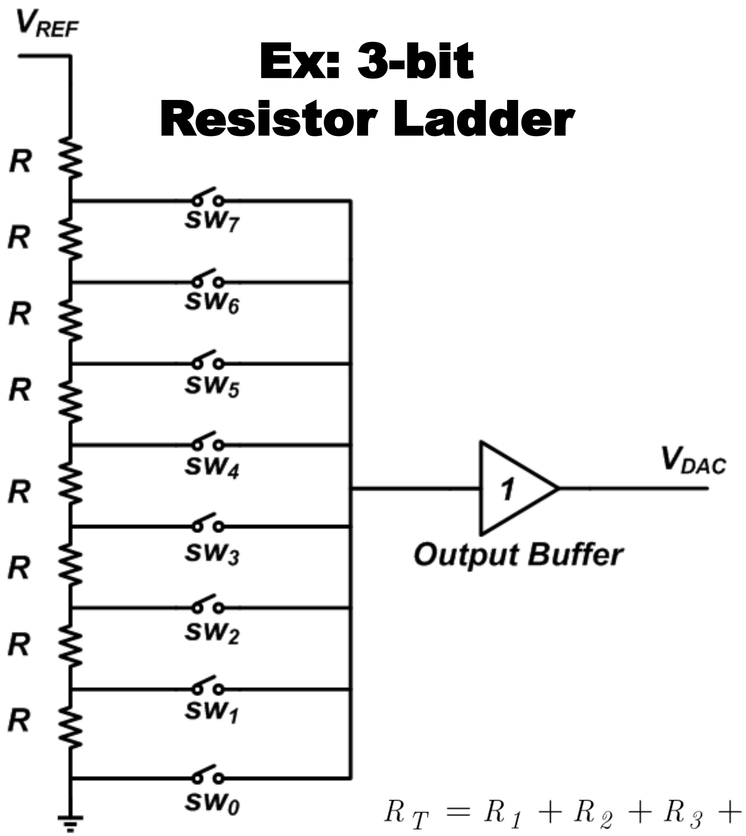
Class Exercise 7.3

- Determine the input code of a 12-bit DAC needed to generate an output voltage of 3.16 V if the reference voltage is 3.3 V.

DAC Architectures

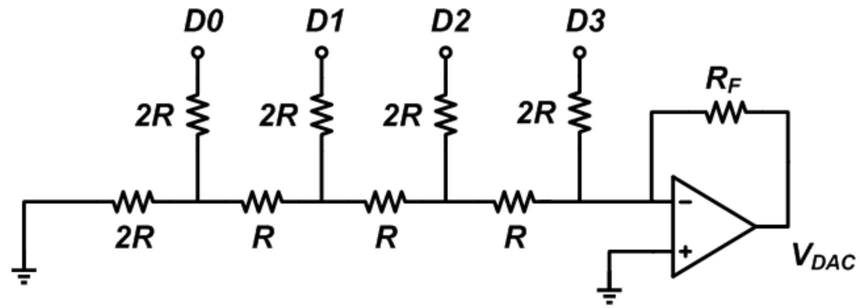
- Two common DAC architectures:
  - **Resistor Ladder**: uses 2^N resistors of equal value connected in series.
  - **R-2R Resistor Ladder**: uses ~N resistors of one value (R) and ~N resistors of twice that value (2R).

Ex: 3-bit Resistor Ladder



$$R_T = R_1 + R_2 + R_3 + etc...$$

Ex: 4-bit R-2R Resistor Ladder



$$R_T = \frac{1}{(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + etc...)}$$

https://www.youtube.com/watch?v=bXUfDLF4MVc

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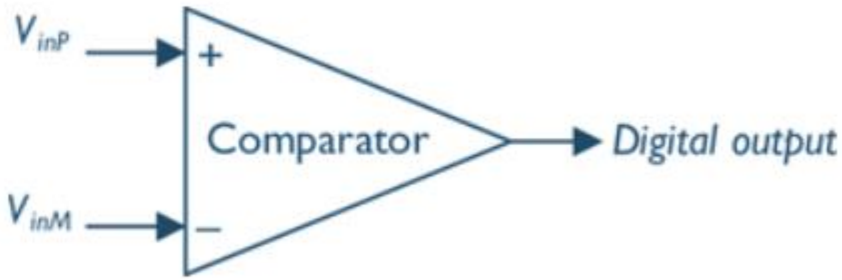
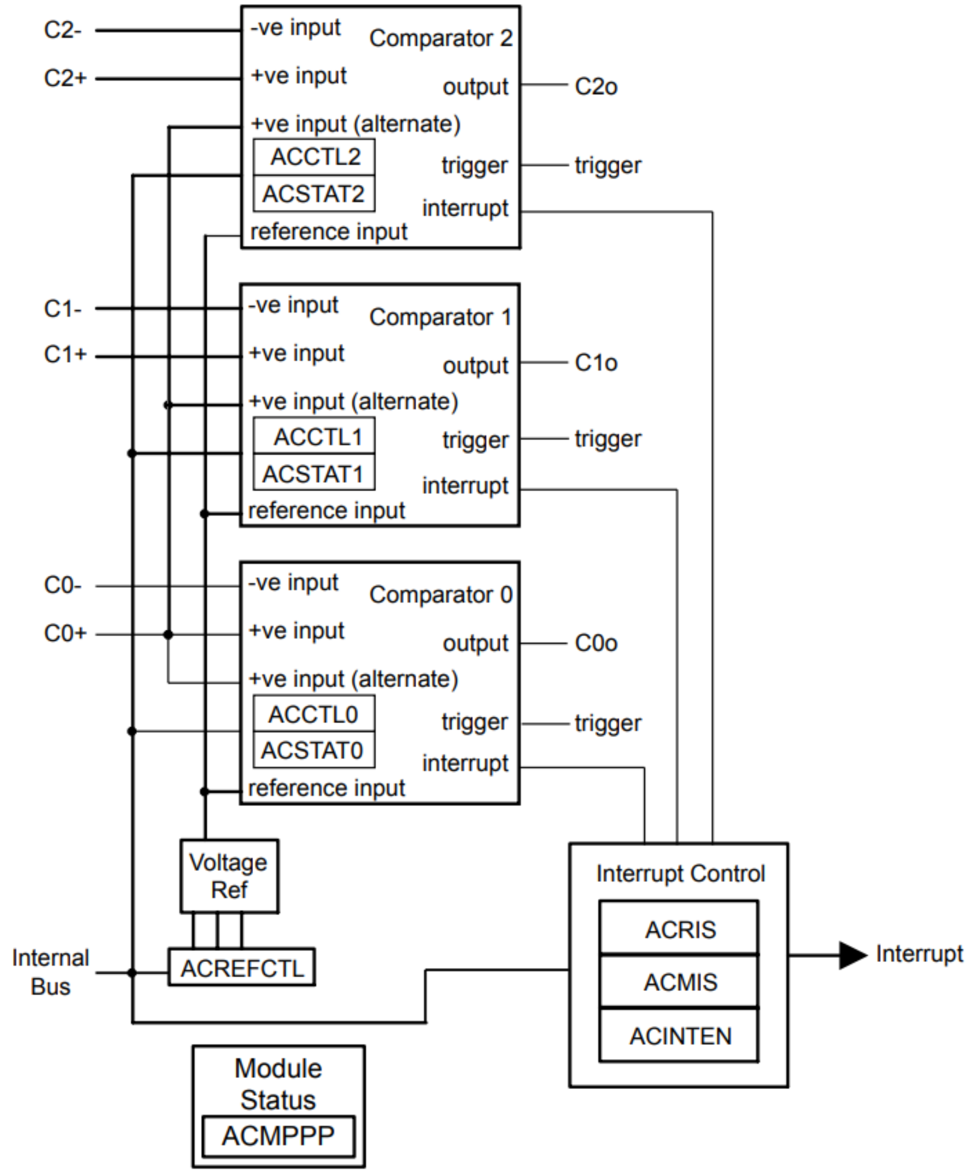
Analog Comparator

- An **analog comparator** is a circuit that compares two analog voltages and indicates which is greater.
  - This can be used to determine if a voltage is above or below a given level.



Analog Comparator on Tiva

- Tiva provides two independent integrated analog comparators.
  - Compare external to external pin inputs;
  - Compare external pin input to internal prog. voltage reference;
  - Compare a test voltage against the following:
    - An individual external reference voltage;
    - A shared single external reference voltage;
    - A shared internal reference voltage.



Analog Comparator Module

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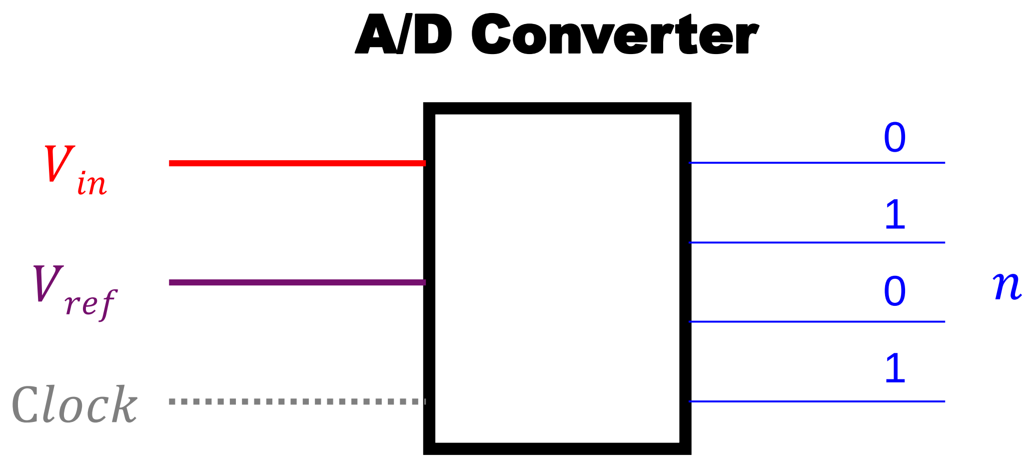
Analog-to-Digital Conversion (ADC)

- An **analog-to-digital converter (ADC)** quantizes an analog input voltage to create a digital output code.
  - It is similar to an analog comparator but provides more quantization levels (i.e., higher resolution).



Transfer Function

$$n = round\left(\frac{V_{in} - V_{-ref}}{V_{+ref} - V_{-ref}} \times 2^B\right)$$

- V_{in}: the input (analog) voltage
- V_{ref}: the reference (analog) voltage
- B: the number of bits of resolution
- n: the output (digital) value

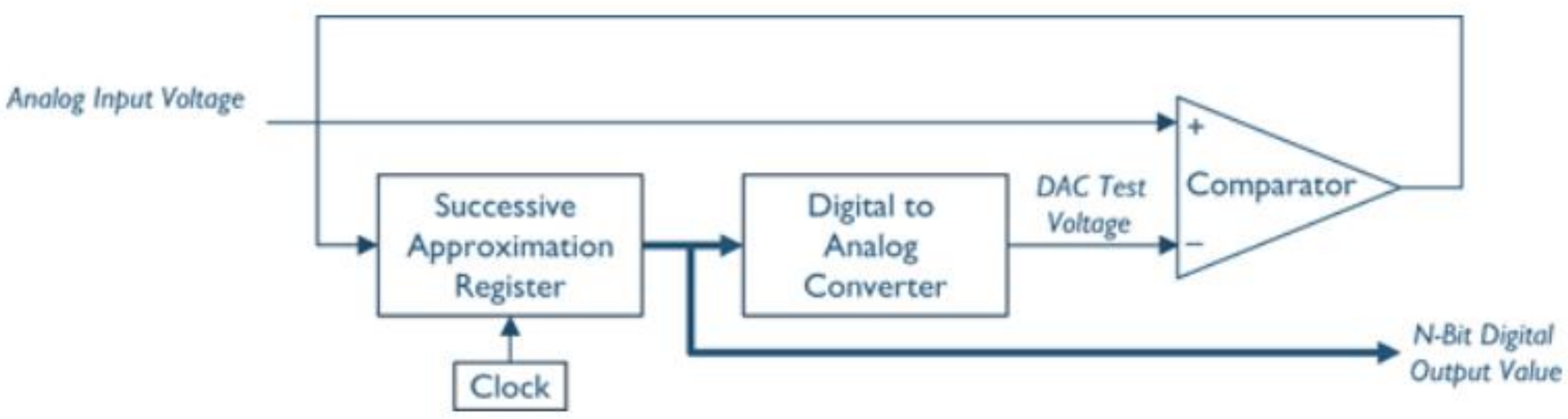
Class Exercise 7.4

- Consider a 16-bit ADC with an unknown reference voltage operating in single-ended mode (with common ground).
- What is the reference voltage if sampling the 1.0 V band gap reference results in a code of 16,384?

ADC Architectures (1/2)

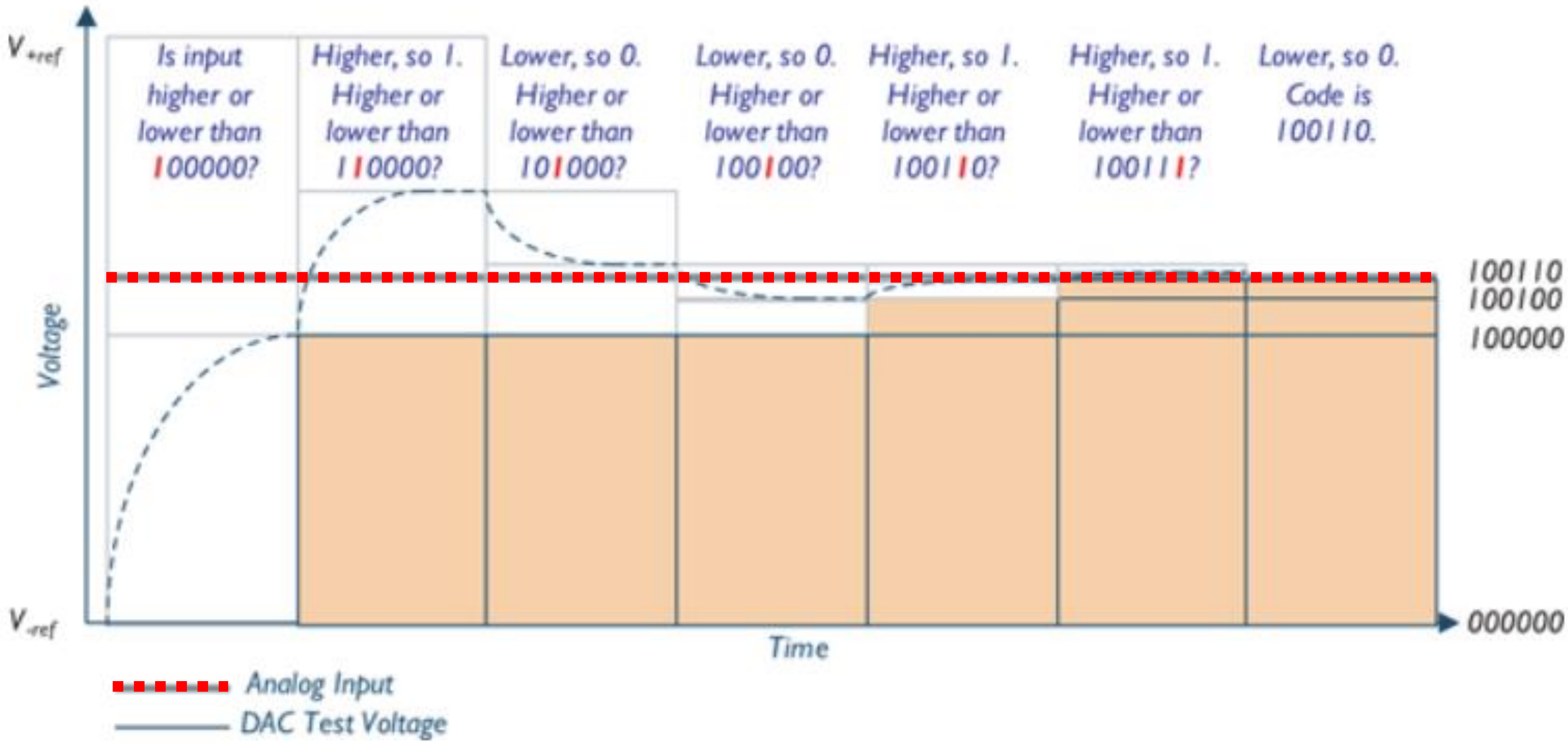
- **Flash Architecture:** operates 2^B analog comparators in parallel, each with a different reference voltage.
  - This is called a flash arch. because it is extremely fast.

- **Successive Approximation Architecture**: uses a single comparator to make a series of comparisons, changing its reference voltage for each.



ADC Architectures (2/2)

- **Successive Approximation Architecture** (Cont'd)
  - It performs a binary search to quantize the input.



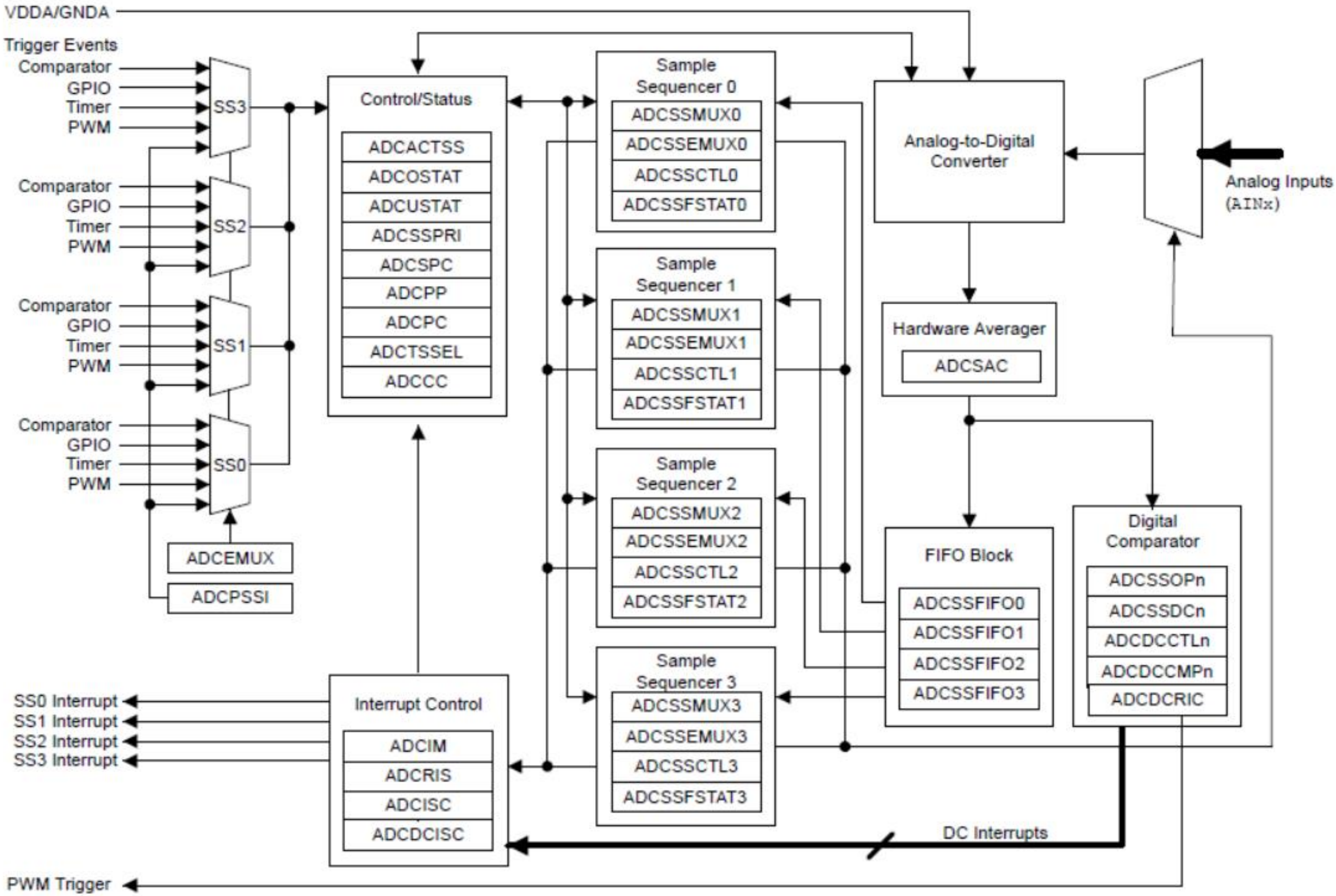
Inputs

- **Differential**
  - Use two channels, and compute difference between them
  - Very good noise immunity
- **Multiplexing**
  - Typically share a single ADC among multiple inputs
  - Need to select an input, allow time to settle before sampling
- **Signal Conditioning**
  - Amplify and filter input signal
  - Protect against out-of-range inputs with clamping diodes

Triggering

- The **trigger** is a signal that tells the ADC to start sampling and converting an input.
- An ADC will typically include two types of triggers:
  - **Software Trigger:** requires the software to write a value to a specific ADC control register to start the conversion.
  - **Hardware Trigger:** requires a hardware signal to be asserted by a circuit or peripheral (e.g., timer).
- The ADC performs sampling and conversion and then indicates that the conversion has completed.
  - This is done by setting a flag in an ADC status register, and possibly also signaling an interrupt request.
  - The result is available in digital in an ADC result register.

ADC Module on Tiva



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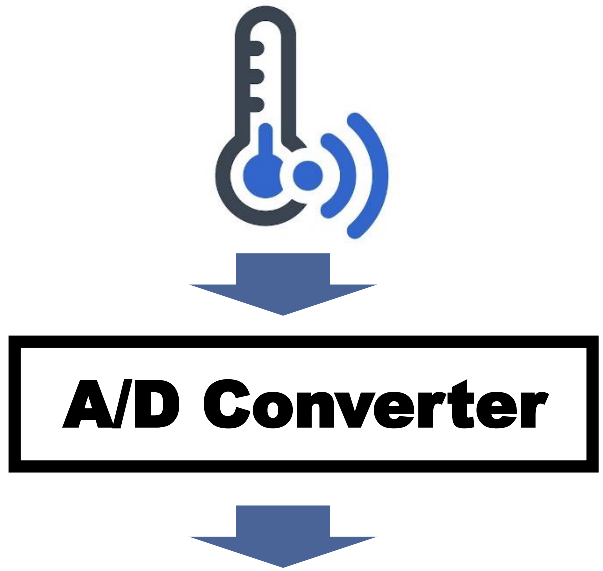
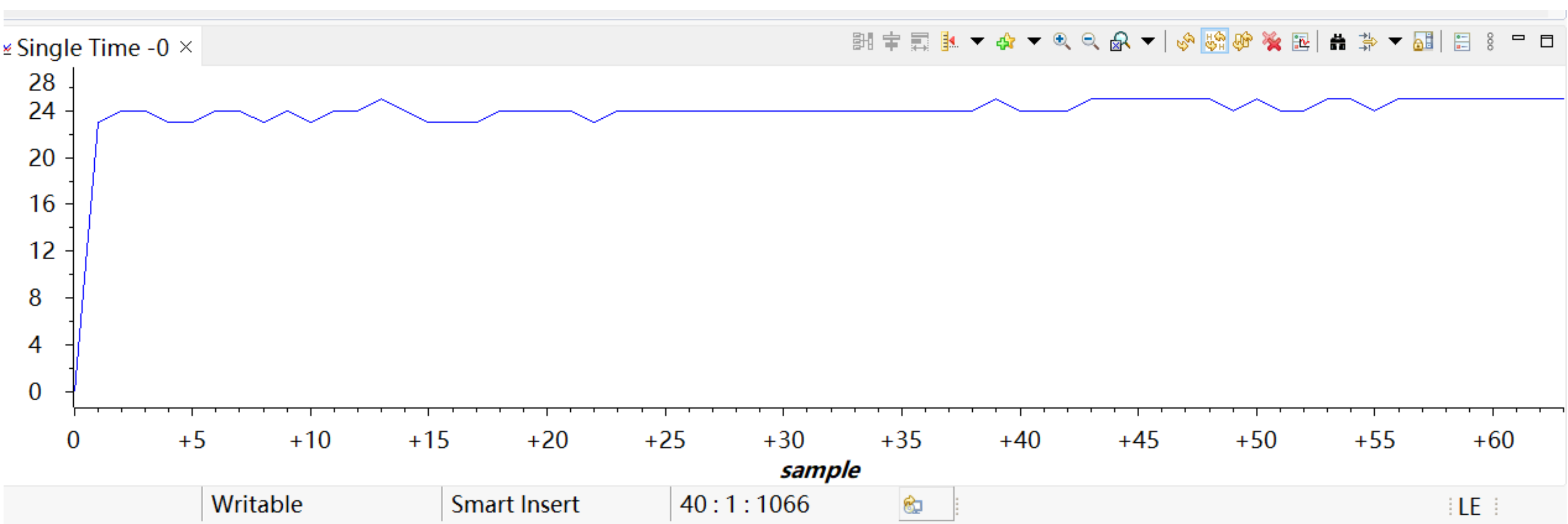
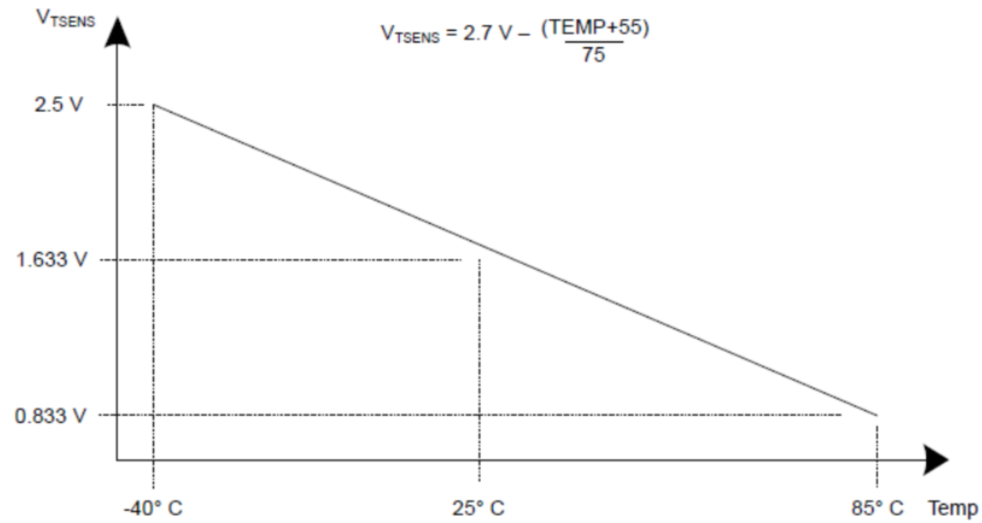
- Each ADC module has an on-chip internal temperature sensor.
  - To notify the system with the internal temperature;
  - To provide temperature measurements for calibration.





Preview: Lab06 (2/2)

- The temperature reading from the temperature sensor can be given as a function of the ADC value.



$$\boxed{TEMP} = 147.5 - ((75 * \boxed{(VREFP - VREFN)} \times \boxed{ADC_{CODE}} / 4096)$$

- We will practice two types of **triggers**:
  - **Software Trigger:** requires the software to write a value to a specific ADC control register to start the conversion.
  - **Hardware Trigger:** requires a hardware signal to be asserted by a circuit or peripheral (e.g., timer).

ADC in TivaWare™ Library

4.2.2.27 ADCSequenceConfigure

Configures the trigger source and priority of a sample sequence.

Prototype:

```
void
ADCSequenceConfigure(uint32_t ui32Base,
                     uint32_t ui32SequenceNum,
                     uint32_t ui32Trigger,
                     uint32_t ui32Priority)
```

Parameters:

ui32Base is the base address of the ADC module.

ui32SequenceNum is the sample sequence number.

ui32Trigger is the trigger source that initiates the sample sequence; must be one of the **ADC_TRIGGER_**∗ values.

ui32Priority is the relative priority of the sample sequence with respect to the other sample sequences.

Description:

This function configures the initiation criteria for a sample sequence. Valid sample sequencers range from zero to three; sequencer zero captures up to eight samples, sequencers one and two capture up to four samples, and sequencer three captures a single sample. The trigger condition and priority (with respect to other sample sequencer execution) are set.

The *ui32Trigger* parameter can take on the following values:

- **ADC_TRIGGER_PROCESSOR** - A trigger generated by the processor, via the ADCProcessorTrigger() function.
- **ADC_TRIGGER_TIMER** - A trigger generated by a timer; configured with TimerControlTrigger().

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