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Question 1.

Lab 3.1 result

Answer:

Figure 1: add4 before

```
❯ ./riscv-lc uop benchmarks/add4.bin
[INFO]: Welcome to the RISCV LC Simulator

[INFO]: load the micro: uop
[INFO]: read 60 bytes from the program into the memory.

RISCV LC SIM > mdump 0x38 0x38


memory content [0x00000038..0x00000038]:
-----------------------------------
  0x00000038 (56) : 0xfffffffb

RISCV LC SIM >
```

Figure 2: add4 after

```
RISCV LC SIM > mdump 0x38 0x38


memory content [0x00000038..0x00000038]:
-----------------------------------
  0x00000038 (56) : 0xffffffff

RISCV LC SIM > q

bye.
```

Figure 3: count10 result

```
[INFO]: RISCV LC is halted.

RISCV LC SIM > rdump


current register/bus values:
-----------------------------------
cycle count  : 412
PC           : 0x00400000
IR           : 0x0000707f
STATE_NUMBER : 0x0000007f

BUS          : 0x00000000
MDR          : 0x0000707f
MAR          : 0x0000001c
Mem. content : 0x00000000
B            : 0x00000000
READY        : 0x00000000
registers:
zero    [x0]:   0x00000000
ra      [x1]:   0x00000000
sp      [x2]:   0x00000000
gp      [x3]:   0x00000000
tp      [x4]:   0x00000000
t0      [x5]:   0x00000020
t1      [x6]:   0x00000000
t2      [x7]:   0x00000037
fp/s0   [x8]:   0x00000000
s1      [x9]:   0x00000000
a0      [x10]:  0x00000000
a1      [x11]:  0x00000000
a2      [x12]:  0x00000000
a3      [x13]:  0x00000000
a4      [x14]:  0x00000000
a5      [x15]:  0x00000000
a6      [x16]:  0x00000000
a7      [x17]:  0x00000000
s2      [x18]:  0x00000000
s3      [x19]:  0x00000000
s4      [x20]:  0x00000000
s5      [x21]:  0x00000000
s6      [x22]:  0x00000000
s7      [x23]:  0x00000000
s8      [x24]:  0x00000000
s9      [x25]:  0x00000000
s10     [x26]:  0x00000000
s11     [x27]:  0x00000000
t3      [x28]:  0x00000000
t4      [x29]:  0x00000000
t5      [x30]:  0x00000000
t6      [x31]:  0x00000000
```

Figure 4: isa register values

```
[INFO]: RISCV LC is halted.

RISCV LC SIM > rdump


current register/bus values:
--------------------------------------
cycle count  : 364
PC           : 0x00400000
IR           : 0x0000707f
STATE_NUMBER : 0x0000007f

BUS          : 0x00000000
MDR          : 0x0000707f
MAR          : 0x0000007c
Mem. content : 0x00000000
B            : 0x00000000
READY        : 0x00000000
registers:
zero    [x0]:   0x00000000
ra      [x1]:   0x00000000
sp      [x2]:   0x00000000
gp      [x3]:   0x00000000
tp      [x4]:   0x00000000
t0      [x5]:   0x00000000
t1      [x6]:   0x00000000
t2      [x7]:   0x00000000
fp/s0   [x8]:   0x00000000
s1      [x9]:   0x00000084
a0      [x10]:  0xfffffffe
a1      [x11]:  0xffffffff
a2      [x12]:  0xfffff800
a3      [x13]:  0xffffffee
a4      [x14]:  0xfffffff9
a5      [x15]:  0x0000000a
a6      [x16]:  0x0000000d
a7      [x17]:  0x00000068
s2      [x18]:  0x00000000
s3      [x19]:  0x00000000
s4      [x20]:  0x00000000
s5      [x21]:  0x00000000
s6      [x22]:  0x00000000
s7      [x23]:  0x00000000
s8      [x24]:  0x00000000
s9      [x25]:  0x00000000
s10     [x26]:  0x00000000
s11     [x27]:  0x00000000
t3      [x28]:  0x00000000
t4      [x29]:  0x00000000
t5      [x30]:  0x00000000
t6      [x31]:  0x00000000
```

Figure 5: isa memory content

```
RISCV LC SIM > mdump 0x94 0x94


memory content [0x00000094..0x00000094]:
----------------------------------------
  0x00000094 (148) : 0xffffffee
```

Figure 6: swap before

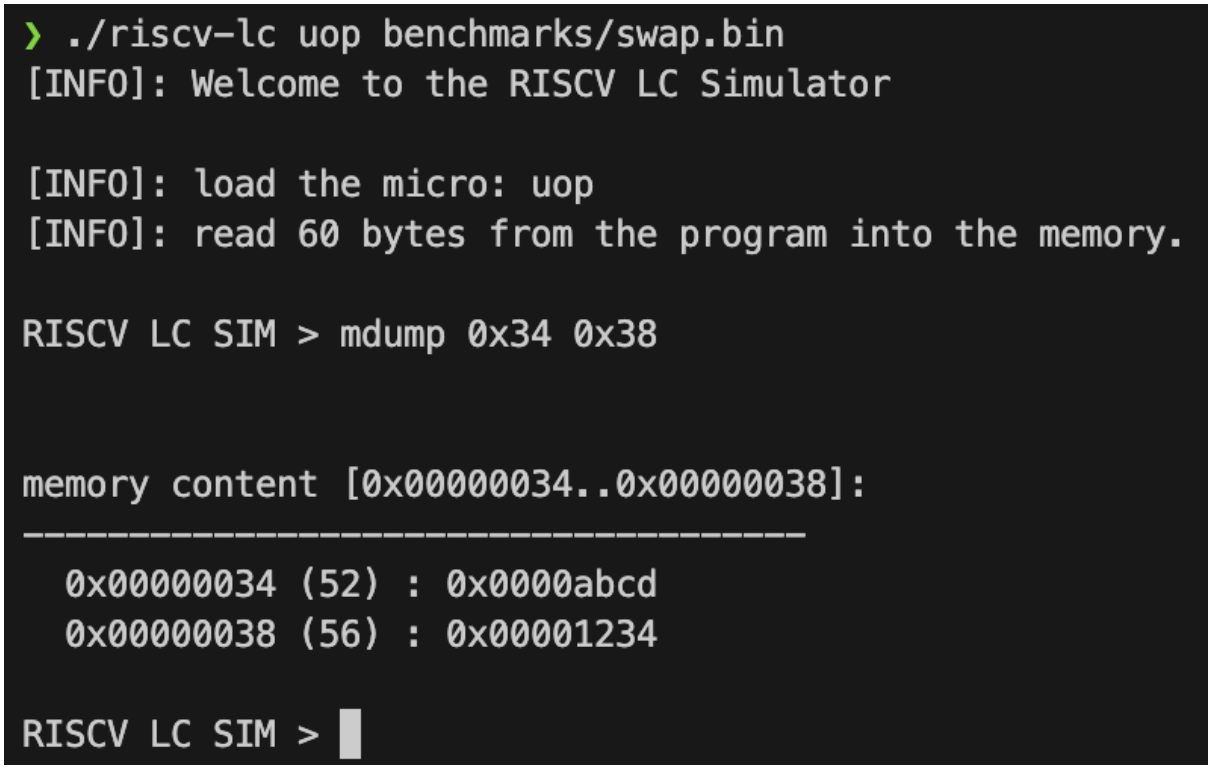
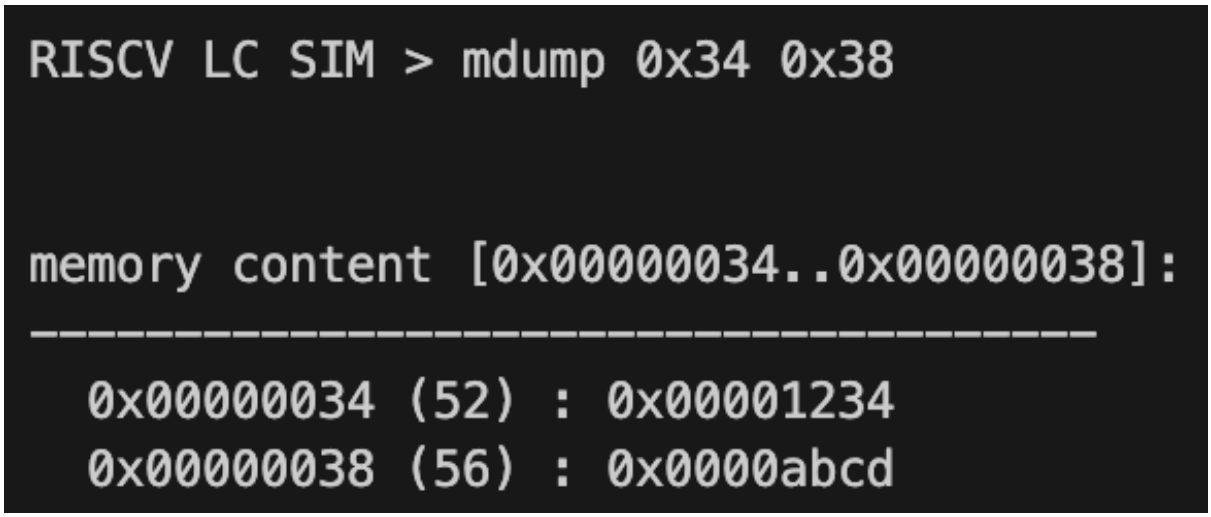


Figure 7: swap after



Question 2.

Lab 3.2 result

Answer:

Figure 8: add4 before

```
❯ ./riscv-lc uop benchmarks/add4.bin
[INFO]: Welcome to the RISCV LC Simulator

[INFO]: load the micro: uop
[INFO]: read 60 bytes from the program into the memory.

RISCV LC SIM > mdump 0x38 0x38


memory content [0x00000038..0x00000038]:
-----------------------------------
  0x00000038 (56) : 0xfffffffb

RISCV LC SIM >
```

Figure 9: add4 after

```
RISCV LC SIM > mdump 0x38 0x38


memory content [0x00000038..0x00000038]:
-----------------------------------
  0x00000038 (56) : 0xffffffff

RISCV LC SIM > q

bye.
```

Figure 10: count10 result

```
[INFO]: RISCV LC is halted.

RISCV LC SIM > rdump


current register/bus values:
-----------------------------------
cycle count  : 412
PC           : 0x00400000
IR           : 0x0000707f
STATE_NUMBER : 0x0000007f

BUS          : 0x00000000
MDR          : 0x0000707f
MAR          : 0x0000001c
Mem. content : 0x00000000
B            : 0x00000000
READY        : 0x00000000
registers:
zero    [x0]:   0x00000000
ra      [x1]:   0x00000000
sp      [x2]:   0x00000000
gp      [x3]:   0x00000000
tp      [x4]:   0x00000000
t0      [x5]:   0x00000020
t1      [x6]:   0x00000000
t2      [x7]:   0x00000037
fp/s0   [x8]:   0x00000000
s1      [x9]:   0x00000000
a0      [x10]:  0x00000000
a1      [x11]:  0x00000000
a2      [x12]:  0x00000000
a3      [x13]:  0x00000000
a4      [x14]:  0x00000000
a5      [x15]:  0x00000000
a6      [x16]:  0x00000000
a7      [x17]:  0x00000000
s2      [x18]:  0x00000000
s3      [x19]:  0x00000000
s4      [x20]:  0x00000000
s5      [x21]:  0x00000000
s6      [x22]:  0x00000000
s7      [x23]:  0x00000000
s8      [x24]:  0x00000000
s9      [x25]:  0x00000000
s10     [x26]:  0x00000000
s11     [x27]:  0x00000000
t3      [x28]:  0x00000000
t4      [x29]:  0x00000000
t5      [x30]:  0x00000000
t6      [x31]:  0x00000000
```

Figure 11: isa register values

```
[INFO]: RISCV LC is halted.

RISCV LC SIM > rdump


current register/bus values:
--------------------------------------
cycle count  : 364
PC           : 0x00400000
IR           : 0x0000707f
STATE_NUMBER : 0x0000007f

BUS          : 0x00000000
MDR          : 0x0000707f
MAR          : 0x0000007c
Mem. content : 0x00000000
B            : 0x00000000
READY        : 0x00000000
registers:
zero    [x0]:   0x00000000
ra      [x1]:   0x00000000
sp      [x2]:   0x00000000
gp      [x3]:   0x00000000
tp      [x4]:   0x00000000
t0      [x5]:   0x00000000
t1      [x6]:   0x00000000
t2      [x7]:   0x00000000
fp/s0   [x8]:   0x00000000
s1      [x9]:   0x00000084
a0      [x10]:  0xfffffffe
a1      [x11]:  0xffffffff
a2      [x12]:  0xfffff800
a3      [x13]:  0xffffffee
a4      [x14]:  0xfffffff9
a5      [x15]:  0x0000000a
a6      [x16]:  0x0000000d
a7      [x17]:  0x00000068
s2      [x18]:  0x00000000
s3      [x19]:  0x00000000
s4      [x20]:  0x00000000
s5      [x21]:  0x00000000
s6      [x22]:  0x00000000
s7      [x23]:  0x00000000
s8      [x24]:  0x00000000
s9      [x25]:  0x00000000
s10     [x26]:  0x00000000
s11     [x27]:  0x00000000
t3      [x28]:  0x00000000
t4      [x29]:  0x00000000
t5      [x30]:  0x00000000
t6      [x31]:  0x00000000
```

Figure 12: isa memory content

```
RISCV LC SIM > mdump 0x94 0x94


memory content [0x00000094..0x00000094]:
----------------------------------------
  0x00000094 (148) : 0xffffffee
```

Figure 13: swap before

```
❯ ./riscv-lc uop benchmarks/swap.bin
[INFO]: Welcome to the RISCV LC Simulator

[INFO]: load the micro: uop
[INFO]: read 60 bytes from the program into the memory.

RISCV LC SIM > mdump 0x34 0x38


memory content [0x00000034..0x00000038]:
------------------------------------
  0x00000034 (52) : 0x0000abcd
  0x00000038 (56) : 0x00001234

RISCV LC SIM >
```

Figure 14: swap after

```
RISCV LC SIM > mdump 0x34 0x38


memory content [0x00000034..0x00000038]:
------------------------------------
  0x00000034 (52) : 0x00001234
  0x00000038 (56) : 0x0000abcd
```

Question 3.

Lab 3.3 result

Answer:

Figure 15: add4 before

```
❯ ./riscv-lc uop benchmarks/add4.bin
[INFO]: Welcome to the RISCV LC Simulator

[INFO]: load the micro: uop
[INFO]: read 60 bytes from the program into the memory.

RISCV LC SIM > mdump 0x38 0x38


memory content [0x00000038..0x00000038]:
-----------------------------------
  0x00000038 (56) : 0xfffffffb

RISCV LC SIM >
```

Figure 16: add4 after

```
RISCV LC SIM > mdump 0x38 0x38


memory content [0x00000038..0x00000038]:
-----------------------------------
  0x00000038 (56) : 0xffffffff

RISCV LC SIM > q

bye.
```

Figure 17: count10 result

```
[INFO]: RISCV LC is halted.

RISCV LC SIM > rdump


current register/bus values:
-----------------------------------
cycle count  : 412
PC           : 0x00400000
IR           : 0x0000707f
STATE_NUMBER : 0x0000007f

BUS          : 0x00000000
MDR          : 0x0000707f
MAR          : 0x0000001c
Mem. content : 0x00000000
B            : 0x00000000
READY        : 0x00000000
registers:
zero    [x0]:   0x00000000
ra      [x1]:   0x00000000
sp      [x2]:   0x00000000
gp      [x3]:   0x00000000
tp      [x4]:   0x00000000
t0      [x5]:   0x00000020
t1      [x6]:   0x00000000
t2      [x7]:   0x00000037
fp/s0   [x8]:   0x00000000
s1      [x9]:   0x00000000
a0      [x10]:  0x00000000
a1      [x11]:  0x00000000
a2      [x12]:  0x00000000
a3      [x13]:  0x00000000
a4      [x14]:  0x00000000
a5      [x15]:  0x00000000
a6      [x16]:  0x00000000
a7      [x17]:  0x00000000
s2      [x18]:  0x00000000
s3      [x19]:  0x00000000
s4      [x20]:  0x00000000
s5      [x21]:  0x00000000
s6      [x22]:  0x00000000
s7      [x23]:  0x00000000
s8      [x24]:  0x00000000
s9      [x25]:  0x00000000
s10     [x26]:  0x00000000
s11     [x27]:  0x00000000
t3      [x28]:  0x00000000
t4      [x29]:  0x00000000
t5      [x30]:  0x00000000
t6      [x31]:  0x00000000
```

Figure 18: isa register values

```
[INFO]: RISCV LC is halted.

RISCV LC SIM > rdump


current register/bus values:
--------------------------------------
cycle count  : 364
PC           : 0x00400000
IR           : 0x0000707f
STATE_NUMBER : 0x0000007f

BUS          : 0x00000000
MDR          : 0x0000707f
MAR          : 0x0000007c
Mem. content : 0x00000000
B            : 0x00000000
READY        : 0x00000000
registers:
zero    [x0]:   0x00000000
ra      [x1]:   0x00000000
sp      [x2]:   0x00000000
gp      [x3]:   0x00000000
tp      [x4]:   0x00000000
t0      [x5]:   0x00000000
t1      [x6]:   0x00000000
t2      [x7]:   0x00000000
fp/s0   [x8]:   0x00000000
s1      [x9]:   0x00000084
a0      [x10]:  0xfffffffe
a1      [x11]:  0xffffffff
a2      [x12]:  0xfffff800
a3      [x13]:  0xffffffee
a4      [x14]:  0xfffffff9
a5      [x15]:  0x0000000a
a6      [x16]:  0x0000000d
a7      [x17]:  0x00000068
s2      [x18]:  0x00000000
s3      [x19]:  0x00000000
s4      [x20]:  0x00000000
s5      [x21]:  0x00000000
s6      [x22]:  0x00000000
s7      [x23]:  0x00000000
s8      [x24]:  0x00000000
s9      [x25]:  0x00000000
s10     [x26]:  0x00000000
s11     [x27]:  0x00000000
t3      [x28]:  0x00000000
t4      [x29]:  0x00000000
t5      [x30]:  0x00000000
t6      [x31]:  0x00000000
```

Figure 19: isa memory content

```
RISCV LC SIM > mdump 0x94 0x94


memory content [0x00000094..0x00000094]:
----------------------------------------
  0x00000094 (148) : 0xffffffee
```

Figure 20: swap before

```
❯ ./riscv-lc uop benchmarks/swap.bin
[INFO]: Welcome to the RISCV LC Simulator

[INFO]: load the micro: uop
[INFO]: read 60 bytes from the program into the memory.

RISCV LC SIM > mdump 0x34 0x38


memory content [0x00000034..0x00000038]:
-----------------------------------
  0x00000034 (52) : 0x0000abcd
  0x00000038 (56) : 0x00001234

RISCV LC SIM >
```

Figure 21: swap after

```
RISCV LC SIM > mdump 0x34 0x38


memory content [0x00000034..0x00000038]:
-----------------------------------
  0x00000034 (52) : 0x00001234
  0x00000038 (56) : 0x0000abcd
```