CENG3420 - Computer Organization & Design
Homework 1

1155193237 - Yu Ching Hei
email: chyu2@cse.cuhk.edu.hk

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Question 1. (10%) This is a question about integrated circuit cost. Assume that a wafer contains 4096 dies and a die has 0.15 defects on average, please answer the following sub-questions.

1. Calculate the yield of this wafer. (5%)
2. Assume that you wanted to spend 10 millions HKD on manufacturing, how much money can you save for manufacturing the same number of dies if the average defects of a die can be reduced to 0.075? (5%)

Answer:

1.
$$\text{Yield} = \frac{1}{[1 + (0.15 \div 2)]^2} = \frac{1600}{1849} = 86.5\%$$

2. Lets assuem the cost per wafer is \$C
   Then,
$$\text{Cost per die} = \frac{C}{\text{Die per wafer} \times \text{Yield}}$$
   Therefore,
$$\begin{aligned} \text{Saved money} &= 10,000,000 \times (\frac{\text{Yield}_{0.15}}{\text{Yield}_{0.075}} - 1) \\ &= 10,000,000 \times \{\frac{[1 + (0.15 \div 2)]^2}{[1 + (0.075 \div 2)]^2} - 1\} \\ &= 10,000,000 \times \frac{507}{6889} \\ &= \$735,956 (\text{round off to the nearest dollar}) \end{aligned} \tag{1}$$

Question 2. (10%)
Suppose we developed a new processor that has 70% of the capacitive load of the older processor. Further, it can reduce voltage 10% compared to previous generation, which results in a 20% shrink in frequency. What is the impact on dynamic power? Give the ratio of $\frac{\text{Power}_{\text{new}}}{\text{Power}_{\text{old}}}$

Answer: Given the power consumption of a processor can be computed by the following formula

$$\text{Power} = \text{Capacitive load} \times \text{Voltage}^2 \times \text{Frequency}^1$$

So we have the ratio

$$\text{Ratio} = \frac{70\% \times (1 - 10\%)^2 \times (1 - 20\%)}{1} = 0.7 \times 0.9^2 \times 0.8 = 0.4536$$

Question 3. (20%) We have an int (32 bits) array named arr0. The pointer of arr0's first element stored in register a0. Please answer the following questions.

1. How to put the 5th element of arr0 to register t1? (5%)
2. How to calculate t1 + 32 and store the result in register t2? (5%)
3. Find an efficient way to calculate t2 / 32 and t2 % 32. Please store the results in t3 and t4, respectively. Note that / is an integer division and % is the modulo operation. (hint: using shift and logical operations) (10%)

Answer:

1. `lw t1, 16(a0)`

2. `addi t2, t1, 32`

3.
   - Division:

     `srli t3,t2,5`

   - Modulo:

     `andi t4,t2,0x1F`

Question 4. (20%) We have an int (32 bits) array named arr1. The pointer to arr1's first element stored in register a0. We also have the registers t1 = 0xAAABCDEF, t2 = 0xF8000000 Please answer the following questions:

1. What is the value of t3 for the following sequence of instructions? (5%)

```
slli t3, t1, 12
srli t3, t3, 12
```

2. What is the value of t3 for the following sequence of instructions? (5%)

```
slli t3, t2, 4
srai t3, t3, 4
```

3. Write a piece of assembly program to: (10%)
   - Store the result of t1 XOR t2 to register t3 (3%)
   - Store t3 to the first element of arr1; (3%)
   - Store the lowest 8 bits of t3 to the third element of arr1. (4%)

Answer:

1. 0xBCDEF
2. 0xF8000000
3. - xor t3, t1, t2
   - sw t3, 0(a0)
   - andi t3, t3, 0xFF
     sw t3, 12(a0)

Question 5. (20%) Consider the following RISC-V instructions:

```
li t1, 5
li t2, 1
li t3, 0
LOOP:
beq t1, t3, DONE
mul t2,t2,t1
addi t1, t1, -1
jal ra, LOOP
DONE:
# end of the program
```

1. How many times is the loop executed (between LOOP and DONE)? (5%)
2. List the value of t2 at each loop iteration. (10%)
3. What does this program do? (5%)

Answer:

1. 5 full loop with one extra bew t1, t3, DONE instruction executed
2. 1, 5, 20, 60, 120, 120
3. factorial of t1

Question 6. (20%) This is a question about using stack. Write RISC-V instructions to implement the following functionalities.

1. Reserve a stack area that can save three words of data (1 word = 4 bytes). (5%)
2. Save the return address in ra, data in a0 and data in a1 to the stack. (5%)
3. Restore the return address and data in the stack to corresponding registers. (5%)
4. Free the reserved stack space. (5%)

Answer:

```
addi sp, sp, -12
sw ra, 0(sp)
sw a0, 4(sp)
sw a1, 8(sp)
lw a1, 8(sp)
lw a0, 4(sp)
lw ra, 0(sp)
addi sp, sp, 12
```