香港中文大學
The Chinese University of Hong Kong

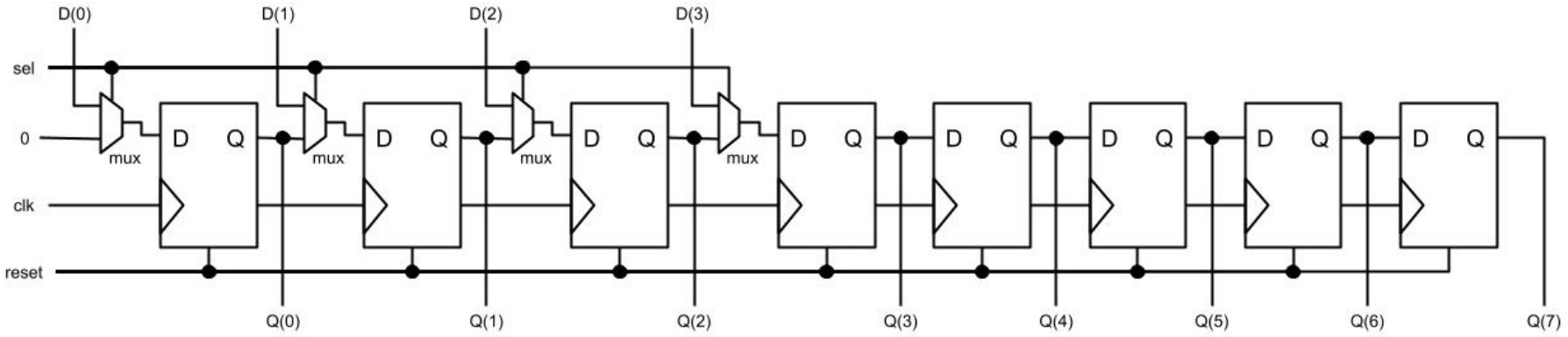
CENG3430 Rapid Prototyping of Digital Systems

Lab09: Shift Register in Verilog

Recall: PIPO in VHDL

Recall: Lab03 – PIPO Shift Register

- A **parallel-in-parallel-out (PIPO) shift register** is composed of **multiplexers (mux)** and **D-Flip-Flops (D-FF)** as follows:
  - It allows **parallel input** (through either external inputs (**Din**) or the shifted outputs from previous D-FFs (**Q**) based on the select signal (**sel**) at rising edges of clock (**clk**));
  - It produces **parallel output** (through external outputs (**Q**)).



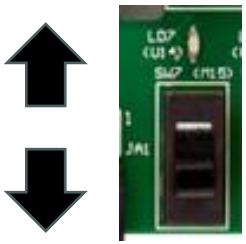
Recall: Lab03 – PIPO Shift Register

- When **reset** equals to 1:
  - All the **Q(s)** are reset to zero(s) **asynchronously** (immediately).

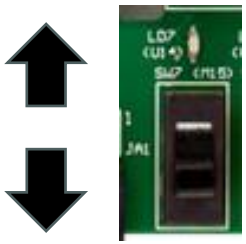
- Otherwise (when **reset** equals to 0), at every **rising edge** of **clk**:
  - When **sel** is 1, the values of **Din** are assigned to **Q** of D-FFs in parallel;
  - Otherwise (when **sel** is 0), the value kept by each D-FF is shifted to the D-FF on its right.
    - A '0' is shifted into to the "leftmost" D-FF;
    - The value kept by the "rightmost" D-FF is shifted out (i.e., discarded) from the PIPO shift register.

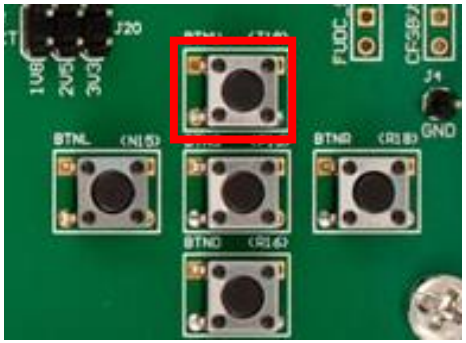
Recall: Lab03 – PIPO Shift Register

- Instructions:
  - Select the digit using SW 0-3
  - Press BTNU and toggle the SW7 at the same time
    - The digit will display on the LED 0-3
  - Then toggle the SW7 only
    - The digit will shift left
  - Press BTNC to reset the LED 0-3



Shift Left

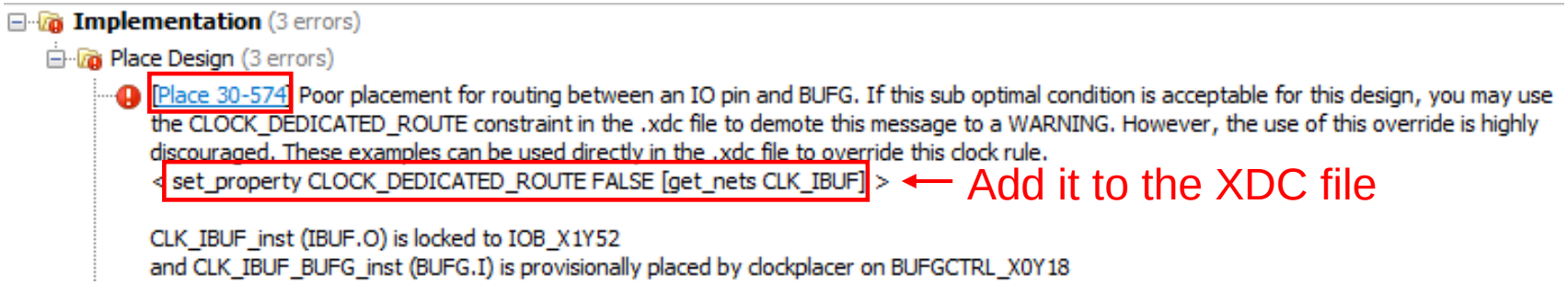




Display digit on the right

Notes on Constraints (XDC file)

- Add the following statement into XDC file when encountering error [Place 30-574].

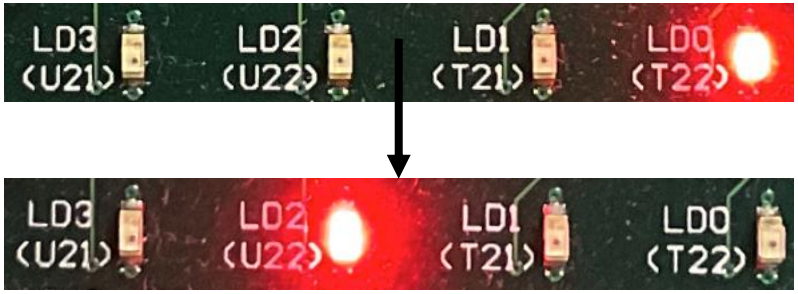


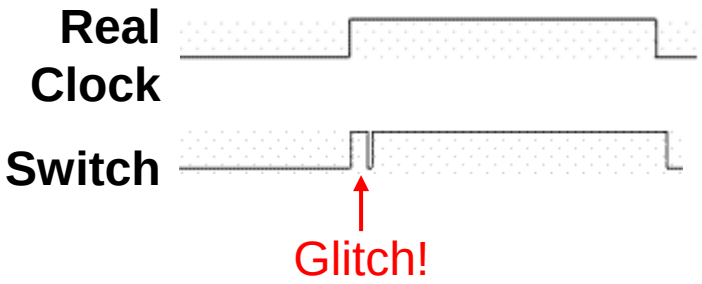
  - The reason is that We bind the signal clk to a switch, which is not a real clock.
  - This statement is also required for Verilog project.

```
architecture arch_dff of D_FF is
begin
    process (clk, reset)
    begin
        if reset = '1' then
            Q <= '0';
        elsif rising_edge(clk) then
            Q <= D;
        end if;
    end process;
end arch_dff;
```

Little Problem: Glitch

- If you switch once SW7 but the SIPO shifts twice, you encounter a glitch.



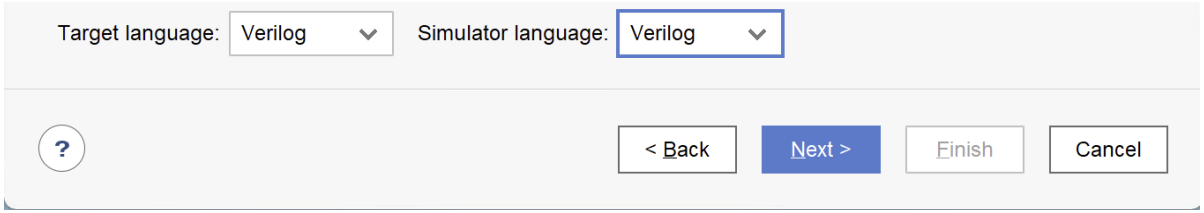


- The glitch is caused by the poor switch contact.
  - Operating once (by human) causes multiple positive edge in the signal.
  - It is also called by switch bouncing.

Task: PIPO in Verilog

Lab09: Step-by-Step Instructions (1/2)

1. Use the structural design to implement the PIPO shift register in Verilog.
   - You can try to translate your VHDL codes of Lab03 into Verilog.
   - When creating the project, please remember to select Verilog as the target language.



2. Create a XDC file with the following assignments:
   - Input: **clk** = SW7, reset = BTNC, **sel** = BTNU, **D0~D3** = SW0~SW3
   - Output: **Q0~Q7** = LD0~LD7
   - Add the following statement to your XDC file:

```
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets clk_IBUF];
```

Lab09: Step-by-Step Instructions (2/2)

3. Generate the bitstream and download it to Zedboard.
4. Toggle SW7 regularly to simulate the **clk** and verify the behavior of your design as follows:
   ① Set D to “0101”, press BTNU and toggle SW7;
   ② Toggle SW7 only until “0101” move to SW4-7;
   ③ Set D to “1010”, press BTNU and toggle SW7;
   ④ Then toggle SW7 three more times to shift the digit;
   ⑤ Asynchronously **reset** PIPO by pressing BTNC.
   ⑥ Record the above verification as a video for submission.
5. Submit your source code.
   – Submit the zip file of source codes and verification video to Blackboard.
   – Deadline: **12:30 on 2 Apr. 2025**
      ➢ Late submission is NOT acceptable (unless otherwise approved)

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Thank You!