Name: Yu Ching Hei
Student ID: 1155193237
email: chyu2@cse.cuhk.edu.hk

2 Standard Cell Library

1. (a) A, B, S
   (b) Y
   (c) (!((S A) + (!S B)))
   (d) 18.5503
2. (a) 0.76×2.47
   (b) 1.52×2.47
   (c) **metal1:** horizontal
   metal2: vertical

3 Synthesis Using Synopsys Design Compiler

1. **Slack:** -0.07ns
   Total cell area: 338.834592μm^2
2. 301.759893μm^2
3. **Shortest clock period:** 0.210000ns
   Corresponding clock frequency: 4.761905GHz
   Total cell area: 297.066893μm^2
4. No.
   Setting max_area to 0 basically tells the compiler to optimize the design for minimum area without any upper bound constraints.