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CENG4120 - VLSI CAD

Assignment 3 - Part B

Date: April 21, 2025

1. DRC Violation: 0

Total Area: 258.115 μm^2

Total Power: $2.33769348 \ mW$

Slack: 0.031 ns

2. $263.7466 \ \mu m^2$

3. Total area unchanged, while slack reduced to 0.024 ns with increasing row density. Total area unchanged probably because of the power routing grid, and slack decreased because of the reduced separation between standard cells.

