CENG 4120

Computer-Aided Design for Very Large Scale Integrated Circuits

January 7, 2025

Lecture 1

Introduction

Course Information

- Lecturer:
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- Teaching Assistant
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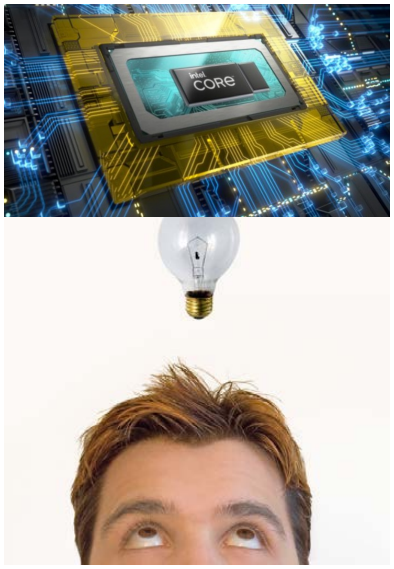
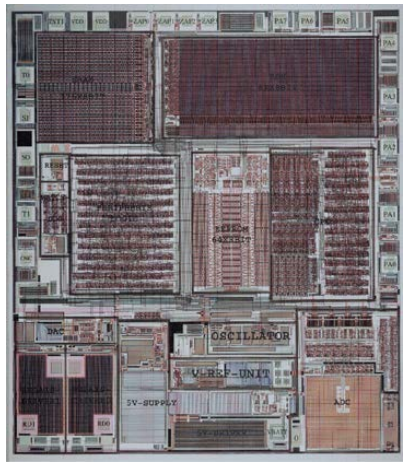
- Lecture: Tu 10:30-12:15 (MMW 706); W 2:30-3:15 (ERB 408)
- Tutorial: W 3:30-4:15 (ERB 408)

What is VLSI CAD Tools?



VLSI CAD tools

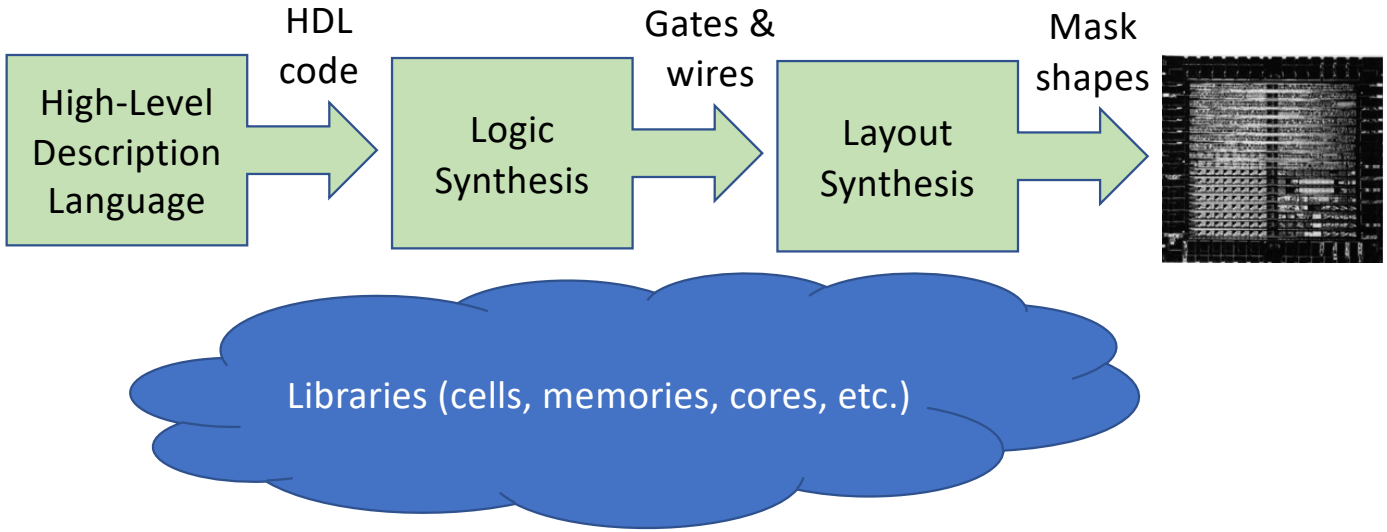


What Background do you need?

- Computer Science
  - Basic programming skills
  - Data structure
- Computer Engineering
  - Basic digital design (gates, flip-flops, Boolean algebra, K-maps)
  - Combinatorial and sequential design (finite state machines)
- Mathematics
  - Discrete (sets, functions, etc.)
  - Continuous (basic calculus, derivatives, integrals, matrices, etc.)
- Good to have some graph theory knowledge and chip layout exposure, but not necessary.

What is this Course about?

- CAD for semi-custom ASIC
  - ASIC = Application Specific Integrated Circuit
  - Semi-custom = Not fully customized, some parts of the design are re-used



Assessment Scheme

- Project + Proposal + Presentation 35%
- 3 Homeworks 25%
- Mid-term 30%
- Class Participation 10%

Topics

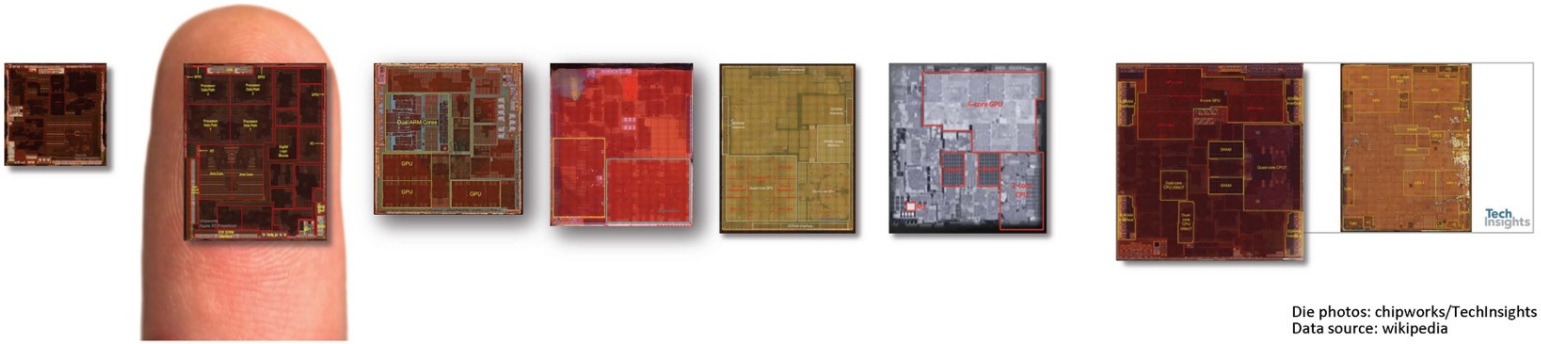
- Logic Synthesis
  - Computational Boolean algebra
  - Boolean verification, eg. BDDs and SAT
  - Logic Synthesis
- Physical Synthesis
  - Placement
  - Routing
  - Circuit Partitioning
  - Technology Mapping in FPGA

Tentative Schedule

Date	Topic	Date	Topic
7/8-Jan	Introduction / Computational Boolean Algebra	4/5-Mar	(Reading Week)
14/15-Jan	Computational Boolean Algebra / BDD	11/12-Mar	Global Routing
21/22-Jan	SAT	18/19-Mar	Mid-term (18/3)/ no class (conference trip)
28/29-Jan	CNY	25/26-Mar	Detailed Routing
4/5-Feb	Two-Level Synthesis	1/2-Apr	Special Net Routing/ Project Proposal (2/4)
11/12-Feb	Multi-Level Synthesis	8/9-Apr	Circuit Partitioning
18/19-Feb	Floorplanning	15/16-Apr	Technology Mapping
25/26-Feb	Placement	(May 6)	Final Project Presentation (Tue 10:30-12nn)

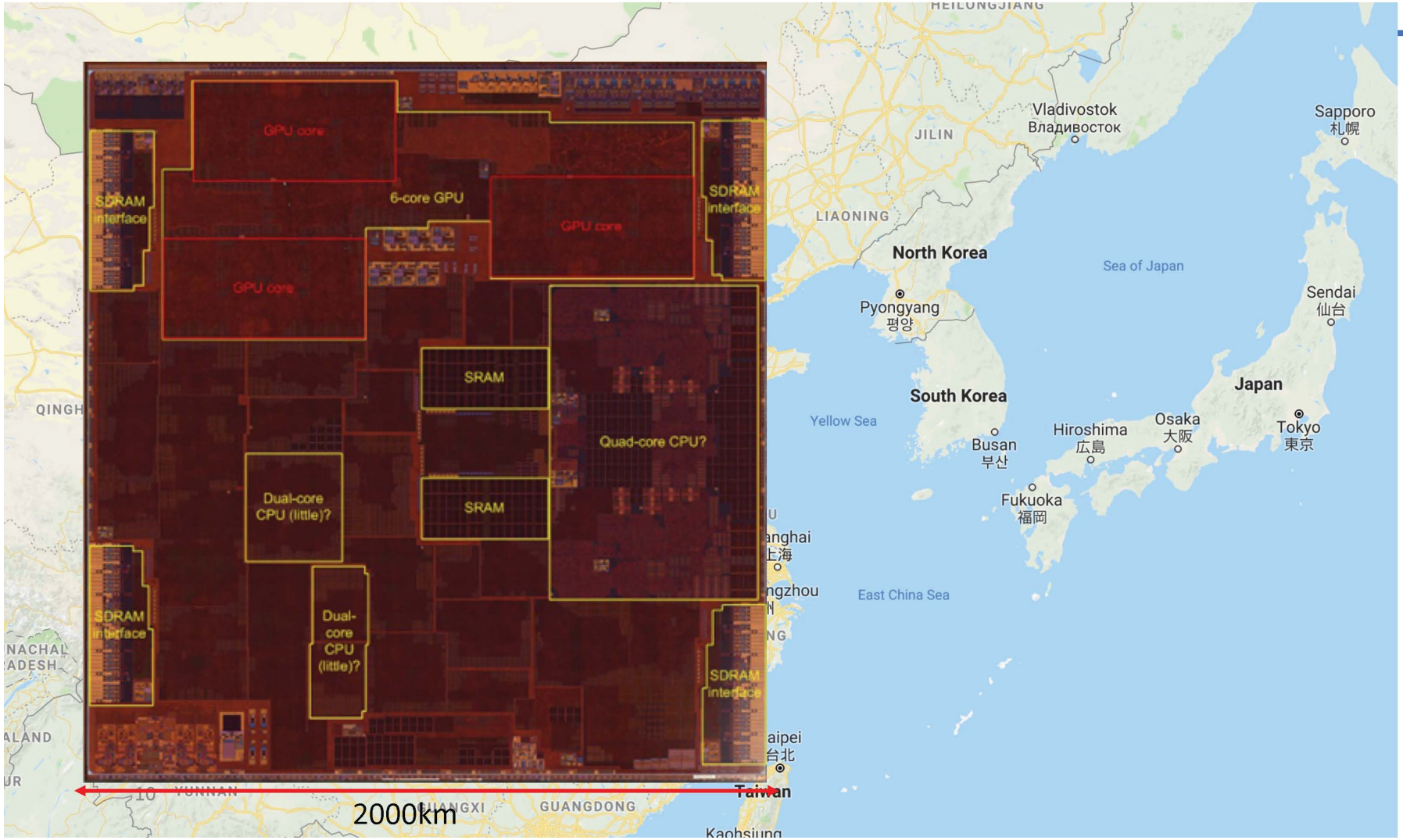
Advancement in Techonology

Chip	A4	A5	A6	A7	A8	A9	A10	A11	A15	A16
Year	2010	2011	2012	2013	2014	2015	2016	2017	2021	2023
Device	iPhone 4	iPhone 4s	iPhone 5	iPhone 5s	iPhone 6	iPhone 6s	iPhone 7	iPhone 8 & X	**iPhone 13**	**iPhone 15**
Node	45nm Samsung	45nm Samsung	32nm Samsung	28nm Samsung	20nm TSMC	16nm/14nm TSMC/Samsung	16nm TSMC	10nm TSMC	**5nm** TSMC	**4nm** TSMC
Area [cm2]	0.52	1.25	0.96	1.03	0.89	1.05/0.96	1.25	0.88	1.06	



Die photos: chipworks/TechInsights
Data source: wikipedia

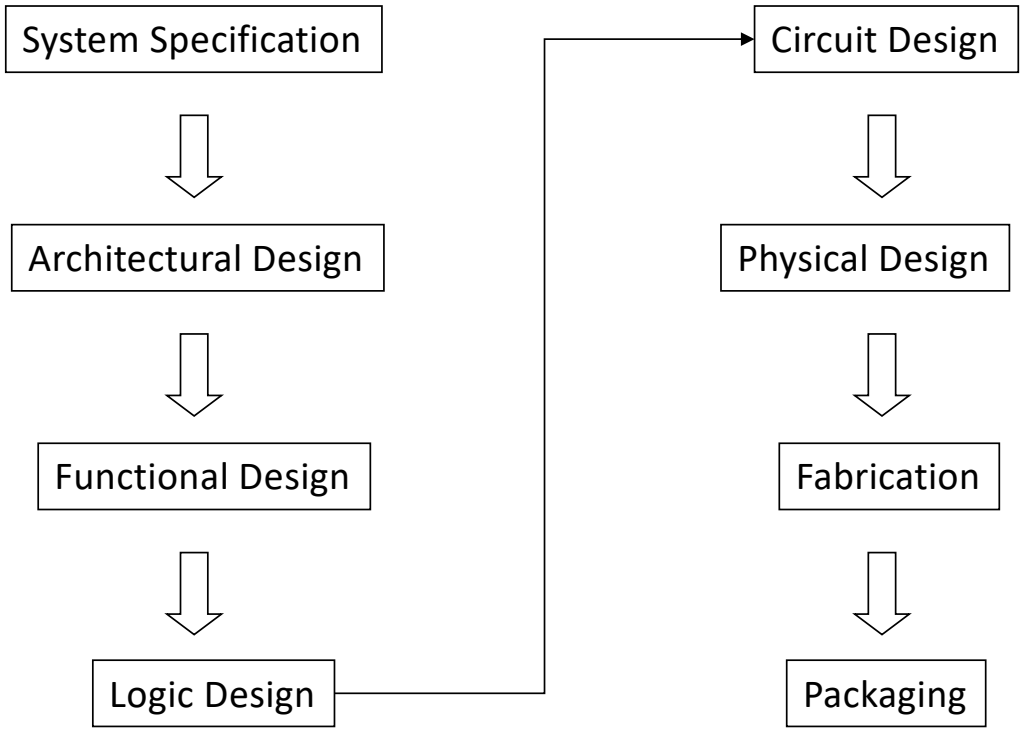
If the Wires on a 10nm Mobile SoC Were as Wide as Roads…



Chip: ~4million km2
Contains
~10 million km
wires in 10 layers.
Connecting
4.4 Billion transistors
in
0.2 Billion cells

USA: ~10million km2
Contains
~4.3 million km
paved roads in 1 layer.
Connecting
0.3 Billion people
in
0.14 Billion homes

VLSI Design Cycle



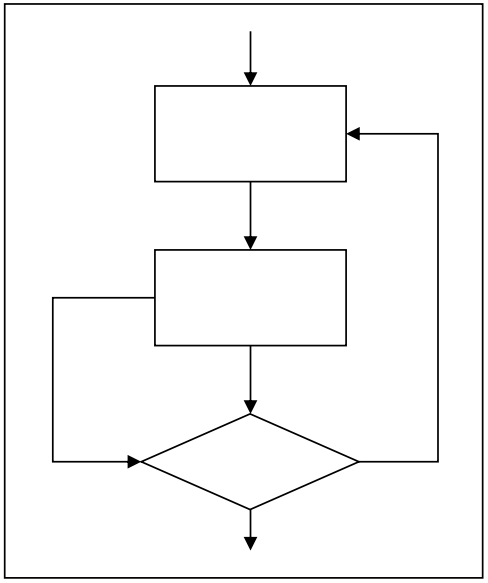
VLSI Design Cycle

- System Specification – Specification of the size, speed, power and functionality of the VLSI system.

- Architectural Design – Decisions on the architecture, e.g., no. of cores, RISC or CISC, no. of ALU's, pipeline structure, size of memory, cache size, etc. Such decisions can provide an estimation of the system performance, die size, power consumption, etc.

VLSI Design Cycle

- Functional Design – Identify main functional units and their interconnections. No detail of implementation is available yet.



VLSI Design Cycle

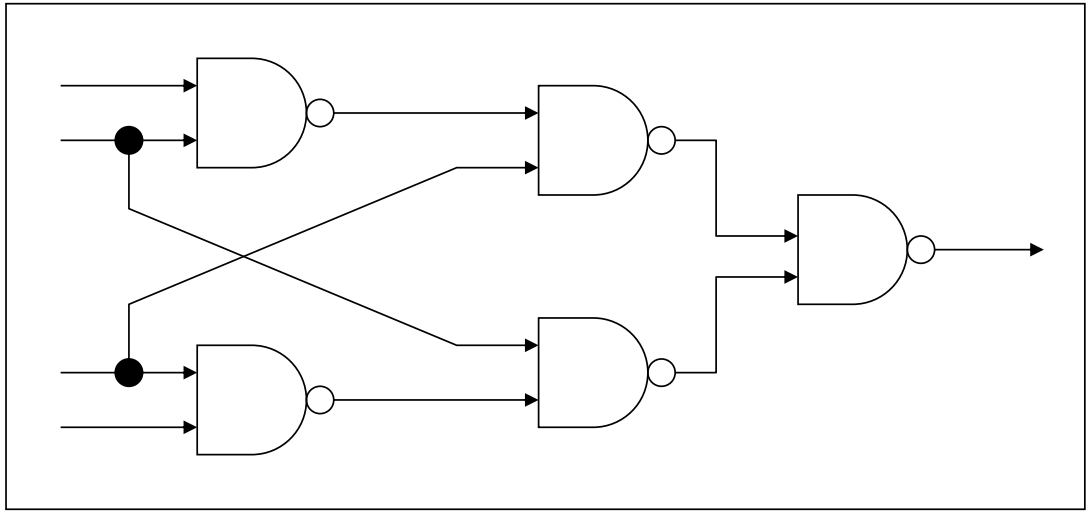
- Logic Design – Design the logic and related properties, e.g., control flow, word width, register allocation, etc. The outcome is called an RTL (*Register Transfer Level*) description, expressed in a HDL (*Hardware Description Language*), e.g., VHDL and Verilog.

$$X = (AB+CD)(E+F)$$
$$Y= (A(B+C) + Z + D)$$

Control flow expressed in Boolean expressions.

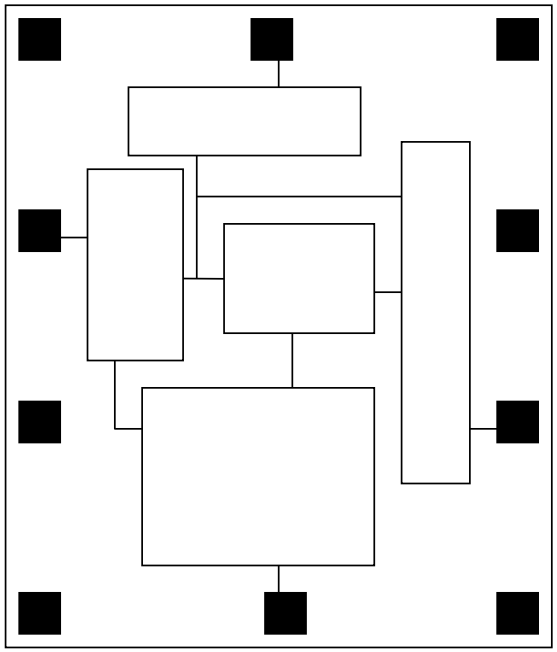
VLSI Design Cycle

- Circuit Design – Design the circuit including gates, transistors, interconnections, etc. The outcome is called a *netlist*.



VLSI Design Cycle

- Physical Design – Convert the netlist into a geometric representation. The outcome is called a *layout*.

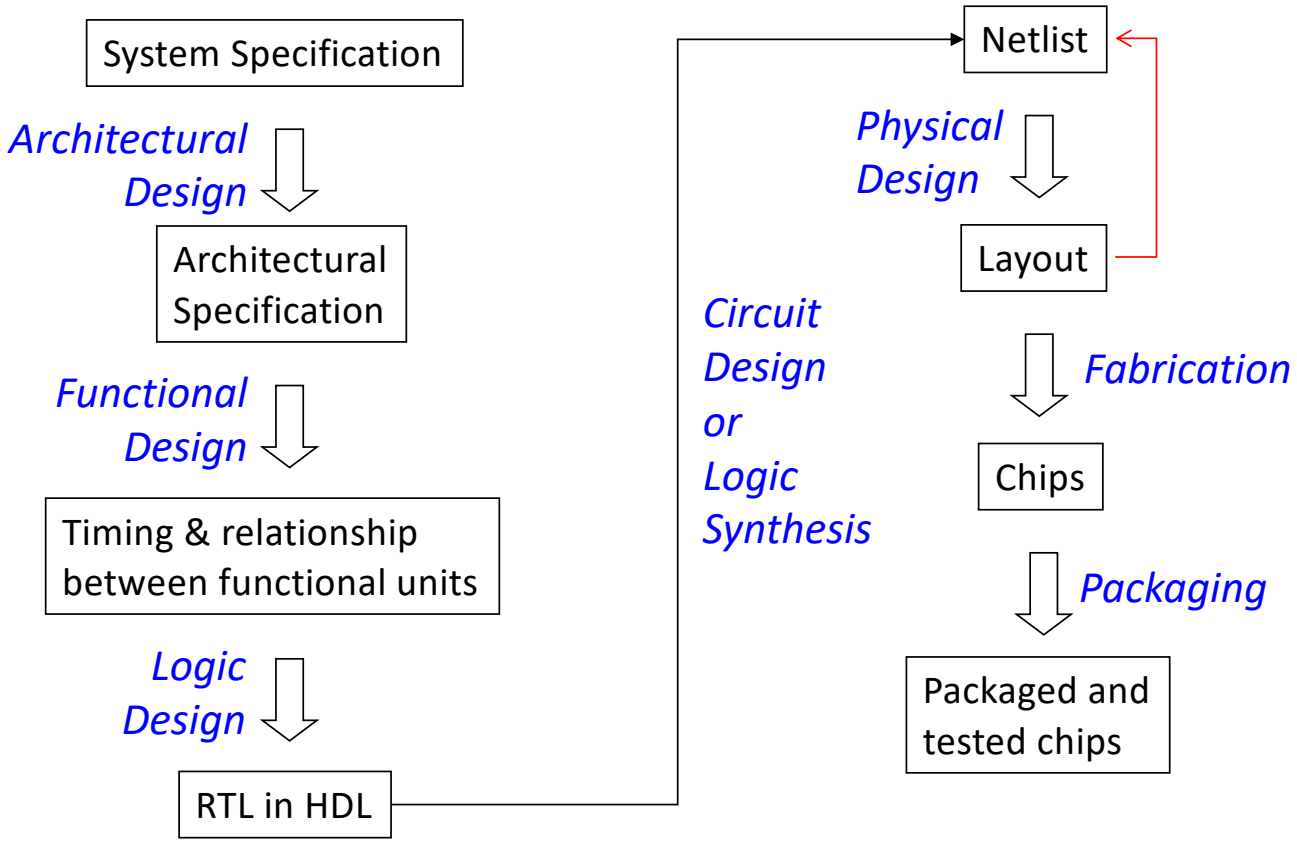


VLSI Design Cycle

- Fabrication – Process includes lithography, polishing, deposition, diffusion, etc. to produce a *chip*.

- Packaging – Put together the chips on a *PCB* (*Printed Circuit Board*) or an *MCM* (*Multi-Chip Module*)

VLSI Design Cycle



Design Styles

- Different design styles have different designing steps and designing objectives.
- Different design styles will thus lead to different designing problems.

Basic Design Styles

- Full custom design
- Standard cell design
- Field Programmable Gate Array design
- System-on-chip design
- 3D chip design

…. and very often, a mixture of the above.

Full Custom Design

- No rigid restrictions on the layout style.
- More compact design can be obtained.
- Longer design time.
- Hierarchical approach: chip → clusters → functional units.

Full Custom Design

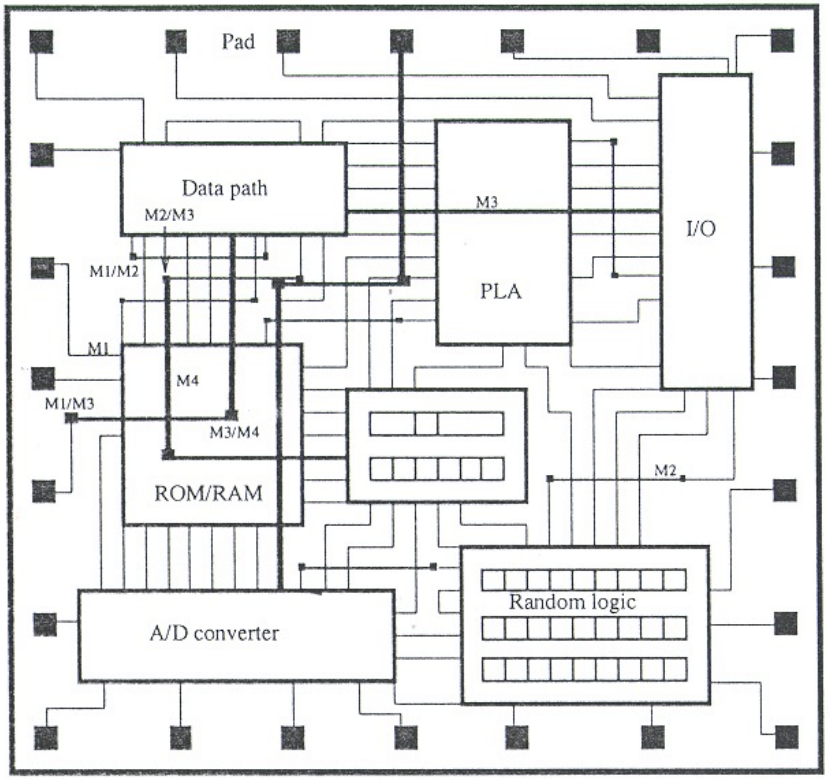
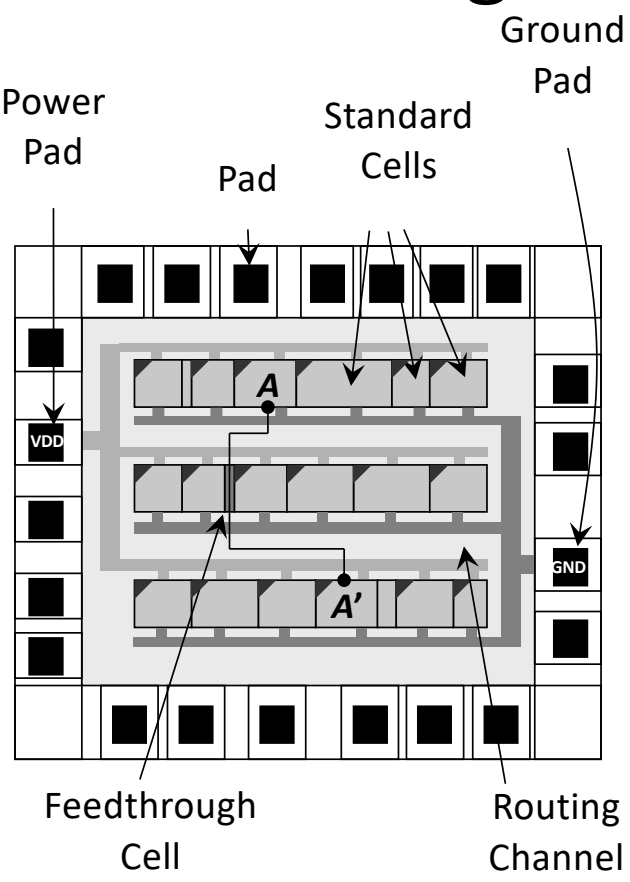


Figure 1.5: Full-custom structure.

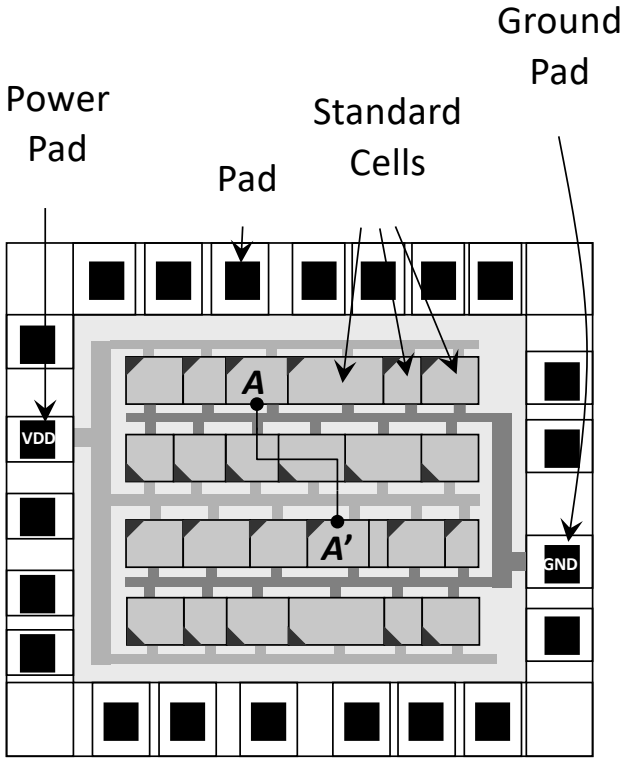
Standard Cell Design

- Make use of a library of small standard cells, each implements some simple logic.
- Standard cells are usually rectangular in shape and of the same height. Today, there are more and more multi-row cells.
- Cell library usually contains 500-1200 types of cells.
- Cells placed in rows and spaces between rows are called channels for routing. Today, channel routing is not that much.

Standard Cell Design

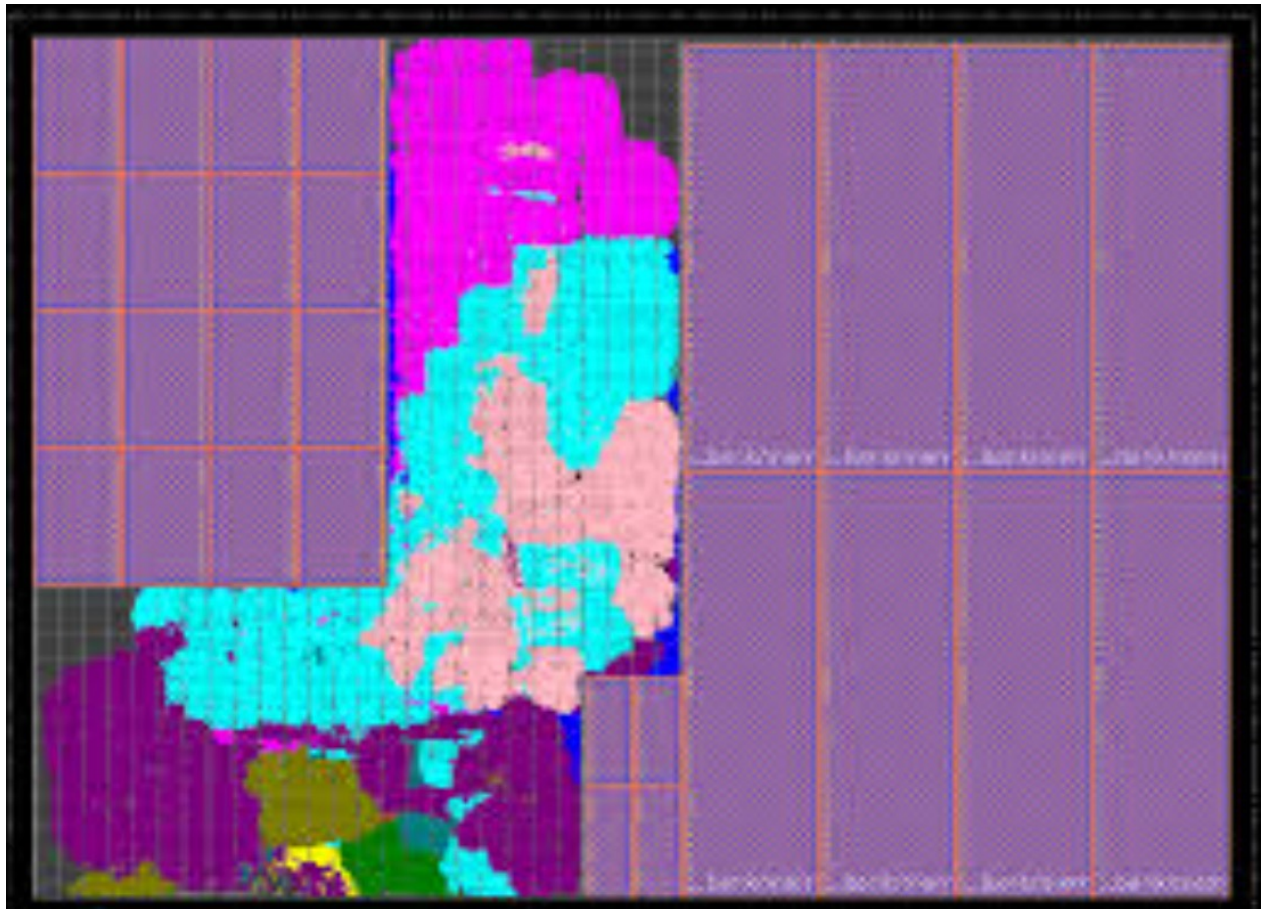


(a)



(b)

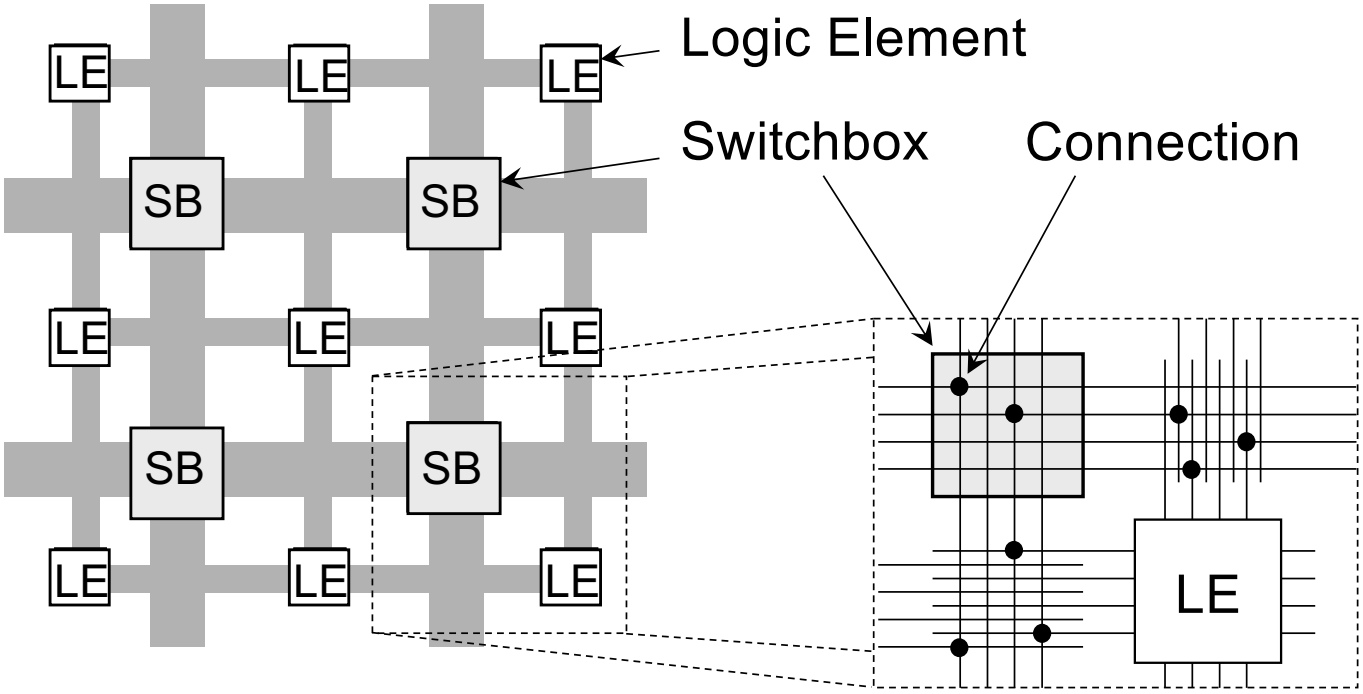
Macro Blocks with Sea of Standard Cells



Field Programmable Gate Array (FPGA)

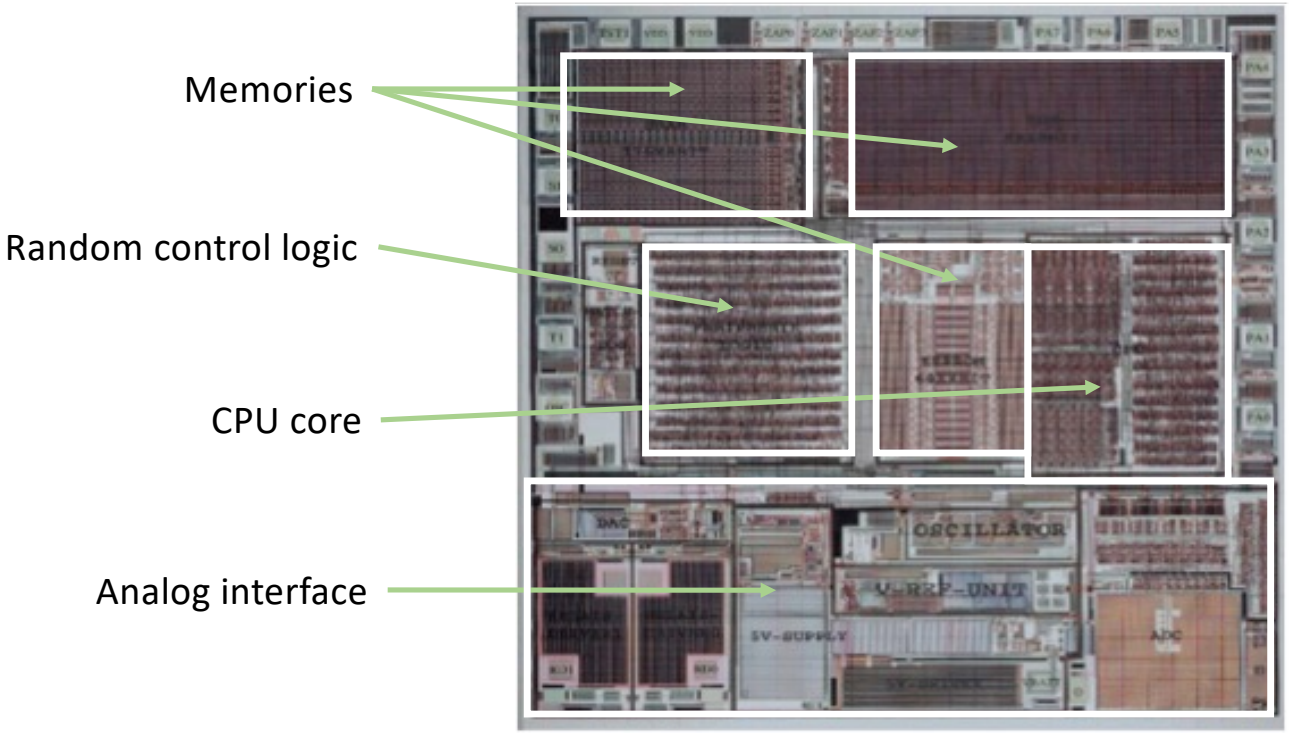
- Chips are prefabricated with logic blocks and interconnects.
- Logic and interconnects can be programmed (erased and re-programmed) by users. No fabrication is needed.
- Interconnects are predefined wire segments of fixed lengths with switches in between.

Field Programmable Gate Array (FPGA)

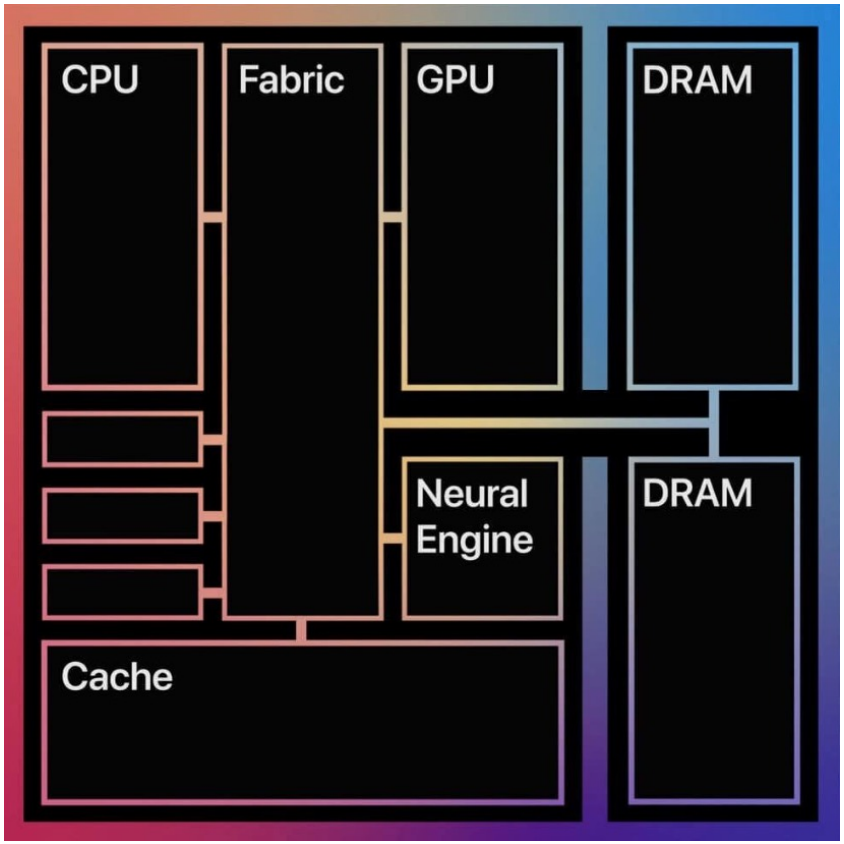


System-on-a-Chip (SOC)

- An integration of many functional blocks on one big chip.



Apple M1 Chip



Trends in VLSI

- Technology is improving progressively as predicted by the Moore's Law in the past:

Year	1989	1992	1995	1997	1999	2001	2004	2006	2010	2012	2014	2016	2019	2021
Techno-logy (μm)	0.8	0.5	0.35	0.25	0.18	0.13	0.09	0.065	0.032	0.022	0.014	0.01	0.007	0.005

- This is due to the continuous effort of shrinking the basic device sizes and a lot of manufacturing techniques.
- This process is called scaling.

Scaling

- The process of shrinking the layout in which every dimension is reduced by a factor is called Scaling.
- Transistors become smaller, less resistive, faster, conducting more electricity and using less power.
- Designs have smaller die sizes, higher yield and increased performance.
- In order to keep scaling work in the future, many technical problems need to be solved, eg., DFM.

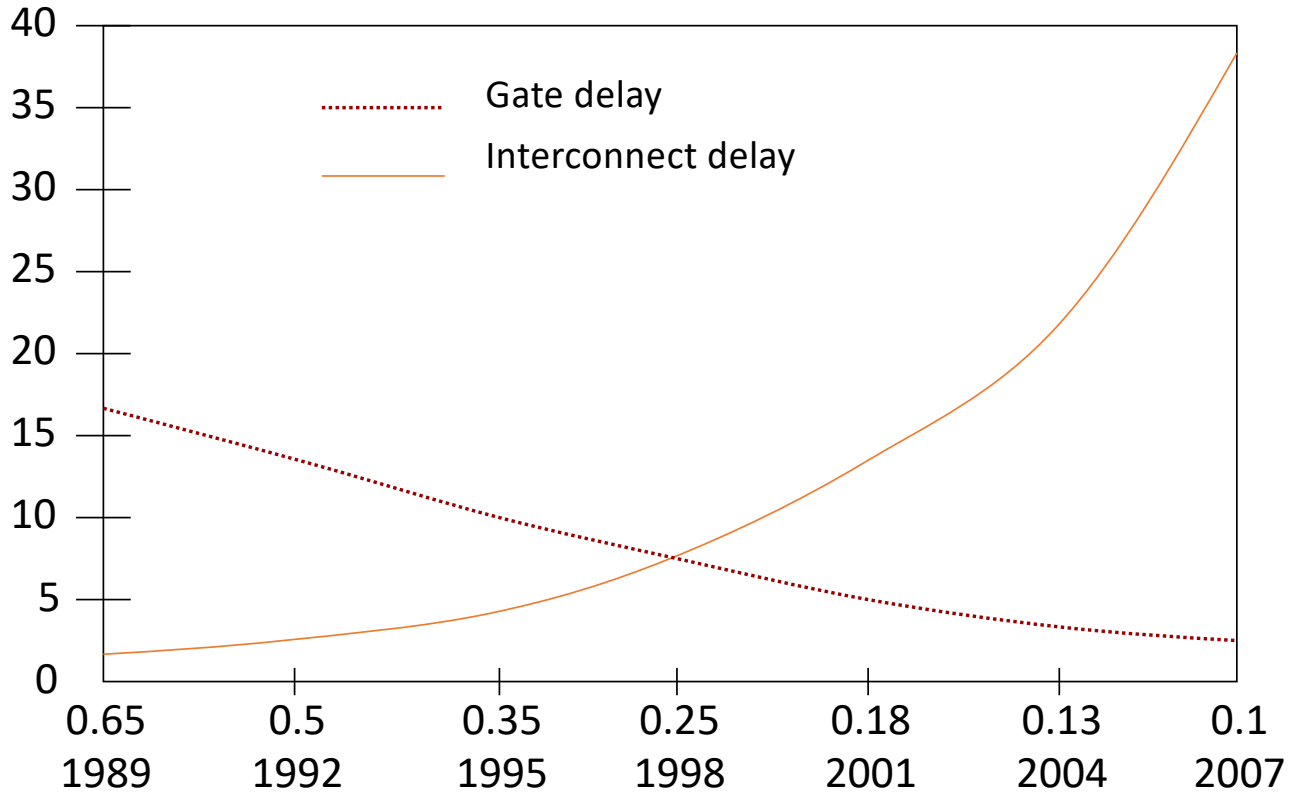
Trends in VLSI

- Transistor
  - Smaller, faster, use less power
- Interconnect
  - Less resistive, faster
- Yield
  - Smaller die size, higher yield

Can Scaling Continue?

- Some characteristics of transistors do not scale uniformly, eg., leakage current, threshold voltage, etc.
- Mismatch in scaling of transistors and interconnects. Interconnect delay has increased from 5-10% of the overall delay to 50-70%.
- Functionality increases which makes designs much more complicated.
- As technology improves, new problems arise, eg, manufacturing problems, process variations, noise problems.

Interconnect Delay



Design for Manufacturability

- As feature sizes shrink, more errors in the chip making process occur.
- Sub-wavelength lithography: 193nm light is used in 65nm, 45nm, 22nm or below 10nm technology nodes.
- Resolution enhancement techniques (RET), e.g., OPC, PSM, are the key enabling technology, but they are very expensive.
- CAD tools should plan for RETs
- Require new methodologies and algorithms

Manufacturing: Transport of an EUV System

New Challenges

- Complicated design
  - Too many transistors to be handled
- High power consumption and high heat dissipation
- Noise and crosstalk
- Too many and too long interconnects
- New design styles, e.g., SOC, NOC, 3D chips, FinFET, quantum circuits
- Design for manufacturability, lithography issues

Future Development