X

Left-to-right
dominates.

y →

y

X

gray scaled
[7:0]

[O]

0
0

256
[6]   1000_0000

196   255   ① 1 1   1 1 1 1   4bit
       − 196   ① 0 1 0 0 0 1 0 0
       ———   2
        40

Compute

56 = 0011 1000

pixel	x0	x1	x2	x3	x4	x5	x6

56

M9K   pixel2 x8
      pixel3

65K

 old

[7:0)

for (< code >) [7:0]   IRD
                            [7:0]
    old ← sram [x][y]   IRD
    [7:0]
    sram[x][y] ← closest(sram[x][y])
    [0] ?   [7:0]
    quant error ←—— old - closest (sram[x][y])
    [7:0]   [7:0] - [7:0]

    $$\frac{sram[x+1][y] \leftarrow sram[x+1][y] + quant \gg 4}{②\ [7:0]}$$ ③
                                                    ⑥
                                                    [7:0]   [7:0]

    x4   — — —
            — — —
            — —

D₁   Q₁

— addressP₁   Q address₁

—D₂   Q₂

—addressD₂   Q address₃

SPI-MOSI

canter.

MCU / FPGA block diagram:
- valid tx
- start sending
- SCLK
- MOSI
- MISO
- SS
- valid rx
- congu
- LCD
- MOSI, MISO, CO1, CO1

Kev — Server Limit. & Printer.

Jas — MCU flash 4MB.
_____
SPI controller.