

TABLE II  
DECODER PROPAGATION DELAYS

Input logic level transitions	Ratio <sup>a</sup> of delays	
	MSB	LSB
0-3	2.1	1.6
3-2	—	0.9
2-1	0.7	1.9
1-0	—	1.0
3-1	0.7	—
1-2	2.5	1.7
2-0	0.5	—
0-1	—	1.8
2-3	—	2.1
3-0	0.6	0.9

<sup>a</sup>The ratio is  $\left( \frac{\text{Decoder 50 percent} - \text{50 percent propagation delay}}{\text{CMOS inverter 50 percent} - \text{50 percent propagation delay}} \right)$

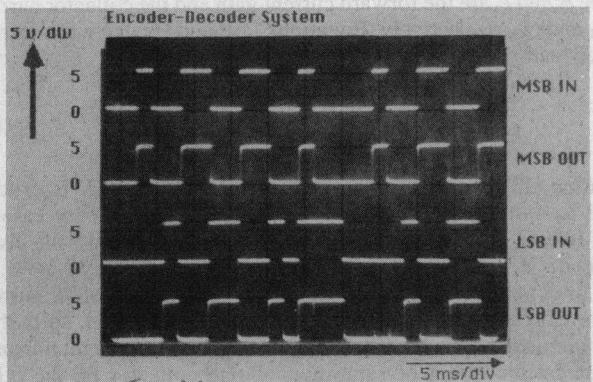


Fig. 11. Operation of the encoder-decoder pair.

been realized on a CMOS gate array chip were presented. These data represent intermediate results in our continuing investigation of MVL circuits. Minor problems in setting decoder comparator thresholds were noted to be characteristic of the selfbiasing, single-ended comparator used; the effects of which were compounded by the fixed, standard, gate array devices we were limited to using in this simplified design. Communication between VLSI chips with quaternary logic signals processed with circuits such as these could provide important new options for pin-limited chip architectures. Continued investigation into alternatives to binary signal processing, such as MVL, is necessary to be able to take full advantage in the future of the rapidly evolving IC fabrication technologies. Quaternary logic's potential has been widely acknowledged; reduction to practice remains a slow process. These studies attempt to carry the practical consideration of MVL closer to viability and stimulate discussion of the practical requirements of a 5 V four-valued signaling system.

#### ACKNOWLEDGMENT

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## The Current Mode Fuzzy Logic Integrated Circuits Fabricated by the Standard CMOS Process

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**Abstract** — Nine basic fuzzy logic circuits employing *p-ch* and *n-ch* current mirrors are presented, and the fuzzy information processing hardware system design at a low cost with only one kind of master slice (semicustom fuzzy logic IC) is described. The fuzzy logic circuits presented here will be indispensable for a "fuzzy computer" in the near future.

**Index Terms** — Current mode circuit, fuzzy computer, fuzzy integrated circuit, fuzzy logic array, fuzzy logic building block, MOS current mirror, ratioless circuit, semicustom IC.

#### I. INTRODUCTION

Advances in fuzzy set theory [1] have brought about its applications to an extensive field employing digital computers, or binary logic hardware systems. Although the fuzzy information processing employing a digital computer is useful for many purposes according to programming, it is not so effective with respect to the speed of processing, the power dissipation, the functional density, the design and fabrication cost, and so on. Accordingly, the hardware systems peculiar to fuzzy information processing will be needed. However, only a few papers on the electronic fuzzy logic circuits have been proposed [2]-[10].

Expansion of the practical applications of fuzzy information processing will excite the advent of many kinds of integrated circuits peculiar to fuzzy logic. The production of full-custom IC's, which are designed and fabricated for the specific purposes, is not so effective to supply many kinds of IC's. On the other hand, logic array IC's are very effective to meet the necessity of many kinds of IC's because one kind of logic array IC can be adapted to various specifications by designing only the connections between logic cells arrayed in a wafer called a master slice. This type of integrated circuits is called a semicustom IC.

This correspondence describes nine basic fuzzy logic circuits in current mode and fuzzy information processing hardware system design at a low cost with only one kind of master slice (semicustom fuzzy logic IC), which can be easily fabricated by the standard CMOS process.

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## II. BASIC FUZZY LOGIC FUNCTIONS

Basic fuzzy logic functions are defined in terms of membership functions  $\mu_x$  and  $\mu_y$  ( $0 \leq \mu_x, \mu_y \leq 1$ ) in the following where  $\vee$ ,  $\wedge$ ,  $+$ , and  $-$  denote MAX, MIN, algebraic sum, and algebraic difference, respectively.

### 1) Bounded Difference:

$$\mu_{x \ominus y} \triangleq 0 \vee (\mu_x - \mu_y) \quad (1)$$

$$= \mu_x \ominus \mu_y. \quad (1')$$

### 2) Fuzzy Complement:

$$\mu_{\bar{x}} \triangleq 1 - \mu_x \quad (2)$$

$$= 1 \ominus \mu_x. \quad (2')$$

### 3) Bounded Product:

$$\mu_{x \odot y} \triangleq 0 \vee (\mu_x + \mu_y - 1) \quad (3)$$

$$= (\mu_x + \mu_y) \ominus 1 \quad (3')$$

### 4) Fuzzy Logic Union (MAX):

$$\mu_{x \cup y} \triangleq \mu_x \vee \mu_y \quad (4)$$

$$= (\mu_x \ominus \mu_y) + \mu_y \quad (4')$$

$$= (\mu_y \ominus \mu_x) + \mu_x. \quad (4'')$$

### 5) Bounded Sum:

$$\mu_{x \oplus y} \triangleq 1 \wedge (\mu_x + \mu_y) \quad (5)$$

$$= 1 \ominus [1 \ominus (\mu_x + \mu_y)]. \quad (5')$$

### 6) Fuzzy Logic Intersection (MIN):

$$\mu_{x \wedge y} \triangleq \mu_x \wedge \mu_y \quad (6)$$

$$= \mu_x \ominus (\mu_x \ominus \mu_y) \quad (6')$$

$$= \mu_y \ominus (\mu_y \ominus \mu_x). \quad (6'')$$

### 7) Implication:

$$\mu_{x \rightarrow y} \triangleq 1(1 - \mu_x + \mu_y) \quad (7)$$

$$= 1 \ominus (\mu_x \ominus \mu_y). \quad (7')$$

### 8) Absolute Difference:

$$\mu_{|x-y|} \triangleq \begin{cases} \mu_x - \mu_y & (\mu_x \geq \mu_y) \\ \mu_y - \mu_x & (\mu_x < \mu_y) \end{cases} \quad (8)$$

$$= (\mu_x \ominus \mu_y) + (\mu_y \ominus \mu_x). \quad (8')$$

### 9) Equivalence

$$\mu_{x \leftrightarrow y} \triangleq \mu_{x \rightarrow y} \wedge \mu_{y \rightarrow x} \quad (9)$$

$$= 1 \ominus [(\mu_x \ominus \mu_y) + (\mu_y \ominus \mu_x)]. \quad (9')$$

All of the basic fuzzy logic functions presented here can be expressed only with the bounded difference and the algebraic sum, as described above. Thus, each basic fuzzy logic function circuit is implemented with the bounded difference circuit and the algebraic sum circuit. In the current mode circuits, the algebraic sum is implemented only by connecting two lines to be summed (wired sum). Therefore, the bounded-difference arrays can be adapted to many kinds of fuzzy information processing hardware systems, the design of which should be directed only to wiring between the bounded-difference circuits (i.e., basic logic cells).

## III. BASIC FUZZY LOGIC FUNCTION CIRCUITS AND MULTIPLE-FANOUT CIRCUIT EMPLOYING MOS CURRENT MIRRORS

A current mirror necessary for constructing the bounded-difference circuit or the basic logic cell is implemented with bipolar transistors or MOS FET's.

A bipolar current mirror produces two types of significant errors. One is caused by the base current or the finite forward current gain of transistors. Fig. 1(a) illustrates its aspect. Assuming that the electrical characteristics of two transistors  $Q_1$  and  $Q_2$  are identical to each other, the input current  $I_i$  and the output current  $I_o$  are obtained from Fig. 1(a) at a glance as

$$I_i = I_c + \frac{2}{\beta} I_c = I_c \left(1 + \frac{2}{\beta}\right) \quad (10)$$

$$I_o = I_c \quad (11)$$

where  $\beta$  and  $I_c$  are the forward current gain and the collector current of  $Q_1$  and  $Q_2$ , respectively. Equations (10) and (11) give the current mirror factor (or current mirror ratio)  $G_I$  as follows.

$$G_I = \frac{I_o}{I_i} = \frac{I_c}{(1 + 2/\beta)I_c} = \frac{1}{(1 + 2/\beta)}. \quad (12)$$

Equation (12) shows that the current mirror factor  $G_I$  is exactly equal to unity only if  $\beta = \infty$ . However, in the ordinary case of  $\beta \approx 100$ ,  $G_I$  is 0.98, and in the case of the standard  $I^2L$ , the lower value of  $\beta = 2-20$  [11]-[13] inadequately gives  $G_I \approx 0.5-0.9$ . In contrast with the bipolar current mirror, an MOS current mirror has the input and output current paths separated, so that no error nominally appears. The other error in bipolar current mirror is caused by the effect of saturation of one collector on the other collectors. It is shown in Fig. 2. The more collectors saturate, the more other collector current is reduced, while drain currents of an MOS current mirror are independent of each other. Since these significant errors are not permissible for fuzzy logic circuits, the multivalued  $I^2L$  family [14] is not suitable for fuzzy logic.

On the other hand, an MOS current mirror produces little error even in the case of multiple-output current mirror. Akiya and Nakashima [15] presented a higher matching accuracy of an MOS current mirror with matching error of less than 0.5 percent even in lower current regions and a smaller pattern area than similar bipolar current mirrors. Therefore, an MOS current mirror is adopted in this correspondence.

The combination of this current mirror and the diode, which is easily obtained from an FET with gate connected to drain, give the basic logic cell shown in Fig. 3. It forms all of the basic fuzzy logic function circuits and thus the various complicated fuzzy hardware systems. In Fig. 3, if the input current,  $I_{i1}$  flows out from the input terminal of the p-MOS current mirror, the same amount of current  $I_D = I_{i1}$  flows out from the output terminal of the current mirror. When  $I_{i2} \geq I_{i1}$ , the output current of the basic logic cell  $I_o$  is equal to  $I_{i2} - I_{i1}$ . When  $I_{i2} < I_{i1}$ , the output current  $I_o$  is equal to 0A, because the reverse current is blocked by the diode  $D$ . Thus,

$$I_o = \begin{cases} I_{i2} - I_{i1} & (I_{i2} \geq I_{i1}) \\ 0 & (I_{i2} < I_{i1}) \end{cases} \quad (13)$$

$$= 0 \vee (I_{i2} - I_{i1}). \quad (13')$$

The use of an FET of diode connection  $D$  facilitates zero error operation under the conditions discussed later on (Section IV).

In this circuit, replacing the input current  $I_{i1}$  and  $I_{i2}$  by  $\mu_y$  and  $\mu_x$ , respectively, we can obtain the output current  $I_o = \mu_x \ominus \mu_y = \mu_{x \ominus y}$ . Therefore, the basic logic cell shown in Fig. 3 operates as the bounded-difference circuit. This circuit exhibits multiple functions according to the assignment of the input current  $I_{i1}$  and  $I_{i2}$ , as shown in Table I.

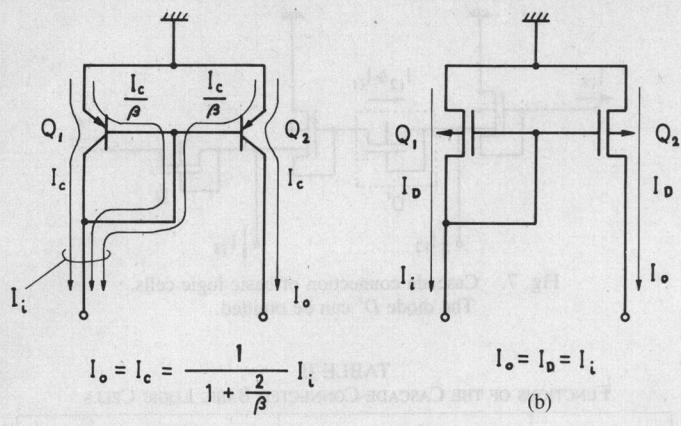


Fig. 1. (a) Current mirror circuit employing p-n-p transistors. (b) Current mirror circuit employing enhancement p-ch MOS FET's. (c) Symbol of p-MOS current mirror circuit.

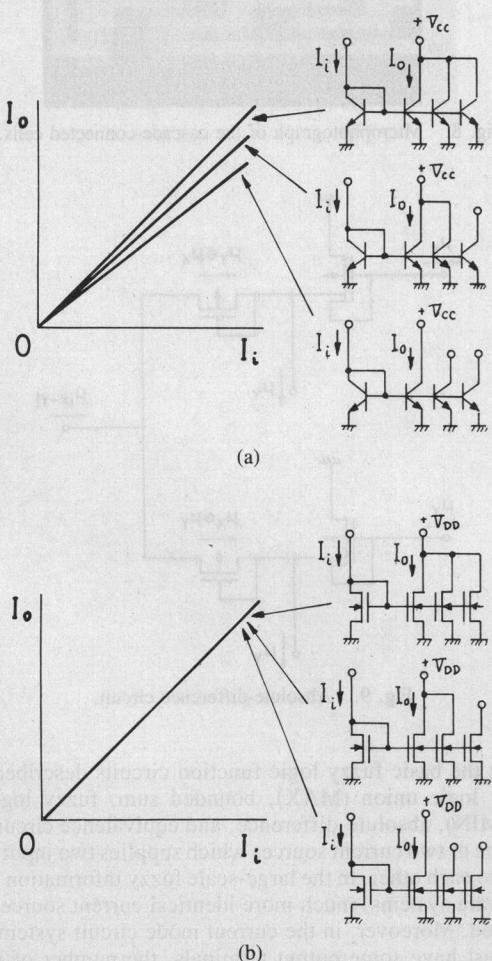


Fig. 2. Input-output characteristics of current mirrors implemented with (a) bipolar transistors and (b) MOS FET's.

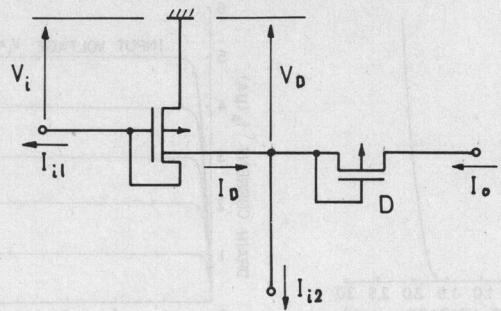


Fig. 3. Basic logic cell circuit.

TABLE I  
FUNCTIONS OF THE BASIC LOGIC CELL

functions	Input		Output
	I <sub>i1</sub>	I <sub>i2</sub>	
Bounded-Difference	$\mu_Y$	$\mu_X$	$\mu_X \ominus \mu_Y$
Complement	$\mu_X$	1	$\mu_X^+ = 1 \ominus \mu_X$
Bounded-Product	1	$\mu_X + \mu_Y$	$\mu_X \odot \mu_Y = (\mu_X + \mu_Y) \ominus 1$

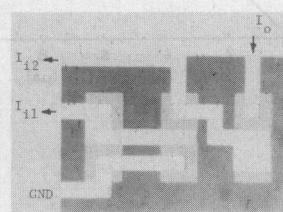


Fig. 4. Microphotograph of the basic logic cell.

Fig. 4 shows a microphotograph of the basic logic cell circuit which is composed of three MOS FET's. It is fabricated in the standard A1 gate MOS technology. The substrate material is an n type wafer having (511) surface orientation and its resistivity is  $30 \Omega \cdot \text{cm}$ . The thickness of gate oxide and field oxide are 700 Å and 2000 Å, respectively, and W/L ratios of all MOS FET's are designed to be 4. The characteristics of the fabricated basic logic cell are shown in Fig. 5. The input characteristics shown in Fig. 5(a) exhibit a rectification and a low input resistance with offset voltage of 1.5 V (which represents the threshold voltage of the p MOS FET composing the current mirror). Fig. 5(b) shows the  $V_D - I_D$  characteristics of the p MOS FET. It illustrates a high drain resistance and a small drain pinch off voltage of about 0.5 V. The input-output characteristics of the current mirror is shown in Fig. 5(c), which shows good linearity. Fig. 5(d) shows the input-output characteristics of the basic logic cell. It illustrates a good linearity and a very small error which can not be easily realized in the voltage mode circuit. This suggests that the basic logic cell can be appropriated to a binary logic and even to a 10-valued logic.

Adding only one input terminal to the basic logic cell brings it to the fuzzy logic union (MAX) circuit as shown in Fig. 6. It needs two input currents identical to each other.

Fig. 7 shows the cascade connection of two basic logic cells. It also exhibits multiple functions according to the assignment of the input currents  $I_{i1}, I_{i2}, I_{i3}$ , as shown in Table II. In this circuit, the input characteristics of the second current mirror exhibits a rectification as described above, so that the diode in the first stage can be omitted. The microphotograph of this circuit is shown in Fig. 8.

Wired sum of two basic logic cells gives us the absolute-difference circuit as shown in Fig. 9. The cascade connection of this

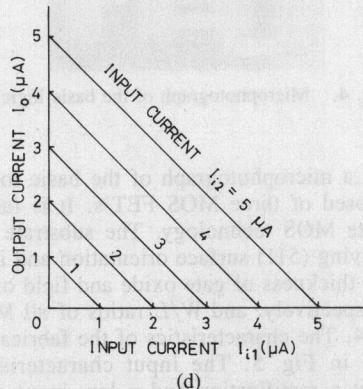
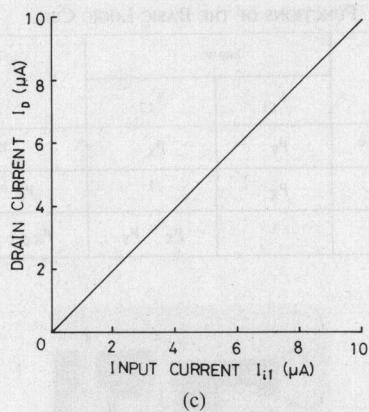
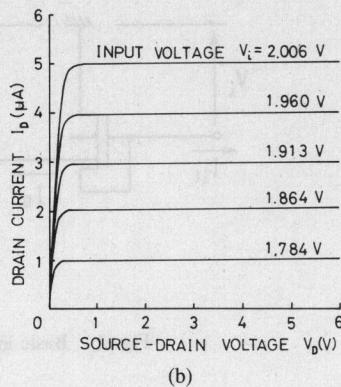
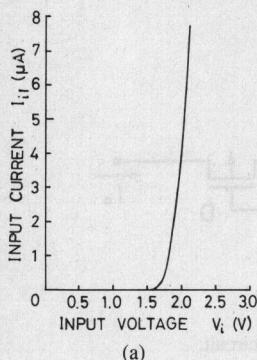


Fig. 5. Characteristics of the fabricated basic logic cell. (a) Input characteristics. (b)  $V_D$  -  $I_D$  characteristics. (c) Input-output characteristics of the current mirror composing the basic logic cell. (d) Input-output characteristics.

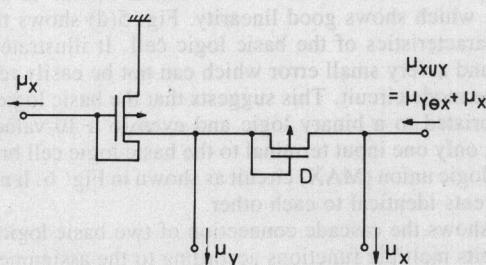


Fig. 6. Union (MAX) circuit.

absolute-difference circuit and the basic logic cell implements the equivalence circuit as shown in Fig. 10. Figs. 11 and 12 show microphotographs of the absolute-difference circuit and the equivalence circuit, respectively.

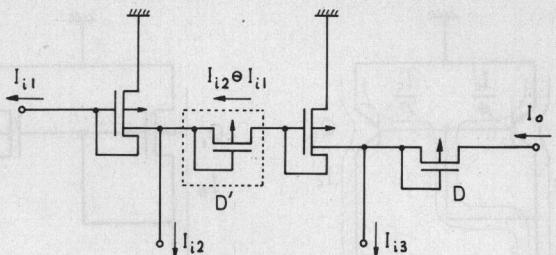


Fig. 7. Cascade connection of basic logic cells. The diode  $D'$  can be omitted.

TABLE II  
FUNCTIONS OF THE CASCADE-CONNECTED BASIC LOGIC CELLS

functions	Input			Output
	$I_{i1}$	$I_{i2}$	$I_{i3}$	
Bounded-Sum	$\mu_X + \mu_Y$	1	1	$\mu_X \oplus Y = 1 \ominus [1 \ominus (\mu_X + \mu_Y)]$
Intersection	$\mu_Y$	$\mu_X$	$\mu_X$	$\mu_X \wedge Y = \mu_X \ominus (\mu_X \ominus \mu_Y)$
Implication	$\mu_Y$	$\mu_X$	1	$\mu_X \rightarrow Y = 1 \ominus (\mu_X \ominus \mu_Y)$

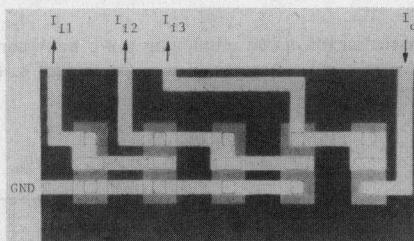


Fig. 8. Microphotograph of the cascade-connected cells.

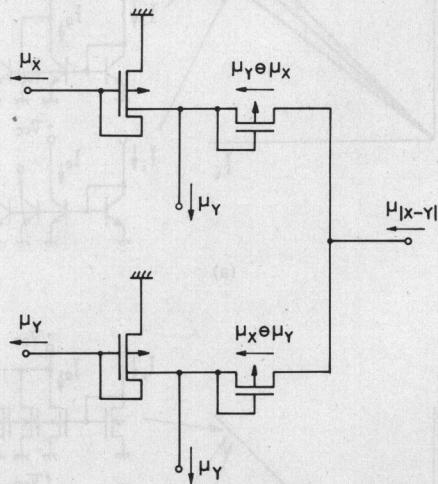


Fig. 9. Absolute-difference circuit.

Among the basic fuzzy logic function circuits described above, the fuzzy logic union (MAX), bounded sum, fuzzy logic intersection (MIN), absolute-difference, and equivalence circuits are in need of one or two current sources which supplies two input currents identical to each other. In the large-scale fuzzy information processing hardware systems, much more identical current sources should be disposed. Moreover, in the current mode circuit systems, every circuit must have some output terminals, the number of which is identical to that of the following circuits to be driven. Therefore, the circuit which supplies many identical currents is necessary. This is the multiple-fanout circuit which is made up of a single-output p

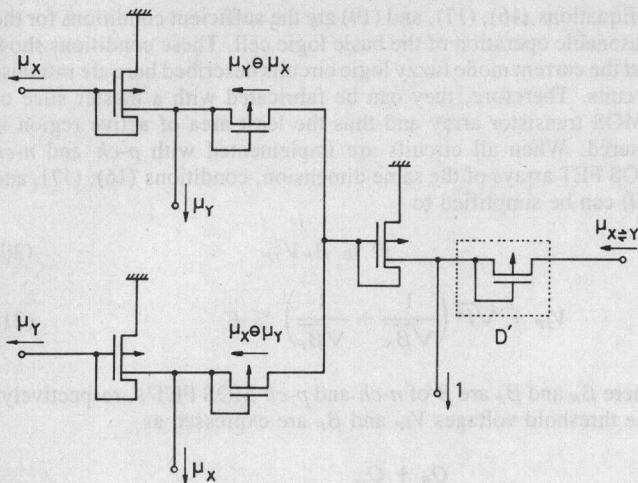


Fig. 10. Equivalence circuit.

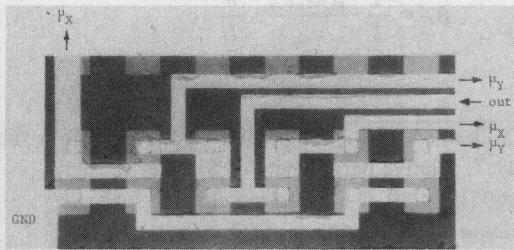


Fig. 11. Microphotograph of the absolute-difference circuit.

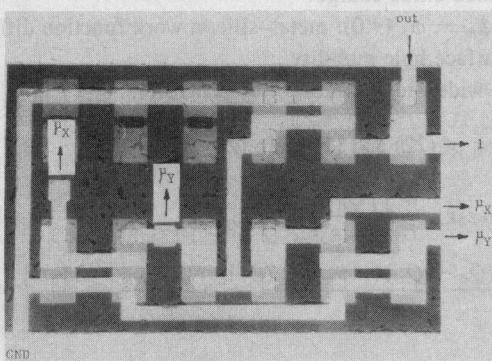


Fig. 12. Microphotograph of the equivalence circuit.

MOS current mirror and a multiple-output n MOS current mirror as shown in Fig. 13. This circuit produces many identical currents from one input current, and thus allows a single-fanout circuit to drive many following circuits. The single-output p MOS current mirror can be extracted from the basic logic cell and thus the multiple-output n MOS current mirror is the basic circuit as well as the basic logic cell, which are essentially necessary for the fuzzy information processing hardware systems.

Accordingly, a master slice, which includes the basic logic cell and multiple-output n MOS current mirror arrays, can be adapted to the arbitrary fuzzy logic semicustom IC's.

#### IV. DESIGN CRITERIA

The sufficient conditions for reasonable operation of the basic logic cell are obtained in the following on the assumption that the short-channel effect is negligible. Fig. 14(a) shows the typical configuration of the basic logic cell driven by two current sources  $Q_1$  and  $Q_2$ .  $Q_4$  is the input portion of the next stage, which acts as the diode in the basic logic cell as described above.

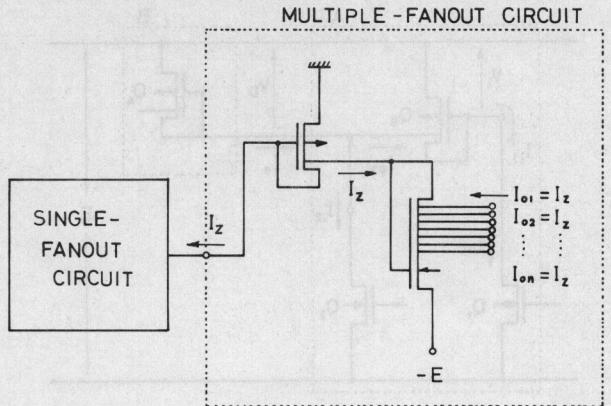


Fig. 13. Multiple-fanout circuit.

The output characteristics  $V_D - I_o$  of circuit A and the input characteristics  $V_D - I_o$  of circuit B are concurrently illustrated in Fig. 14(b), naming each curve A and B, respectively. Curve C represents the drain characteristics of  $Q_2$ , and the curve D the locus of the saturation drain voltage of  $Q_3$ , below which the drain current  $I_{D3}$  is smaller than  $I_{n1}$ .  $V_D$  and  $I_o$  in Fig. 14(a) are obtained from the cross point p in Fig. 14(b). The reasonable output current  $I_o$  (13) of the basic logic cell can be obtained only if the cross point p is on the flat portion of the curve A. Thus, the following conditions are obtained:

$$\sqrt{\frac{I_{n1}}{\beta_3}} \leq V_{TP} \quad (14)$$

$$V_{TP} + \sqrt{\frac{I_o}{\beta_4}} \leq E - \sqrt{\frac{I_{n2}}{\beta_2}} \quad (15)$$

where  $\beta_2, \beta_3, \beta_4: \beta$  of MOS FET's  $Q_2, Q_3, Q_4$ , respectively.

$\beta$	$= \frac{1}{2} \cdot \frac{\mu \epsilon_o \epsilon_{ox}}{t_{ox}} \cdot \frac{W}{L}$ .
$\mu$	= surface carrier mobility.
$\epsilon_o$	$= 8.86 \times 10^{-14}$ F/cm, permittivity of free space.
$\epsilon_{ox}$	$= 3.9$ , relative permittivity of gate oxide.
$t_{ox}$	= thickness of gate oxide.
$W, L$	= width and length of channel.
$V_{TP}$	= threshold voltage of an enhancement mode p-ch MOS FET (absolute value)
$E$	= supply voltage.

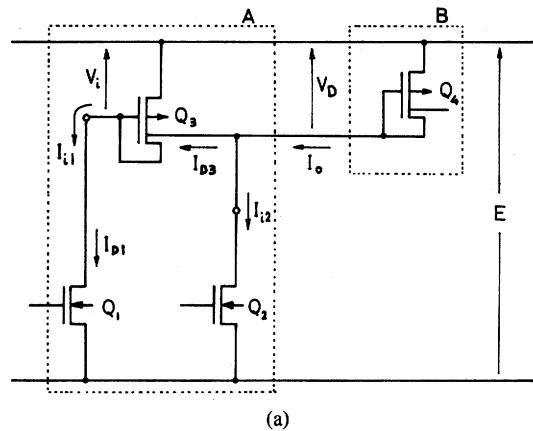
The conditions for the reasonable operation within the range of  $0 \leq I_{n1}, I_{n2} \leq I^*$  is obtained by substituting  $I_{n1} = I_{n2} = I_o = I^*$  to (14) and (15) as

$$I^* \leq \beta_3 V_{TP}^2 \quad (16)$$

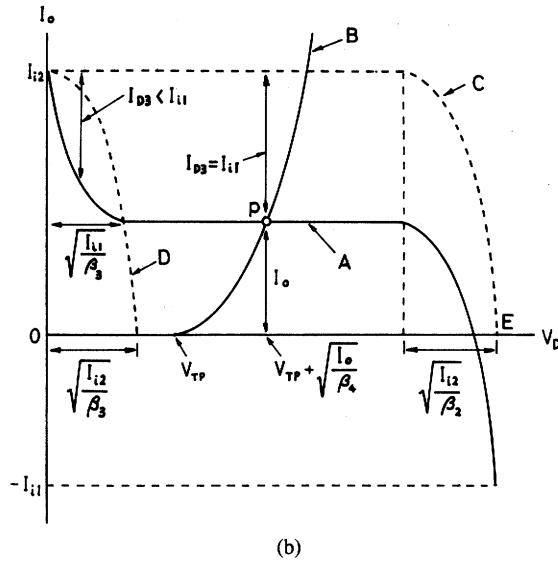
$$V_{TP} + \sqrt{I^*} \left( \frac{1}{\sqrt{\beta_2}} + \frac{1}{\sqrt{\beta_4}} \right) \leq E \quad (17)$$

where  $I^*$  represents the maximum current corresponding to the fuzzy truth value (or grade) of 1.0.

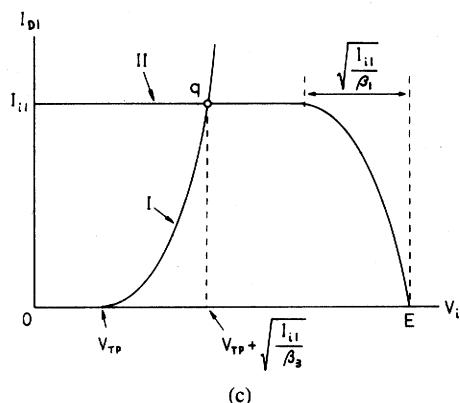
Moreover, the basic logic cell should be properly driven by the current source  $Q_1$ . Fig. 14(c) shows the  $V_i - I_{D1}$  characteristics where curves I and II illustrate the input characteristics of  $Q_3$  and the drain characteristics of  $Q_1$ , respectively. The cross point q gives the input current and voltage of the basic logic cell.  $Q_1$  can supply an input current of nominal value  $I_{n1}$  only if the cross point q is on the flat portion of the curve II in Fig. 14(c). Thus the following condition is obtained.



(a)



(b)



(c)

Fig. 14. (a) Typical configuration of the basic logic cell for design criteria. (b)  $V_D - I_o$  characteristics of the circuits A and B to get the operating point p. (c) The input characteristics of  $Q_3$  (curve I) and the drain characteristics of  $Q_1$  (curve II) to get the operating point q.

$$V_{TP} + \sqrt{\frac{I_{ii}}{\beta_3}} \leq E - \sqrt{\frac{I_{ii}}{\beta_1}} \quad (18)$$

where  $\beta_1$  is  $\beta$  of  $Q_1$ .

The condition for  $Q_1$  to drive  $Q_3$  properly within the range of  $0 \leq I_{ii} \leq I^*$  is obtained by substituting  $I_{ii} = I^*$  in (18) as follows:

$$V_{TP} + \sqrt{I^*} \left( \frac{1}{\sqrt{\beta_1}} + \frac{1}{\sqrt{\beta_3}} \right) \leq E. \quad (19)$$

Equations (16), (17), and (19) are the sufficient conditions for the reasonable operation of the basic logic cell. These conditions show that the current mode fuzzy logic circuits described here are ratioless circuits. Therefore, they can be fabricated with a master slice of CMOS transistor array and thus the least area of active region is assured. When all circuits are implemented with  $p$ -ch and  $n$ -ch MOS FET arrays of the same dimension, conditions (16), (17), and (19) can be simplified to

$$I^* \leq \beta_P V_{TP}^2 \quad (20)$$

$$V_{TP} + \sqrt{I^*} \left( \frac{1}{\sqrt{\beta_N}} + \frac{1}{\sqrt{\beta_P}} \right) \leq E \quad (21)$$

where  $\beta_N$  and  $\beta_P$  are  $\beta$  of  $n$ -ch and  $p$ -ch MOS FET's, respectively. The threshold voltages  $V_{TP}$  and  $\beta_P$  are expressed as

$$V_{TP} = \frac{Q_B + Q_{ss}}{\epsilon_o \epsilon_{ox}} t_{ox} + (-\phi_{MS} + 2\phi_F) \quad (22)$$

$$\beta_P = \frac{1}{2} \cdot \frac{\mu_P \epsilon_o \epsilon_{ox}}{t_{ox}} \cdot \frac{W}{L} \quad (23)$$

where

$$Q_B = \sqrt{2 \epsilon_o \epsilon_{Si} q N_D (2\phi_F)}, \text{ depletion-layer charge in n substrate.}$$

$$\epsilon_{Si} = 11.7, \text{ relative permittivity of Si.}$$

$$q = 1.60218 \times 10^{-19} \text{ C, electron charge.}$$

$$N_D = \text{donor concentration in n substrate.}$$

$$\phi_F (>0 \text{ for } p\text{-ch}): \text{potential difference between the Fermi level and the intrinsic level.}$$

$$Q_{ss} = \text{fixed oxide charge.}$$

$$\phi_{MS} = \phi_M - \phi_S (<0): \text{metal-silicon work function difference.}$$

$$\mu_P = \text{surface hole mobility.}$$

$$W/L = \text{width-length ratio of all transistors.}$$

Substitution of (22) and (23) into (20) gives

$$I^* \leq \frac{1}{2} \mu_P \epsilon_o \epsilon_{ox} \frac{W}{L} \left\{ \left( \frac{Q_B + Q_{ss}}{\epsilon_o \epsilon_{ox}} \right)^2 t_{ox} + \frac{2(Q_B + Q_{ss})(-\phi_{MS} + 2\phi_F)}{\epsilon_o t_{ox}} + \frac{(-\phi_{MS} + 2\phi_F)^2}{t_{ox}} \right\} = f(t_{ox}). \quad (24)$$

When

$$t_{ox} = \frac{\epsilon_o \epsilon_{ox} (-\phi_{MS} + 2\phi_F)}{Q_B + Q_{ss}} \quad (25)$$

the function  $f(t_{ox})$  exhibits the minimum value

$$f(t_{ox})|_{\min} = 2\mu_P (Q_B + Q_{ss})(-\phi_{MS} + 2\phi_F) \frac{W}{L}. \quad (26)$$

Substituting (26) into (24), we can get the following condition:

$$I^* \leq 2\mu_P (Q_B + Q_{ss})(-\phi_{MS} + 2\phi_F) \frac{W}{L}. \quad (20')$$

It is interesting that this condition is independent of the gate oxide thickness  $t_{ox}$ .

Accordingly, the sufficient conditions for the reasonable operation of the basic logic cell and its derivatives composed with the  $p$ -ch and  $n$ -ch transistor array are found to be

$$\left\{ \begin{array}{l} I^* \leq 2\mu_p(Q_B + Q_{ss})(-\phi_{MS} + 2\phi_F) \frac{W}{L} \\ V_{TP} + \sqrt{I^*} \left( \frac{1}{\sqrt{\beta_N}} + \frac{1}{\sqrt{\beta_P}} \right) \leq E \end{array} \right. \quad (20')$$

$$(21)$$

In order to design whole systems, the following condition, which is obtained by the condition of a multiple-fanout circuit, should be added to two conditions (20') and (21).

$$V_{TN} + \sqrt{I^*} \left( \frac{1}{\sqrt{\beta_N}} + \frac{1}{\sqrt{\beta_P}} \right) \leq E \quad (27)$$

where  $V_{TN}$  is the threshold voltage of an enhancement mode  $n$ -ch MOS FET (absolute value).

## V. CONCLUSION

Nine basic fuzzy logic functions are all expressed only with the bounded difference and the algebraic sum. The algebraic sum is implemented only by wiring in the current mode circuits. Thus, the bounded-difference circuit is regarded as a basic logic cell.

Any complicated fuzzy hardware systems made up of nine basic fuzzy logic functions can be realized with only one kind of master slice including the bounded-difference (basic logic cell) and multiple-output n MOS current mirror array.

CMOS fuzzy logic semicustom IC presented here exhibits the following distinctive features. 1) The effect of the variation in  $V_{TH}$  and  $g_m$  on the electrical characteristics of the hardware systems can be cut off by adjusting the supply voltage to the appropriate value. Thus, the expensive ion implanter is not needed. 2) The basic logic cell exhibits good linearity which can not be easily achieved in voltage mode. 3) Since it does not need resistors nor isolation, it is suitable for a large scale fuzzy hardware system. 4) Circuits presented here can be appropriated to a binary logic and even to a 10-valued logic. 5) It exhibits the advantage over fuzzy information processing by using binary circuits, which arises from the ability to provide much more "functions per unit area." 6) It presents a low cost and a short term of design and fabrication.

Nine basic fuzzy logic function circuits presented here will be indispensable for a "fuzzy computer" in the near future.

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## Ternary Scan Design for VLSI Testability

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**Abstract** — In this correspondence, a new scheme is proposed in which ternary clocking signals are used to replace binary clocking signals in VLSI scan-testing designs. This scheme has the same advantage of high testability as the binary scan method [1], but it eliminates the mode-selecting signal line. Since this mode-selecting line must be routed to each flip-flop in the binary scan scheme, the saving is significant in reducing the circuit interconnection complexity and chip area. This correspondence describes the new ternary scheme in detail, and also suggests appropriate circuit designs using CMOS technology. Furthermore, comparisons are made between ternary scan and binary scan [3] and between ternary scan and a scan scheme using binary with a local decoder [2].

**Index Terms** — Multivalued signaling, scan design, ternary logic, testability, VLSI.

## I. INTRODUCTION

Testability is a very important aspect of VLSI design. This is because the test problem becomes more and more difficult as circuit complexity increases. The testability problem is further compounded if its consideration is left until too late a stage of the design process. Among many testability design techniques proposed, the scan method [1] is a well-known and effective one. In this method, the circuit is designed to have two operating modes, namely the normal mode and the scan mode. In the scan mode, all flip-flops in the circuit are connected to form one or more shift registers so that the states of each flip-flop can be preset and tested using a serial scanning process. By virtue of the scan mode the testability of the circuit is greatly enhanced.

One disadvantage of the scan method is the requirement of an additional mode-selecting input which must be routed to every flip-flop in the circuit. This increases the control-connection complexity

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