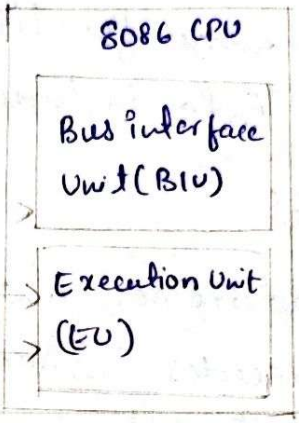
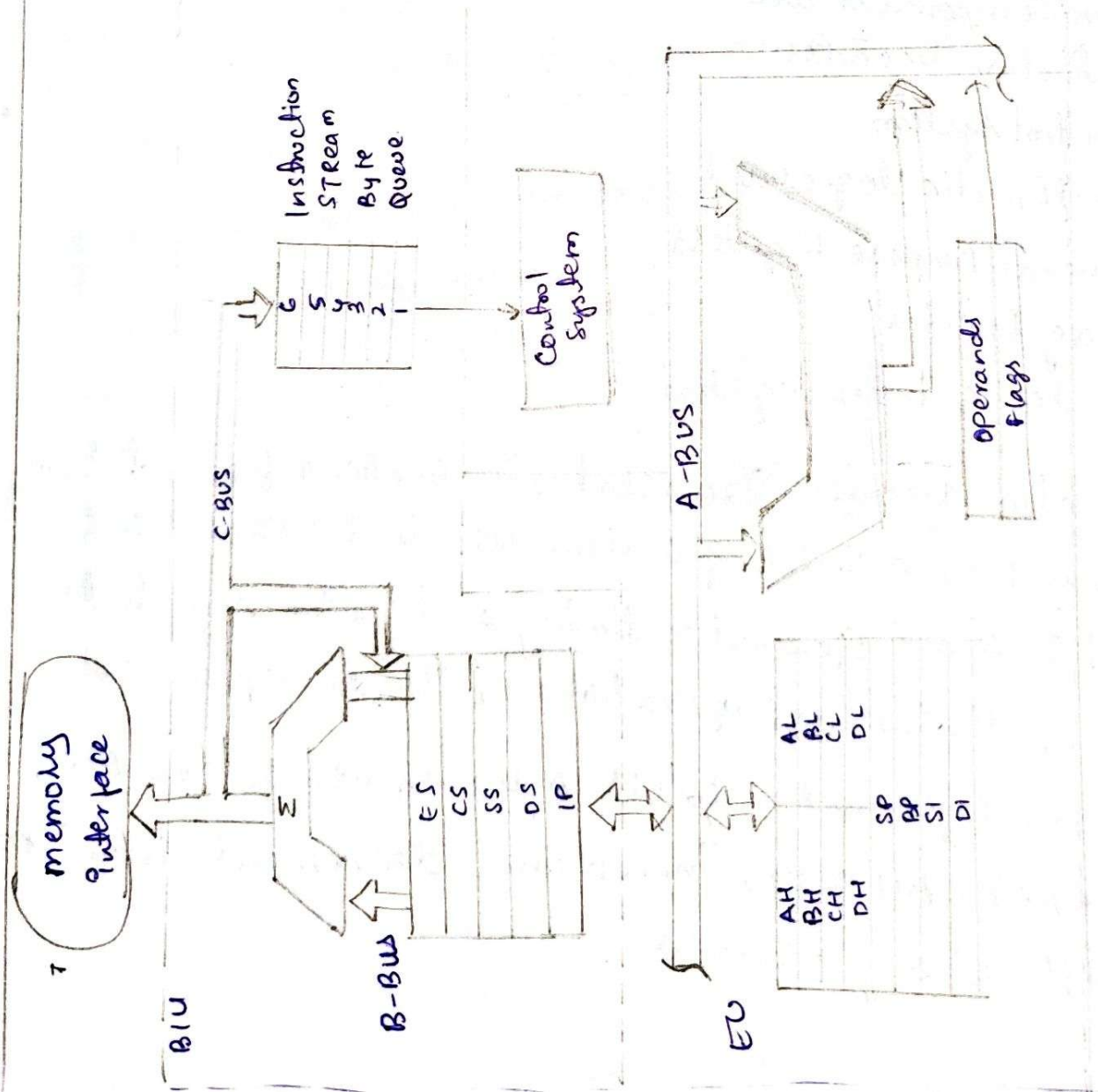
UNIT-1

1) Describe the architecture of 8086 Microprocessor with neat diagram.

Ans Architecture Diagram of 8086

* 8086 employs parallel processing
* 8086 CPU have two parts which operate at the same time
  - Bus interface Unit
  - Execution Unit
* CPU functions.
  1. Fetch
  2. Decode
  3. Execute





Bus interface unit

* Main components are
  - Instruction Queue
  - Segment Registers
  - Instruction pointer.

BIU
- Sends out addresses for memory locations
- Fetches instructions from memory
- Reads/writes data to memory
- Sends out addresses for I/O ports
- Reads/writes data to Input / Output ports

Execution unit

- Tells BIU (addresses) where to fetch instructions or data
- Decodes & Executes instructions
- Main components are
  - Instruction Decoder
  - Control System
  - Arithmetic logic unit
  - General Purpose Registers
    - Flag Register
    - pointer & Index registers.

Instruction Decoder: Translates instructions fetched from memory into a series of actions which EU carries out

Control System :- Generates timing and control signals to perform the internal operations of the microprocessor.

Arithmetic logic unit : 16 bit ALU ~~with~~ which can ADD, SUBTRACT, AND, OR, increment, decrement, complement or shift binary numbers

→ General Purpose Register:- To store temporary data

→ Flag Register:- Flags tell about the status of the processor after any arithmetic or logic operations.

→ Pointer and Index Register:- The pointers will always store some address or memory location. They usually store the offset through which the actual address is calculated.

2 Define Addressing mode and explain about different types of Addressing modes of 8086 microprocessor.

Ans Addressing modes in 8086 microprocessor.

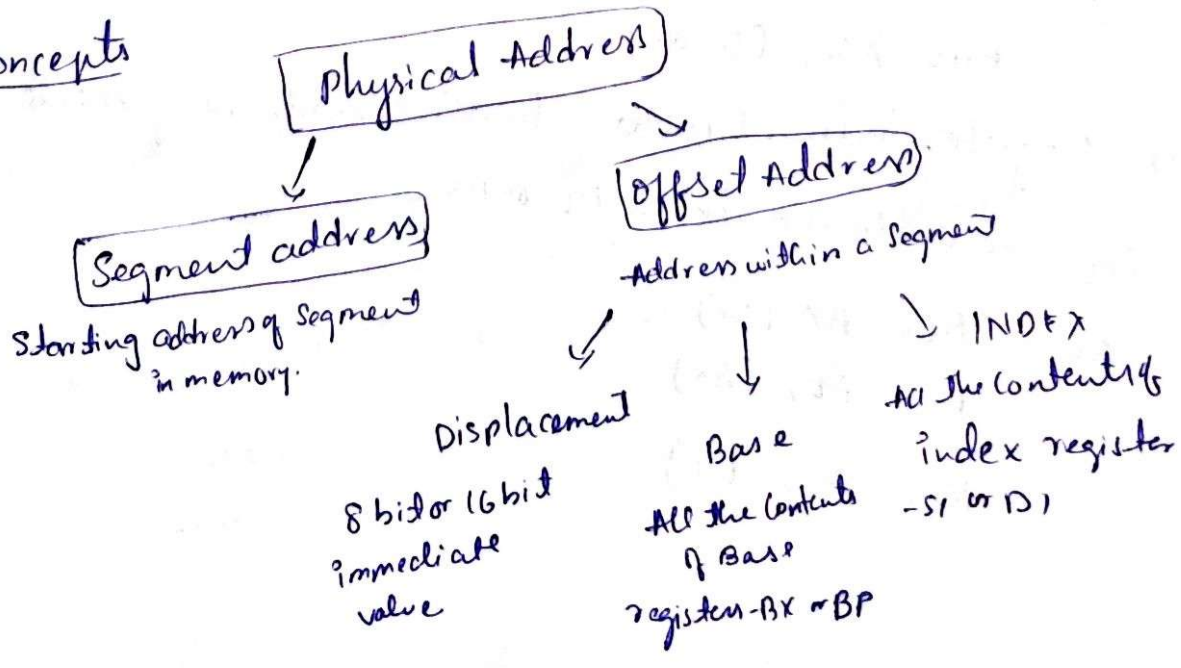
- The way of specifying data to be operated by an instruction is known as addressing modes.
- This specifies that the given data is an immediate data or an address.
- It also specifies whether the given operand is register or register pair.

eg. MOV AL, BL eg. MOV AX, [SI]

eg. MOV DX. [BX + SI]

eg MOV DX 1000H

Few concepts



Types of Addressing Modes

1. Register mode - In this type of addressing mode both the operands are registers

Example : MOV AX, BX
XOR AX, DX
ADD AL, BL

2. Immediate mode - In this type of addressing mode the source operand is a 8 bit or 16 bit data. Destination operand can never be immediate data.

Ex:- MOV AX, 2000
MOV CL, 0A
ADD AL, 45
AND AX, 0000

Note that to initialize the value of segment register an register is required

MOV AX, 2000 MOV CS, AX

3. Displacement or direct mode - In this type of addressing mode the effective address is directly given in the instruction as displacement.

Ex: MOV AX, [DISP]
MOV AX, [0500]

4. Register indirect mode :- In this addressing mode the effective address is in SI, DI or BX.

Ex: MOV AX, [DI]
ADD AL, [BX]
MOV AX, [SI]

5. Based indexed mode :- In this the effective address is sum of base register and index register.

- Base register : BX, BP index register : SI, DI The Physical memory address is calculated according to the base register.

Example:

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MOV AL, [BP+SI]
MOV AX, [BX+DI]
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6. Indexed mode :- In this type of addressing mode the effective address is sum of index register and displacement

Example: MOV AX, [SI + 2000]
MOV AL, [DI + 3000]

7. Based mode - In this the effective address is the sum of base register and displace-ment.

Example: MOV AL, [BP + 0100]

8. Based indexed displacement mode: In this type of addressing mode the effective address is the sum of index register, base register and displacement.

Example: MOV AL, [SI + BP + 2000]

9. String mode - This addressing mode is the related to string instructions. In this value of SI and DI are auto incremented and decremented depending upon the value of directional flag

Example: MOVS B
MOVS W

10. Relative mode: In this the effective address is calculated with reference to instruction pointer.

Example: JNZ 8 bit address

IP = IP+8 bit address.

3 Explain the memory Segmentation in 8086 microprocessor and ~~micro~~ memory Organization of 8051 microcontroller.

Ans Memory Segmentation in 8086 microprocessor

⇒ 8086 has a 20-bit address bus

⇒ So it can address a maximum of 1MB of memory

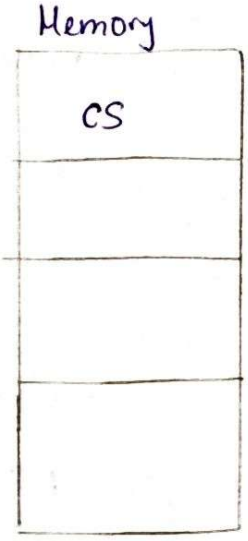
⇒ 8086 can work with only four 64KB Segments at a time within this 1MB range

⇒ These four memory segments are called

- Code Segment
- Stack Segment
- Data Segment
- Extra Segment

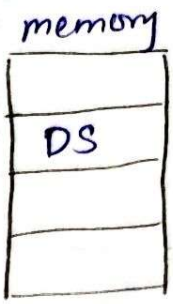
Code Segment register (CS):

Used for addressing memory location in the code segment of the memory. where the executable program is stored.



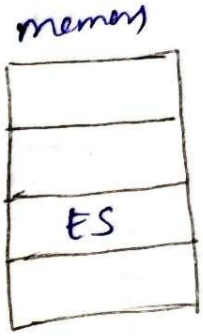
Data Segment register (DS):

Points to the data Segment of the memory where the data is Stored



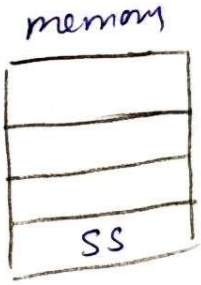
Extra Segment Register [ES]:

Also refers to a Segment in the memory which is another data Segment in the memory



Stack Segment Register (SS):

Is used for addressing stack Segment of the memory. The stack Segment is that segment of memory which is used to store stack data.



Example:

0000 0110 1110 1111 0000 Segment, 16 bits, shifted 4 bits left (or multiplied by 0x10)

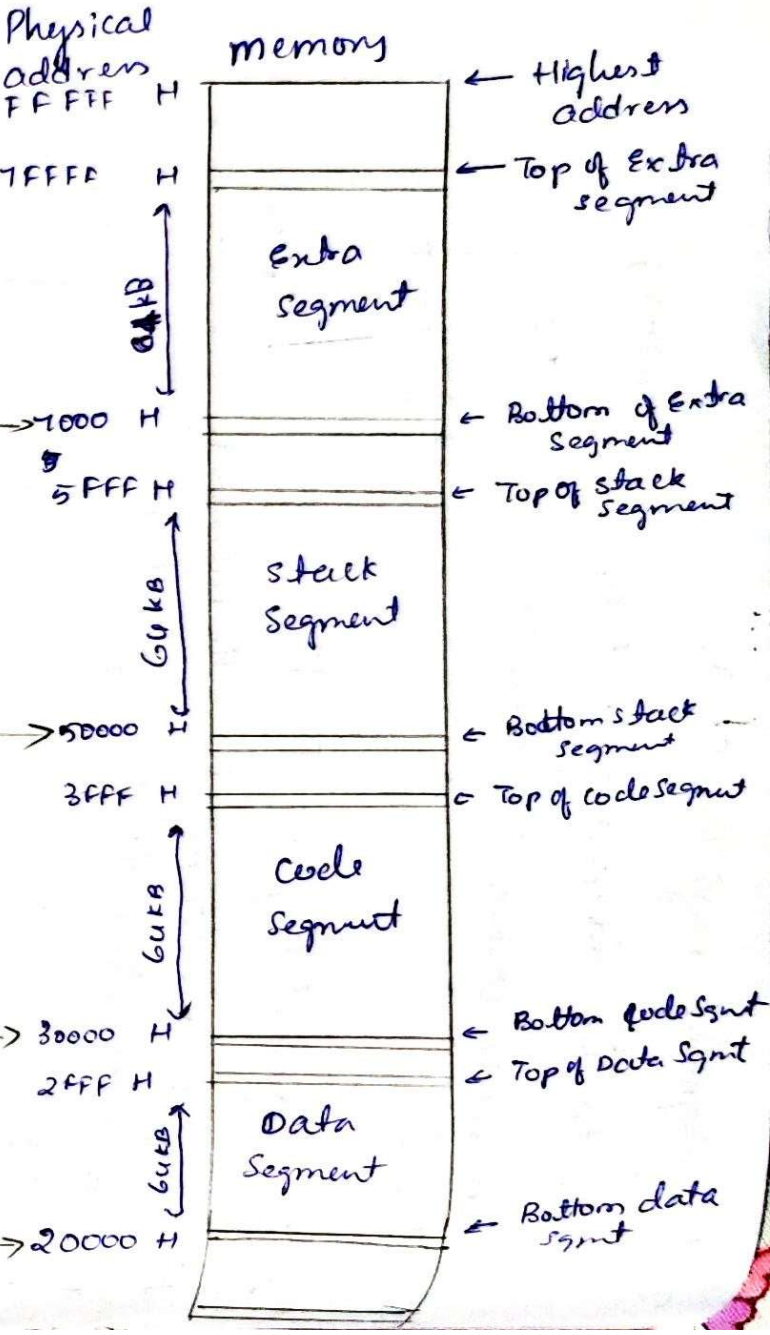
\+ 0001 0010 0011 0100 Offset, 16 bits

0000 1000 0001 0010 0100 Address, 20 bits

Four Segment registers
In BIU

ES	7	0	0	0
CS	3	0	0	0
SS	5	0	0	0
DS	2	6	6	6

Segment registers hold the upper 16 bits of the starting addresses of four memory segments that 8086 is working with at any particular time



8051 memory organization:

The 8051 has two memory spaces.

- Program memory
- Data memory
- The program memory is read only memory
- The data memory is read - write memory.

8051 MC program memory.

- 8051 has 64KB of program memory
- In ROM/EPROM versions of 8051 lower 4K (0000H - 0FFFH) provided internally, 60K (1000H - FFFFH) provided externally
- After reset the CPU begin the execution from address 0000H of the program memory.
- In ROM/EPROM versions EA pin is used, when it is connected to VCC it access the internal address 0000 to 0FFF (internal ROM)

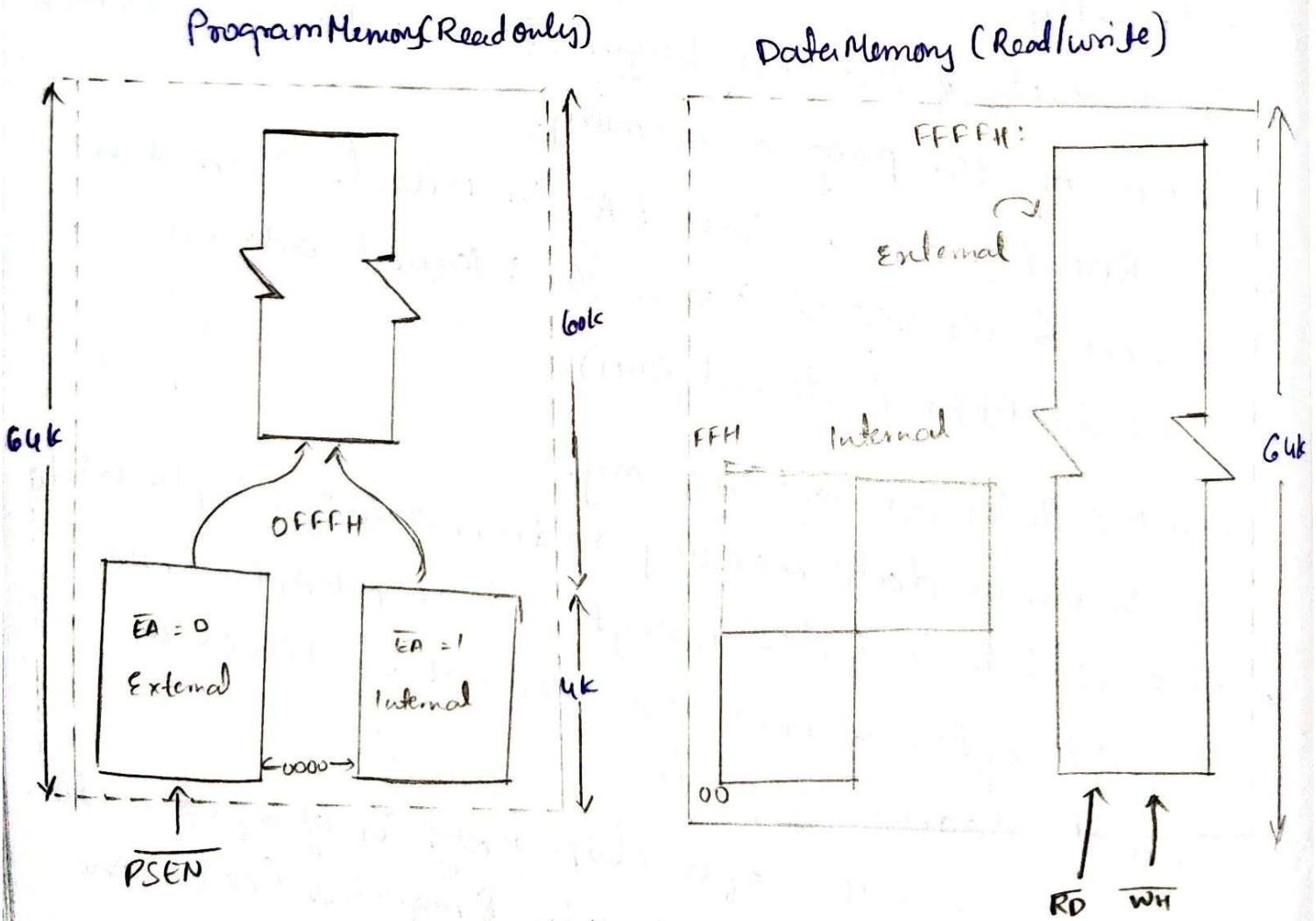
8051 MC internal Data memory.

- The internal data memory address are one byte wide
- The which includes 128 bytes on chip RAM + SFRs.
- The 128 bytes of RAM can accessed by direct or indirect addrening mode
- The lower 32 bytes of on chip RAM is grouped in to 4 Banks. Each bank contain 8 registers (each one 8-bit wide)
- By using PSW we can select which register is in use

8051 Mc External Data memory

- There can be upto 64kB of data memory external to the Clip
- Depending upon the addressing mode the address of memory 1 or 2 bytes wide
- MOVX instruction can be used to access the external data memory.
- External data memory and program memory may be Combined by enabling both RD' and PEN' signals

8051 memory Organization.



4. Describe the Architecture of 8051 Microcontroller with neat diagram.

Components of 8051

1. Bus Control
   - Data Bus: 8 bit data bus for carrying data
   - Address Bus: 16 bit address bus used to carry address
2. Four (8 bit each) general purpose parallel I/O ports:
   - PORT0: when no external memory is connected it acts as general-purpose I/O port
   - If external memory applied then it acts as multiplexed add and data bus.
   - Can operate in dual mode
   - PORT1: Normal I/O port
   - PORT2: Same as port0
   - PORT3: Dedicated I/O port
3. Timers and Counters: Used for synchronization of clock Circuits in the internal operation by XTAL1 and XTAL2
   - 4 additional pins are:
   - EA (External Enable)
   - PSEN (Program Store enable)
   - ALE (Address latch enable)
   - RST (Reset)
4. Memory:
   - ROM - A program of 4k memory can be stored
   - RAM - 128 bytes Internal RAM divided into 32 working registers. Each register has 4 register bank of 8 registers each

5. Serial port - for communication.

- SBUF: Serial port data buffer holds the data
- SCON: Serial control for managing communication.
- PCON: parallel control manages data transfer rates.
- RXD and TXD
- 4 programmable modes

⇒ Serial data mode 0 (shift register mode)

⇒ Serial data mode 1 (Standard UART)

⇒ Serial data mode 3

6 Interrupt control (Software or hardware)

- 5 sources are present
- 2 external interrupt sources connected through INT0 and INT1
- 3 external interrupt sources through serial port interrupt, timer & flag 0, and timer flag 1

7 CPU: 8051 system bus connects all the support devices to CPU.

Port 2 Drivers

Port 0 Drivers

⑤ Distinguish between Microprocessor and microcontroller.

Microcontroller	Microprocessors.
1. CPU is stand-alone, RAM, ROM I/O, timer are separate	1. CPU, RAM, ROM, I/O and timer are all on a single chip.
2. Designer can decide on the amount of ROM, RAM and I/O Ports	2. Fixed amount of on-chip ROM, RAM, I/O ports
3. Microprocessor based system requires More hardware	3. Microcontroller system requires less hardware
4. General-purpose Device	4. Single Special purpose Device
5. Microprocessor based System is more flexible	5. Microcontroller based System is not flexible
6. Access time for memory and I/O is more	6. Access time for memory and I/O is less
7. It has many Instructions to move data between memory and CPU	7. It has less instructions to move data between memory and CPU.