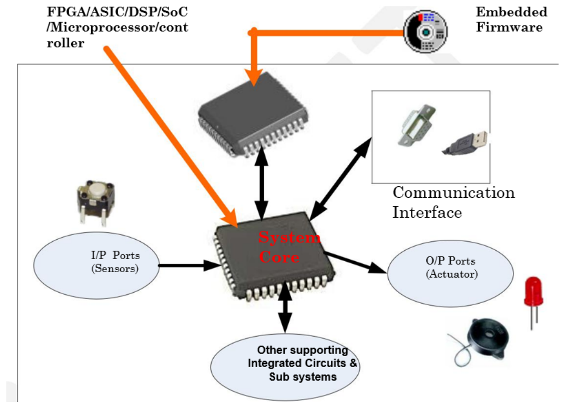
ES Unit-3 Imp QnA

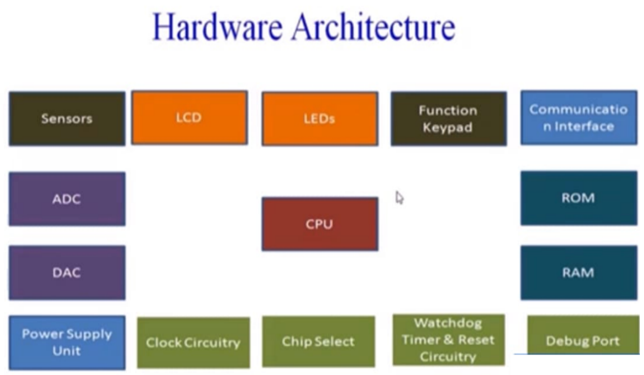
1. Draw the block diagram of typical embedded system & explain in detail about Core of the Embedded System.

A)

EMBEDDED SYSTEM BLOCK DIAGRAM

1. An embedded system is a combination of Hardware and Software and it is supposed to do one specific task only
2. A typical embedded system contains a single chip controller which acts as the master brain of the system.
3. Embedded systems are basically designed to regulate a physical variable or to manipulate the state of some devices by sending some signals to the actuators or devices connected to the output port system in response to the input signal provided by the end users or sensors which are connected to the input ports.
4. Examples of common user interface input devices are
    a. Keyboards
    b. push button,
    c. switches, etc..
5. Examples for common user interface output devices are
   ➢ LEDs,
   ➢ LCDs,
   ➢ Piezoelectric buzzers etc…
6. The requirement of type of user interface changes from application to application based on domain





THE CORE OF THE EMBEDDED SYSTEMS

The core of the embedded system falls into any one of the following categories:

1. General Purpose and Domain Specific Processors
    a. Microprocessor
        i. A silicon chip representing a Central Processing Unit (CPU), which is capable of performing arithmetic as well as logical operations according to a pre-defined set of Instructions, which is specific to the manufacturer
        ii. In general the CPU contains the Arithmetic and Logic Unit (ALU), Control Unit and Working registers
        iii. Microprocessor is a dependant unit and it requires the combination of other hardware like Memory, Timer Unit, and Interrupt Controller etc for proper functioning.

iv. Intel claims the credit for developing the first Microprocessor unit Intel 4004, a 4 bit processor which was released in Nov 1971

v. DEVELOPERS MICROPROCESSOR
   ➢ Intel – Intel 4004 – November 1971(4-bit)
   ➢ Intel – Intel 4040.
   ➢ Intel – Intel 8008 – April 1972.
   ➢ Intel – Intel 8080 – April 1974(8-bit).
   ➢ Motorola – Motorola 6800.
   ➢ Intel – Intel 8085 – 1976.
   ➢ Zilog - Z80 – July 1976

b. MICROCONTROLLER:

i. A highly integrated silicon chip containing a CPU, scratch pad RAM, Special and General purpose Register Arrays, On Chip ROM/FLASH memory for program storage, Timer and Interrupt control units and dedicated I/O ports

ii. Microcontroller can be general purpose (like Intel 8051, designed for generic applications and domains) or application specific (Like Automotive AVR from Atmel Corporation. Designed specifically for automotive applications)

iii. Since a microcontroller contains all the necessary functional blocks for independent working, they found greater place in the embedded domain in place of microprocessors

iv. Microcontrollers are cheap, cost effective and are readily available in the market

v. Texas Instruments TMS 1000 is considered as the world’s first microcontroller

2. Digital Signal Processors

a. Powerful special purpose 8/16/32 bit microprocessors designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications

b. Digital Signal Processors are 2 to 3 times faster than the general purpose microprocessors in signal processing applications

c. DSPs implement algorithms in hardware which speeds up the execution whereas general purpose processors implement the algorithm in firmware and the speed of execution depends primarily on the clock for the processors

d. DSP can be viewed as a microchip designed for performing high speed computational operations for ‘addition’, ‘subtraction’, ‘multiplication’, and ‘division’

e. A typical Digital Signal Processor incorporates the following key units

    i. Program Memory

    ii. Data Memory

    iii. Computational Engine

    iv. I/O Unit

f. Audio video signal processing, telecommunication and multimedia applications are typical examples where DSP is employed

3. Application Specific Integrated Circuits (ASICs)

    a. A microchip designed to perform a specific or unique application.

    b. It is used as replacement to conventional general purpose logic chips.

    c. ASIC integrates several functions into a single chip and thereby reduces the system development cost

    d. Most of the ASICs are proprietary products.

e. As a single chip, ASIC consumes very small area in the total system and thereby helps in the design of smaller systems with high capabilities or functionalities.

f. ASICs can be pre-fabricated for a special application or it can be custom fabricated by using the components from a re-usable “building block" library of components for a particular customer application.

4. Programmable Logic Devices (PLDs):

   a. These offer customers a wide range of logic capacity, features, speed, and voltage characteristics - and these devices can be re-configured to perform any number of functions at any time

   b. Designers can use inexpensive software tools to quickly develop, simulate, and test their logic designs in PLD based design. The design can be quickly programmed into a device, and immediately tested in a live circuit

   c. PLDs are based on re-writable memory technology and the device is reprogrammed to change the design

   d. FIELD PROGRAMMABLE GATE ARRAYS (FPGAS):

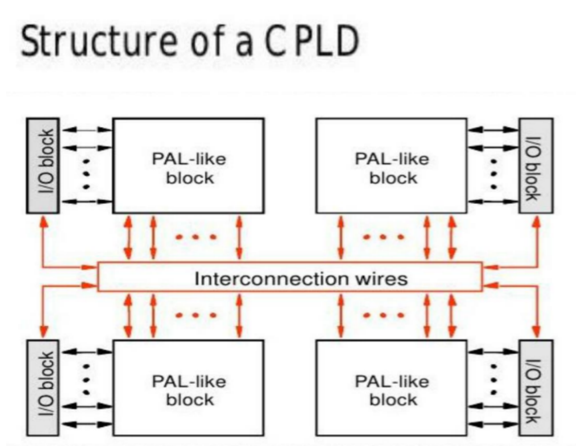
      i. FPGA is an IC designed to be configured by a designer after manufacturing.
      ➢ FPGAs offer the highest amount of logic density, the most features, and the highest performance.
      ➢ Logic gate is Medium to high density ranging from 1K to 500K system gates
      ➢ These advanced FPGA devices also offer features such as built-in hardwired processors, substantial amounts of memory, clock management systems, and support for many of the latest, very fast device-to-device signaling technologies.
      ➢ FPGAs are used in a wide variety of applications ranging

from data processing and storage, to instrumentation, telecommunications, and digital signal processing

e. COMPLEX PROGRAMMABLE LOGIC DEVICES (CPLDS)

   i. ➢ A complex programmable logic device (CPLD) is a programmable logic device with complexity between that of PALs and FPGAs, and architectural features of both.
   ➢ CPLDs, by contrast, offer much smaller amounts of logic - up to about 10,000 gates.
   ➢ CPLDs offer very predictable timing characteristics and are therefore ideal for critical control applications
   ➢ CPLDs such as the Xilinx CoolRunner series also require extremely low amounts of power and are very inexpensive, making them ideal for cost-sensitive, battery-operated, portable applications such as mobile phones and digital handheld assistants.

   ii.



f. ADVANTAGES OF PLDS:

   i. ➢ PLDs offer customer much more flexibility during design cycle
   ➢ PLDSs do not require long lead times for prototype or production-the PLDs are already on a distributor's self and ready for shipment.

➢ PLDs do not require customers to pay for large NRE costs and purchase expensive mask sets
➢ PLDs allow customers to order just the number of parts required when they need them. allowing them to control inventory.
➢ PLDs are reprogrammable even after a piece of equipment is shipped to a customer.
➢ The manufacturers able to add new features or upgrade the PLD based products that are in the field by uploading new programming file

5. Commercial off the shelf Components (COTS)

   a. ➢ A Commercial off-the-shelf (COTS) product is one which is used “as-is"
   ➢ COTS products are designed in such a way to provide easy integration and interoperability with existing system components
   ➢ A COTS component in turn contains a General Purpose Processor (GPP) or Application Specific Instruction Set
   Processor (ASIP) or Application Specific Integrated Chip (ASIC)/Application Specific Standard Product (ASSP) or Programmable Logic Device (PLD)

2. What are Sensors and Actuators and explain the Role of Sensor and Actuators in the Embedded Systems

A)

SENSORS & ACTUATORS

- Embedded system is in constant interaction with the real world
- Controlling/monitoring functions executed by the embedded system is achieved in accordance with the changes happening to the Real World.
- The changes in the environment or variables are detected by the sensors connected to the input port of the embedded system.
- If the embedded system is designed for any controlling purpose, the system will produce some changes in controlling variable to bring the controlled variable to the desired value.

- It is achieved through an actuator connected to the out port of the embedded system.

SENSOR:

- A transducer device which converts energy from one form to another for any measurement or control purpose.
- Sensors acts as input device.

Examples:

1. IR Sensor(Obstacle Detection)
2. Humidity(measures moisture) .
3. PIR -passive infra red(detects motion)
4. Ultrasonic (measures the distance)
5. Piezoelectric (measure changes in pressure)
6. Smoke sensor (detecting that fire)

ACTUATOR:

- A form of transducer device (mechanical or electrical) which converts signals to corresponding physical action (motion).
- Actuator acts as an output device.

Examples:

1. Printer
2. LED/LCD Display units
3. Speakers
4. Head Phone
5. Webcam

3. Explain about a) SPI Bus communication interface b) RS232C

A) a)

SERIAL PERIPHERAL INTERFACE (SPI) BUS

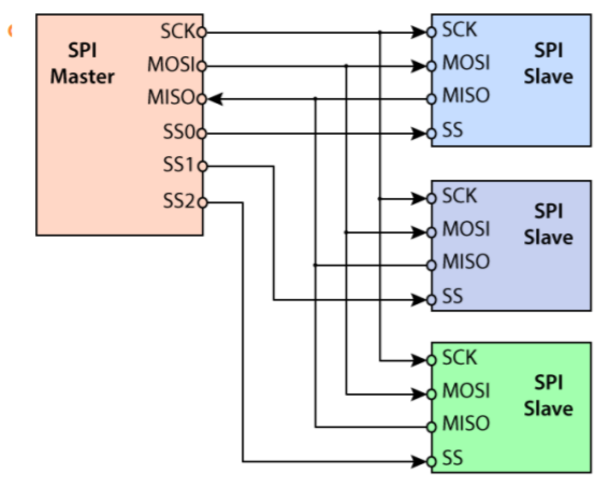
- The Serial Peripheral Interface Bus (SPI) is a synchronous bi-directional full duplex four wire serial interface bus.
- The concept of SPI is introduced by Motorola
- SPI is a single master multi-slave system.
- It is possible to have a system where more than one SPI device can be master, provided the condition only one master device is active at any given point of time, is satisfied.
- SPI is used to send data between Microcontrollers and small peripherals such as shift registers, sensors, and SD cards.
- SPI requires four signal lines for communication. They are:
    - Master Out Slave In (MOSI): Signal line carrying the data from master to slave device. It is also known as Slave Input/Slave Data In (SI/SDI).
    - Master In Slave Out (MISO): Signal line carrying the data from slave to master device. It is also known as Slave Output (SO/SDO)
    - Serial Clock (SCLK): Signal line carrying the clock signals
    - Slave Select (SS): Signal line for slave device select.
    - It is an active low signal.
- The master device is responsible for generating the clock signal.
- Master device selects the required slave device by asserting the corresponding slave device's slave select signal "LOW".
- The data out line (MISO) of all the slave devices when not selected floats at high impedance state
- The serial data transmission through SPI Bus is fullyconfigurable.
- SPI devices contain certain set of registers for holding these configurations.
- The Serial Peripheral Control Register holds the various configuration parameters like master/slave selection for the device, baudrate selection for communication, clock signal control etc.

- The status register holds the status of various conditions for transmission and reception.
- SPI works on the principle of "Shift Register".
- The master and slave devices contain a special shift register for the data to transmitter receive.
- The size of the shift register is device dependent.
- Normally it is a multiple of 8

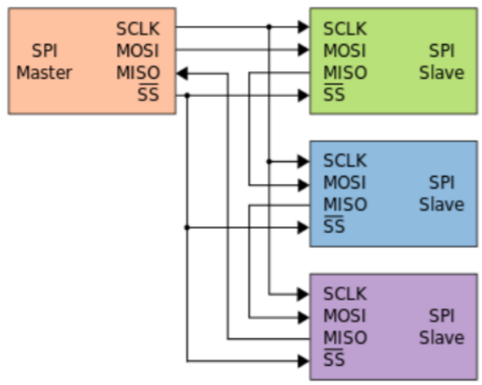
SPI BASIC ARCHITECTURE

- It has two configurations:
  1. Independent slave
  2. Daisy Chain

1. INDEPENDENT SLAVE CONFIGURATION



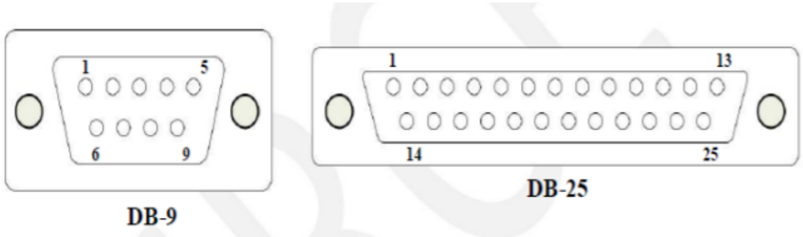
2. DAISY CHAIN



b)

RS-232C:

- RS-232 C (Recommended Standard number 232, revision C from the Electronic Industry Association) is a legacy, full duplex, wired, asynchronous serial communication interface
- RS-232 extends the UART communication signals for external data communication.
- UART uses the standard TTL/CMOS logic (Logic „High" corresponds to bit value 1 and Logic "LOW" corresponds to bit value 0) for bit transmission whereas RS232 use the EIA standard for bit transmission.
- As per EIA standard, a logic "0" is represented with voltage between +3 and +25V and a logic "1" is represented with voltage between -3 and-25V.
- In EIA standard, logic "0" is known as "Space" and logic "1" as "Mark".
- The RS232 interface define various handshaking and control signals for communication apart from the „Transmit" and „Receive" signal lines for data communication.
- RS-232 supports two different types of connectors, namely; DB-9: 9-Pin connector and DB-25: 25-Pin connector.



- RS-232 is a point-to-point communication interface and the devices involved in RS-232 communication are called „Data Terminal Equipment (DTE)‟ and „Data Communication Equipment(DCE)‟
- If no data flow control is required, only TXD and RXD signal lines and ground line (GND) are required for data transmission and reception.
- The RXD pin of DCE should be connected to the TXD pin of DTE and vice versa for proper data.
- If hardware data flow control is required for serial transmission, various control signal lines of the RS-232 connection are used appropriately.
- The control signals are implemented mainly for modem communication and some of them may be irrelevant for other type of devices
- The Request To Send (RTS) and Clear To Send (CTS) signals co-ordinate the communication between DTE and DCE.
- Whenever the DTE has a data to send, it activates the RTS line and if the DCE is ready to accept the data, it activates the CTS line
- The Data Terminal Ready (DTR) signal is activated by DTE when it is ready to accept data.
- The Data Set Ready (DSR) is activated by DCE when it is ready for establishing a communication link.
- DTR should be in the activated state before the activation of DSR
- The Data Carrier Detect (DCD) is used by the DCE to indicate the DTE that a good signal is being received
- Ring Indicator (RI) is a modem specific signal line for indicating an incoming call on the telephone line.

- As per the EIA standard RS-232 C supports baudrates up to 20Kbps (Upper limit19.2Kbps)
- The commonly used baudrates by devices are 300bps, 1200bps,2400bps, 9600bps, 11.52Kbps and19.2Kbps
- The maximum operating distance supported in RS-232 communication is 50 feet at the highest supported baud rate.
- Embedded devices contain a UART for serial communication and they generate signal levels conforming to TTL/CMOS logic.
- A level translator IC like MAX 232 from Maxim Dallas semiconductor is used for converting the signal lines from the UART to RS-232 signal lines for communication.
- On the receiving side the received data is converted back to digital logic level by a converter IC.
- Converter chips contain converters for both transmitter and receiver
- RS-232 uses single ended data transfer and supports only point-to-point communication and not suitable for multi-drop communication

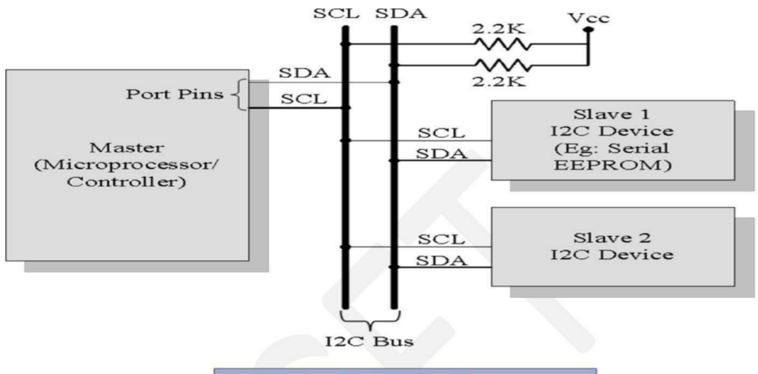
4. Explain about a) I2C (Inter Integrated Circuit) Bus communication interface b) Wi-Fi?

A) a)

I2C (Inter Integrated Circuit)Bus:

- Inter Integrated Circuit Bus (I2C - Pronounced „I square C‟) is a synchronous bidirectional half duplex (one-directional communication at a given point of time) two wire serial interface bus.
- The concept of I2C bus was developed by "Philips Semiconductors" in the early 1980s.
- The original intention of I2C was to provide an easy way of connection between a microprocessor/microcontroller system and the peripheral chips in Television sets.
- The I2C bus is comprised of two bus lines, namely; Serial Clock – SCL and Serial Data –SDA.

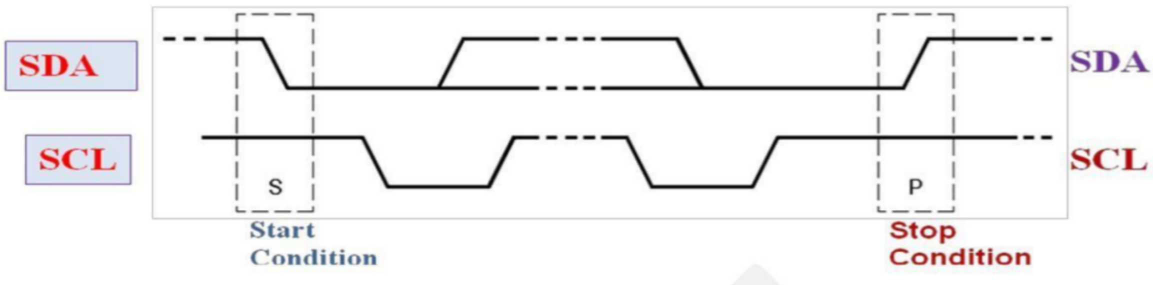
- SCL line is responsible for generating synchronization clock pulses and SDA is responsible for transmitting the serial data across devices.
- I2C bus is a shared bus system to which many number of I2C devices can be connected.
- Devices connected to the I2C bus can act as either "Master" device or "Slave" device
- The ‘Master’ device is responsible for controlling the communication by initiating/terminating data transfer, sending data and generating necessary synchronization clock pulses.
- ‘Slave’ devices wait for the commands from the master and respond upon receiving the commands.
- ‘Master’ and ‘Slave’ devices can act as either transmitter or receiver.
- Regardless whether a master is acting as transmitter or receiver, the synchronization clock signal is generated by the ‘Master’ device only.
- I2C supports multi masters on the same bus



I2C Bus Interfacing

I2C BUS OPERATION:

- Master device pulls the clock line (SCL) of the bus to "HIGH"
- Master device pulls the data line (SDA) „LOW", when the SCL line is at logic "HIGH" (This is the „Start" condition for data transfer)



- Master sends the address (7 bit or 10 bit wide) of the ‘Slave’ device to which it wants to communicate, over the SDA line.
- Clock pulses are generated at the SCL line for synchronizing the bit reception by the slave device.
- The MSB of the data is always transmitted first.
- The data in the bus is valid during the „HIGH" period of the clocksignal
- In normal data transfer, the data line only changes state when the clock is low.
- Master waits for the acknowledgement bit from the slave device whose address is sent on the bus along with the Read/Write operation command.
- Slave devices connected to the bus compares the address received with the address assigned to them
- The Slave device with the address requested by the master device responds by sending an acknowledge bit (Bit value =1) over the SDA line
- Upon receiving the acknowledge bit, master sends the 8bit data to the slave device over SDA line, if the requested operation is „Write to device".
- If the requested operation is ‘Read from device’, the slave device sends data to the master over the SDA line.
- Master waits for the acknowledgement bit from the device upon byte transfer complete for a write operation and sends an acknowledge bit to the slave device for a read operation
- Master terminates the transfer by pulling the SDA line ‘HIGH’ when the clock line SCL is at logic ‘HIGH’ (Indicating the ‘STOP’ condition).

5. Discuss about the following Communication Interfaces a) Bluetooth b) ZigBee

A) a)

BLUETOOTH:

Bluetooth is a wireless technology standard for short distances (using short-wavelength UHF band from 2.4 to 2.485 GHz)for exchanging data over radio waves in the ISM and mobile devices, and building personal area networks(PANs).Invented by telecom vendor Ericsson in 1994, it was originally conceived as a wireless alternative to RS- 232 data cables.

Bluetooth uses a radio technology called frequency- hopping spread spectrum. Bluetooth divides transmitted data into packets, and transmits each packet on one of 79 designated Bluetooth channels. Each channel has a bandwidth of 1 MHz. It usually performs 800 hops per second, with Adaptive Frequency-Hopping (AFH)enabled

Originally, Gaussian frequency-shift keying (GFSK) modulation was the only modulation scheme available. Since the introduction of Bluetooth 2.0+EDR, π/4-DQPSK(Differential Quadrature Phase Shift Keying) and 8DPSK modulation may also be used between compatible devices. Bluetooth is a packet-based protocol with a master- slave structure. One master may communicate with up to seven slaves in a piconet. All devices share the master's clock. Packet exchange is based on the basic clock, defined by the master, which ticks at312.5 µs intervals.

A master BR/EDR Bluetooth device can communicate with a maximum of seven devices in a piconet (an ad-hoc computer network using Bluetooth technology), though not all devices reach this maximum. The devices can switch roles, by agreement, and the slave can become the master (for example, a headset initiating a connection to a phone necessarily begins as master—
as initiator of the connection—but may subsequently operate as slave).

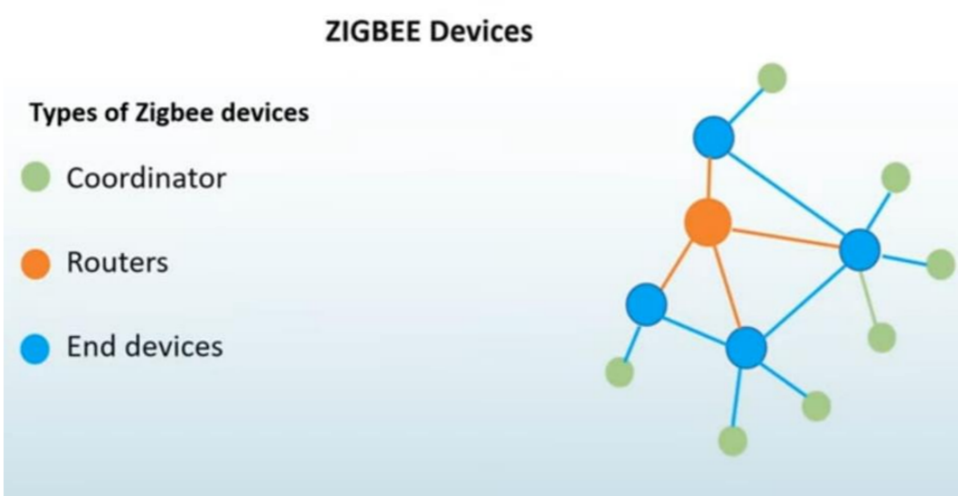
b)

ZIGBEE:

Zigbee is an IEEE 802.15.4-based specification for a suite of high- level communication protocols used to create personal area networks with small, low-power digital radios, such as for home automation, medical device data collection, and other low-power low-bandwidth needs, designed for small scale projects which need wireless connection. Hence, zigbee is a low-power, low data rate, and close proximity(i.e., personal area) wireless ad hoc network

The technology defined by the zigbee specification is intended to be simpler and less expensive than other wireless personal are a networks (WPANs), such as Bluetooth or Wi-Fi .Applications include wireless light switches, electrical meters with in-home-displays, traffic management systems, and other consumer and industrial equipment that require short-range lowrate wireless data transfer.

Its low power consumption limits transmission distances to 10– 100 meters line-of-sight, depending on power output and environmental characteristics. Zigbee devices can transmit data over long distances by passing data through a mesh network of intermediate devices to reach more distant ones.



Zigbee Coordinator: The zigbee coordinator acts as the root of the zigbee network. The ZC is responsible for initiating the Zigbee network and it has the capability to store information about the network.

Zigbee Router: Responsible for passing information from device to another device or to another ZR.

Zigbee end device: End device containing zigbee functionality for data communication. It can talk only with a ZR or ZC and doesn't have the capability to act as a mediator for transferring data from one device to another.

Zigbee supports an operating distance of up to 100 meters at a data rate of 20 to 250 Kbps