VPR Assessment of a Novel Partitioning Algorithm

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Abstract

Field Programmable Gate Array (FPGA) systems would be well suited to space based applications except for their vulnerability to space based radiation. Various techniques for dealing with their susceptibility have been discussed in literature. This thesis aims to implement and assess a key part of a theoretical technique to protect against radiation induced Single Event Upsets (SEUs) and assess the overheads of said technique.

Contents

VPR	Versatile Place and Route
MCNC	Microelectronics Centre of North Carolina
BLE	Basic Logic Element
CLB	Configurable Logic Block
DFG	Directed Flow Graphor a DataFlow Graph
DAG	Directed Acyclic Graph
SEU	Single Event Upset
LUT	Look Up Table
VTR	Verilog To Routing
STL	Standard Template Library
FPGA	Field Programmable Gate Array
TMR	Triple Modular Redundancy
BLIF	Berkeley Logic Interchange Format
ASIC	Application Specific Integrated Circuit
LAB	Logic Array Block
I/O	Input/Output
ICAP	Internal Configuration Access Port
SRAM	Static RAM
mux	Multiplexer
CAD	Computer Aided Design
MBU	Multi Bit Upset
NRE	Non Recurring Engineering
DICE	Dual Interlock Storage Cell
VHDL	VSIC Hardware Description Language
SAT	Boolean Satisfiability Problem

Chapter 1

Introduction

1.1 Overview

Space plays an increasingly important role in the functioning of modern societies, being vital for fields including navigation, meteorology, and communications [17]. Field Programmable Gate Array systems (FPGAs) have many beneficial features, such as their flexibility and low Non Recurring Engineering (NRE) costs which make them highly desirable for space based applications. Unfortunately they have far greater susceptibility to space radiation. Hardened Field Programmable Gate Arrays (FPGAs) offer only a fraction of the gate counts (and hence capability of implementing large or complex circuits) of non hardened offerings prompting a search for a solution to the radiation susceptibility of FPGAs using mainstream hardware [16], one of the most popular of which is Triple Modular Redundancy (TMR). In TMR, vulnerable components are triplicated allowing for errors to be detected and mitigated. This thesis is based on the work of [8] which introduces an approach to TMR, and aims to implement a key part of the approach and assess the implementation with the aid of an open source Computer Aided Design (CAD) toolchain for FPGAs. The remainder of this chapter provides an overview of these technologies, discusses alternatives to our approach, and details why we have chosen the technique we have. Chapter 2 introduces our approach to benchmarking circuits, and presents our initial results along with a brief discussion; Chapter 3 describes our implementation and design choices made in the implementation and Chapter 4 outlines our schedule and current progress, and our final chapter presents our closing remarks.

FPGAs

Field Programmable Gate Arrays (FPGAs) are popular devices capable of implementing a wide variety of circuits. Unlike Application Specific Integrated Circuits (ASICs) which must be specially designed and manufactured for an application—a lengthy and expensive process—FPGAs are a generic off the shelf device which can be mass produced by manufacturers and then adapted for an individual user's needs. Their flexibility, low cost, and faster development time make them the most economic for a number of applications.

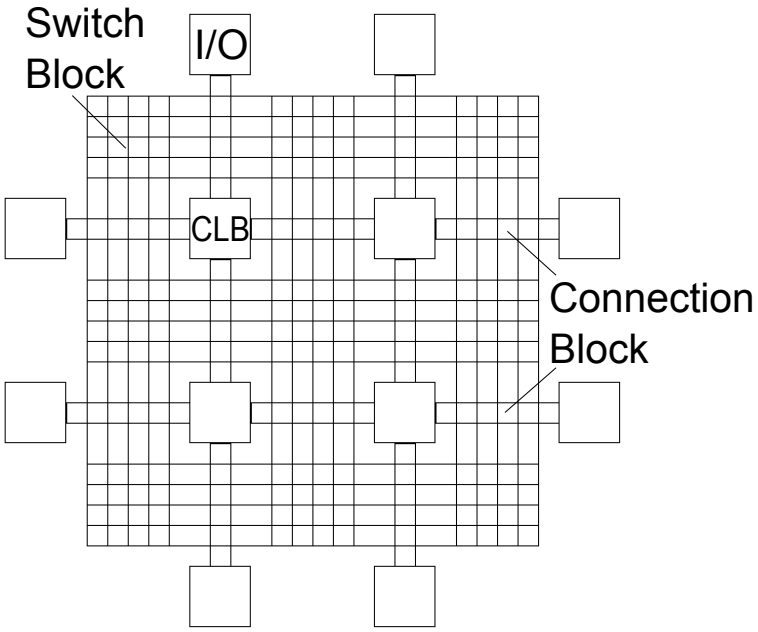

Figure 1.1: Island Style FPGA

TODO: Use own image. Wilton lecture notes have no license/copyright notice/etc attached, so don't know if this usage is actually allowed. Plus, doesn't look that good.

There are three main components to an FPGA: Input/Output (I/O) blocks, usually around the edge, allowing for input and output from the FPGA, Configurable Logic Blocks (CLBs) containing all the logic elements or *primitives*, and the routing between all the components. Most FPGAs also contain other structures embedded in the CLB array to provide commonly used resources such as multipliers. While they can be implemented using latches and Look Up Tables (LUTs), embedding them as discrete components allows for denser designs. The routing between components consists of channels running horizontally and vertically with a number of wires and programmable switches connecting the wires to each other and to CLBs allowing for configurable paths between arbitrary components. A typical switch or connection block has a configuration cell storing the state, and a connection can be made or unmade by writing a new value to the cell for that switch. The most common style of routing is known as island style (as the CLBs are located as islands in a sea of routing) with the routing area making up some 80%-90% of the FPGA's area [10]. Each CLB is a cluster of smaller blocks, called Basic Logic Elements (BLEs), with each BLE containing the logic primitives, typically a programmable LUT to implement combinational logic, a latch for register operations and implementing sequential logic, and a Multiplexer (mux) to switch between the two. The values for the LUT, whether the mux is selecting the latch or LUT output, and other component states are all stored in configuration memory like the routing switches and are typically implemented in SRAM.

Programming an FPGA involves loading in a bitstream which describes all the component values

(i.e. contents of the configuration memory for each cell) for a circuit, accomplished through writing the bitstream to a special configuration port on the FPGA. A number of FPGAs also allow for run time programming, or reconfiguration, of parts of a circuit through loading the bitstream for only the section of interest while the rest of the FPGA keeps running.

Check grammar in this next section. There are four main technologies used to implement the configuration memory in FPGAs:

- Static RAM (SRAM), which gives the highest density devices and includes the Virtex-5 family this thesis focuses on however they are volatile and must be reprogrammed every power up from an external configuration memory;
- (anti)fuse, which are only one time programmable;
- flash, which is non-volatile (thus not requiring an external configuration memory) and reprogrammable however has a lower density than SRAM based FPGAs [10].

Partial Reconfiguration

Partial reconfiguration involves loading configuration information for part of a circuit during operation. Much like the complete configuration described above, it involves writing a configuration bitstream to one of the available configuration ports, in this case also including the location to reconfigure. The configuration memory of recent Virtex devices is subdivided into frames, and one can only reconfigure entire frames. A configuration frame is 41 (32-bit) words long on a Virtex-5 device and configures a bit slice of the device that spans 20 CLB rows. As more frames are being reconfigured the larger the bitstream, and consequently the longer the time to reconfigure. The main configuration ports used are the external SelectMAP interface, or the internal Internal Configuration Access Port (ICAP), each with a bandwidth of 400MB/s in all Virtex devices [8, 22]

Space Based Applications

Space is quite different from a terrestrial environment, and FPGAs have a number of advantages due to their lower Non Recurring Engineering (NRE) costs and flexibility. As FPGAs can be reconfigured during a mission, faulty or outdated designs can be replaced remotely; however, there is a significant downside: as systems go further into space and are no longer protected by the earth's atmosphere they become increasingly likely to suffer from radiation induced errors where ionising radiation intersecting with a component causes charge build up, potentially triggering incorrect operation [20]. As outlined in Table 1.1, for higher orbits the mean time to upset is on the order of only a second, and this rate increases as technology advances and chip density further increases. Of the potential effects, which range from unnoticeable to device destruction, this thesis is concerned with mitigating Single Event Upsets (SEUs), where an incorrect signal is triggered but the underlying circuitry is not damaged. We

Orbit	SEUs per device/day	Mean time to upset (s)
LEO (560 km)	4.09	2.11×10^4
Polar (833 km)	1.49×10^4	5.81
GPS (20,200 km)	5.46×10^4	1.58
Geosynchronous (36,000 km)	6.20×10^4	1.39

Table 1.1: SEU Rate Predictions for Virtex-4 devices at various orbits [8]

also concern ourselves primarily with errors affecting only single bits or components rather than Multi Bit Upsets (MBUs) in which multiple components are affected at the same time. Keep in? !

In an ASIC, while SEUs may be picked up and latched or otherwise continue affecting the circuit in future, the component itself continues operating normally.

FPGAs on the other hand are vulnerable to configuration errors as well. When the charged particle impacts configuration memory it can flip the state of that cell changing the actual circuit. Unlike transient errors, these functional errors persist until corrected.

Additionally for SRAM devices, the off-chip configuration memory itself can be affected, so the next time the chip is reprogrammed (e.g. after power cycling), an incorrect circuit configuration will be loaded.

(Anti)fuse devices, being non reprogrammable, are immune to configuration errors, though both SRAM and flash based FPGAs are vulnerable and all three are susceptible to transient SEU [6].

How We Deal With FPGA Downsides

Clearly, in order for FPGAs to be viable in space based systems the effects of SEUs must be mitigated. A number of technologies and techniques are available, each with their own advantages and disadvantages. A number of options exist which detect errors but are unable to determine the correct result, requiring a reload of the configuration memory while the circuit is non operational until the reconfiguration completes. For many applications this downtime is impractical, thus we will be looking at options which allow the circuit to continue operating correctly. There are three main categories of SEU hardening techniques [4]:

- Charge Dissipation, which aims to keep the effect of the radiation below the level where it would have an effect. This includes techniques such as increasing the drive current. These methods typically require custom hardware (increasing costs) and usually increase power usage.

- Temporal Filtering, which aims to filter out transient SEUs, includes methods such as delay-and-vote [4]. These techniques often slow down operation and are ineffective against configuration errors.

- Spatial Redundancy, which uses multiple redundant circuits to detect errors and be able to continue operating. Spatial redundancy techniques include Dual Interlock Storage Cell (DICE) [7] and Triple

	Power (μW)	Speed (ns)	HARDNESS (e/b-d)	AREA (mm^2)
Standard	Rise – 0.7 Fall – 0.2	Rise – 0.21 Fall – 0.27	10^{-8} 1 node	360
Increased Drive Current	Rise – 1.0 Fall – 0.2	Rise – 0.16 Fall – 0.15	2×10^{-9} 1 node	460
TMR	Rise – 1.72 Fall – 1.27	Rise – 0.2 Fall – 0.27	10^{-11} 2 node	1200
DICE	Rise - 1.4 Fall - 1.1	Rise - 0.96 Fall - 0.97	1.6×10^{-10} 2 node	520

Table 1.2: Comparison of hardening techniques [4]

Modular Redundancy (TMR) and can be implemented either in hardware or at the design level not requiring any custom hardware. These methods typically increase area and power usage.

While hardened FPGAs are available, they typically lag well behind mainstream commercial offerings [16], thus solutions which can be implemented on mainstream commercial FPGA hardware are desirable. Additionally, there is very little point hardening an FPGA and not its configuration buffers and memory which take up far more surface area [10] and are thus even more vulnerable. For these reasons TMR, requiring no custom hardware and providing SEU protection against both transient and functional errors, is one of the more popular SEU hardening techniques even though it comes at the cost of more than tripling area and greatly increasing power usage. Table 1.2 details power usage, operating speed, hardness, and required area for flip flops which have been hardened using the techniques listing within the table. Explain columns One additional technique specific to SRAM based FPGAs relates to the protection of the off-chip configuration memory. As SRAM is volatile and loads the state from off chip at power up, this external configuration memory must also be protected from SEUs. This can be accomplished by incorporating error detection and correction techniques in the RAM, something already in place on a number of mainstream FPGAs such as the Virtex-4 and -5 [9].

1.2 Triple Modular Redundancy

Triple Modular Redundancy is a commonly used method for creating fault tolerant systems in which a given circuit is implemented three times with independent components, with the outputs feeding into a voter circuit to determine the majority value. Any SEU will affect the output value of at most one version, so the majority vote is still correct. For transient errors that are not in a feedback loop correcting the output is enough to fix the error; however, SEUs in feedback paths or in the configuration memory will persist, and this require some method for eliminating them. One possible approach is resetting the system but while this occurs the system is unavailable so a reset may not be a feasible solution. Instead, partial

reconfiguration can reconfigure only the faulty circuit while the redundant circuits continue operating and providing output. After reconfiguration the circuit must then be resynchronised to the same state as the other two. We use the approach presented by [8] which involves running the circuit until the state converges, which is guaranteed (for acyclic circuits) to occur within a timeframe given by the number of register stages and the clock frequency. In order for this approach to always resynchronise correctly the circuit must have no feedback loops which may carry incorrect data. To solve this we simply ensure that all feedback loops are *cut*, that is, the value is voted on before being passed back into the circuit. This has the additional benefit of correcting transient errors which would otherwise be caught in a feedback cycle by ensuring the cycle data is correct.

This approach requires three times as many circuit elements (as the circuits are triplicated) plus whatever is required for voters. By minimising the number of voters, we can thus reduce the overhead of our approach.

Once an error occurs it takes up to T_{path} to reach the voter and be detected, where T_{path} is given by the clock period and number of register stages. This is called the *error detection time*. Detection of an error can then be used to trigger reconfiguration. Sending a request to the reconfiguration controller goes through a token ring network consisting of the other voters, and the reconfiguration controller. In the worst case it takes one full cycle of the network to receive the token, one full cycle to reach the reconfiguration controller, and three cycles to transmit the request, giving $5 \times TimePerHop$. Benchmarks of a sample voter indicate 50 clock cycles per hop is a good estimate. *Reconfiguration time* $= T_R$ is dependent upon the circuit size. For a Virtex-5 device, each reconfiguration area consists of 160 LUTs and 160 latches, where only whole reconfiguration areas can be reconfigured. The bitstream size for this area is Fill in which takes $15.4\mu s$ to reconfigure at $100MHz$. Once the error has been detected and the circuit reconfigured it must then be resynchronised with the other partitions, which takes up to T_{path} using the previously described technique. !

The error recovery time consists of the time to detect the error, send a request to the configuration controller, and then reconfigure and resynchronise the circuit, thus is a function of the circuit area, clock frequency, and number of register stages. Therefore it is required that the number of register stages and area are small enough, and frequency large enough, that our error recovery time is within a user specified

limit.

$$
\begin{aligned}
\text{Error Recovery Time} &= \text{Error Detection Time} + \text{Reconfiguration Time} + \text{Resynchronisation Time} \\
\text{Error Detection Time} &<= T_{path} = \text{Clock Period} \times \text{Register Stages} \\
\text{Communication Time} &= \text{Cycles per flit per hop} \times \text{Number of flits} \times \text{NumStops} \times \text{Clock Period} \\
\text{Communication Time} &= 50 \times 5 \times (\text{NumPartitions} + 1) \times \text{Clock Period} \\
\text{Reconfiguration Time} &= \text{Clock Period} \times \frac{\text{Bitstream Size}}{\text{Reconfiguration Speed}} \\
&= \text{Clock Period} \times \left\lceil \frac{\max(numLUTs, numLatches)}{160} \right\rceil \times 1.54 \times 10^{-5} \\
\text{Resynchronisation Time} &<= T_{path} = \text{Clock Period} \times \text{Register Stages}
\end{aligned}
\tag{1.1}
$$

[8]

Additionally, as each voter circuit adds some constant overhead in terms of area, power usage and clock frequency slowdown it is desirable to have each partition as large as possible. This thesis is concerned with implementing and assessing this TMR design; a discussion of other TMR methods and our reasons for not using them is included below.

This method only works when at most one SEU occurs within the error detection and recovery time; should SEUs occur in two of the three partitions then it is impossible for the voter to determine the correct value necessitating a complete reload of the configuration memory (*scrubbing*). Therefore, we require the error detection and recovery time to be sufficiently small that the likelihood of multiple events occurring within that time period are sufficiently small.

Additionally, as mentioned earlier, it is also desirable to minimise the number of voters to reduce the overhead of this approach. To that end, having larger partitions (and hence fewer) is preferable to smaller provided we still stay within our target recovery time.

Triple Modular Redundancy Implementations

This thesis builds on the work of [8] which details a partitioning algorithm that traverses a circuit represented as a Directed Flow Graph (DFG) in a breadth first manner, creating partitions that stay within our constraints. Our goal is to create an algorithm which stays within a user specified error recovery time, doesn't require existing code to be rewritten, allows for both custom voting and reconfiguration logic to be added, can use industry standard FPGAs rather than custom hardware, and effectively protects the entire system from SEUs with as close to no downtime as achievable. Additionally, it is desirable to limit the overhead of implementing TMR through minimising the number of voters required. There are a number of existing TMR solutions, however none quite meet our requirements. Our first requirement is that standard FPGA hardware can be used, with our implementation specifically targeting Virtex-5 chips. Options with custom hardware such as [16] (with three FPGAs and an ASIC voter in a single package), are often

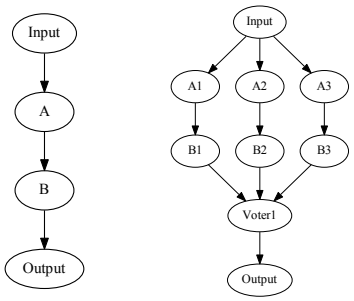

Figure 1.2: DFG before and after partitioning

prohibitively expensive, and prevent us from using our existing boards. Many FPGAs marketed specifically at space based applications are, in addition to featuring specialised hardware, only latchupexplain? immune or only include inbuilt TMR on registers, leaving them still vulnerable to SEUs [12]. Non hardware solutions are typically implemented pre-synthesis, such as [11] (which introduces a VHDL library featuring triplicated components), and require existing code to be rewritten, or during synthesis such as [1] and [2] which support neither specifying an error recovery limit, nor for adding reconfiguration logic. Other options look at using partial TMR (such as [18]) which, while it does reduce the overhead of TMR, means the entire circuit is no longer protected, or have excessive downtimes to recover from errors such as [3], which uses idle cycles in a data path to calculate redundant results. One approach similar to ours is presented by [13] who also partition a post-synthesis netlist (represented by a DFG), but their focus is on evaluating techniques for cutting feedback loops, while we focus on partitioning circuits into smaller sub circuits. Cutting feedback loops is however a part of this thesis, and their work could be incorporated in, although for our current implementation a simple depth first traversal described later was chosen.

Our Algorithm

Given a netlist description of a circuit, it is possible to represent the circuit as a DFG [10]. Our goal is to split a DFG into a number of smaller subgraphs, triplicate the components of each subgraph, and insert voting and recovery logic, with each subgraph having independent components and an error recovery time within our threshold. We can then proceed to implement our graph, made up of our new subgraphs, as normal. To do so we traverse the DFG in a depth first manner, keeping track of the number of register stages, area, and maximum frequency, extending our partition area as we do so, until our recovery time constraint would be violated. As we extend our partition area we must detect any cycles and cut them, joining them back up after the output has been voted on, ensuring that each partitions is acyclic guaranteeing that the circuit will resynchronise and not get incorrect data trapped in a feedback loop. At that point we cleave off our partition and write it to a file, open a new empty partition, and repeat for all circuit

elements. Once this is done, we have a set of subcircuits. We now triplicate each partition and insert our additional voting logic, then join each subcircuit back together.

1.3 CAD Flow

FPGAs are typically programmed in a higher level description language such as VHDL or Verilog, and then a number of programs (collectively making up the Computer Aided Design (CAD) flow or development toolchain) turn the source into a bitstream to program a target FPGA. The design flow process can be split into a number of sub processes as illustrated in Figure 1.3 [5, 10, 15].

1. The synthesiser turns a hardware description language such as VHDL or Verilog into a netlist of basic gates and flip flops.
2. The optimiser removes redundant logic, and attempts to simplify logic.
3. The mapper maps logic elements to primitives, the basic logic elements contained on the FPGA.
4. The packer combines logic elements into CLBs.
5. The placer locates each CLB within the FPGA architecture, deciding which physical block implements which logic block.
6. The router makes the required connections between each element by deciding which switches are on or off. This includes the connections within each CLB (local routing) and in between CLBs (global routing).

For our partitioner we will insert an additional step into the design flow between mapping and packing, which operates directly on a netlist. The additional steps are described more fully in section Reference. !

How VPR Works

For this thesis we will be assessing the results of our algorithm implementation after processing by Versatile Place and Route (VPR), an open source packer, placer and router. VPR was chosen as it is open source allowing modifications to be made if necessary, and it is well documented and popular in research, making it much easier for us to determine what's happening and why, rather than relying on proprietary black box processes from commercial vendors. A brief understanding of the algorithms used in VPR and the effects of different settings is useful, though not critical, for understanding the results. [15] has a more detailed list of all the options VPR takes. Unless otherwise specified, all values are at their defaults.

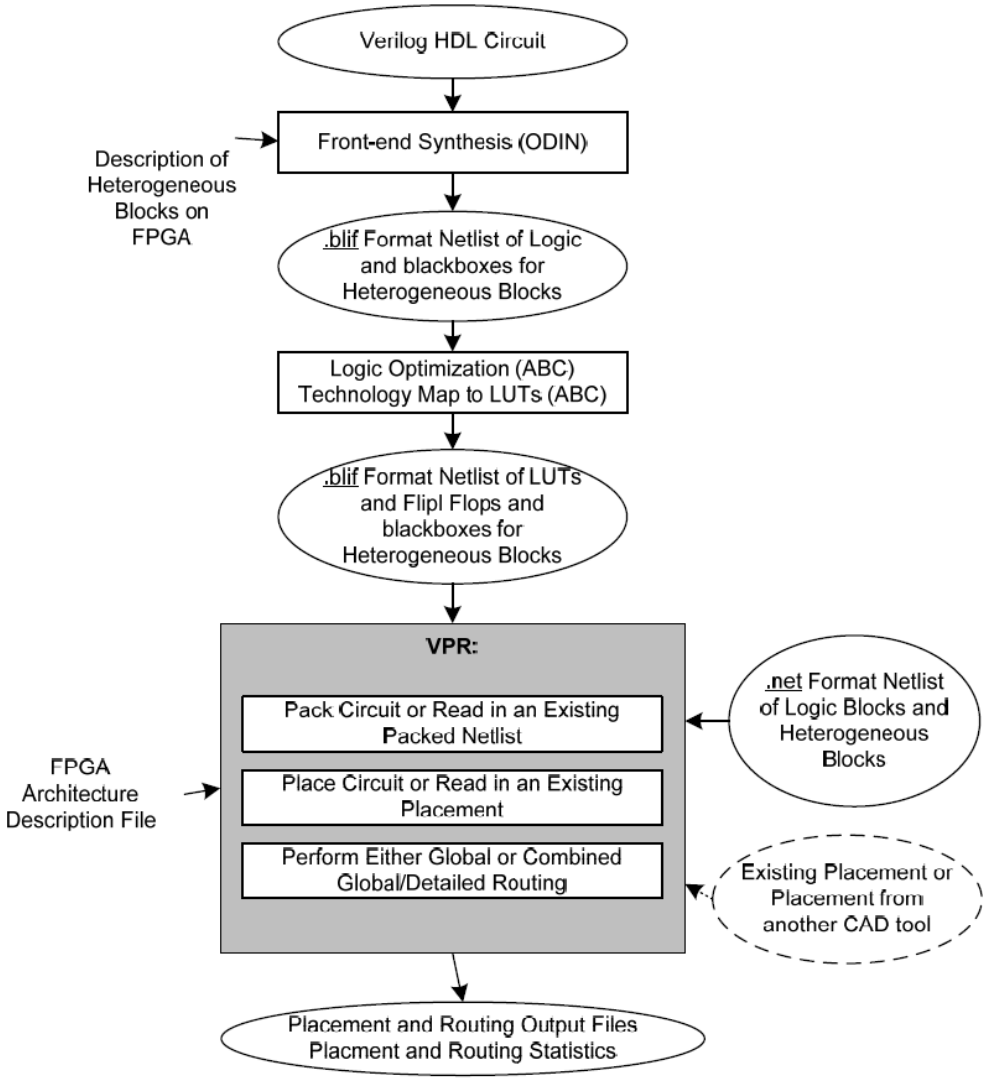

Figure 1.3: Cad Design Flow. [15]

Packer

VPR uses the AAPack algorithm described by [14]. This is a greedy algorithm which operates on blocks sequentially, starting with an FPGA area of 1 block by 1 block. For each block it greedily adds *primitives* (latches or LUTs) based on a configurable cost function until no more primitives can be added. It then repeats for the next block, and the next after that, until every primitive has been packed. As it runs out of blocks in the current FPGA area it expands the FPGA area used until it reaches the physical limit specified in the architecture file (or grows indefinitely if no limit is specified). This means that even if the device is of area 40 by 40, if the packer can fit everything in a 30 by 30 area it will do so, and VPR will treat the FPGA as being only 30 by 30. The cost function can be configured through options passed to VPR, to [15]:

- prioritise optimisation of timing or area (default is prefer timing)

- prioritise absorbing nets with fewer connections over those with more (default is yes)
- when prioritising absorbing nets with fewer connections, focus more on signal sharing or absorbing smaller nets (default is greatly prefer absorbing smaller nets)
- determine the next complex block to pack based on timing or number of inputs (default is timing).

The main thing to note, as relates to our results, is that as much as possible AAPack will never leave blocks partially packed while there is still a primitive which will fit. Even when optimising timing exclusively, it will still attempt to maximally pack each cluster.

Placer

VPR's placer uses a simulated annealing algorithm where the options allow us to specify annealing schedule parameters and cost function. The default options were chosen via experimentation and are likely superior to custom options we may choose to use, and affect the quality of the result rather than materially affecting the behaviour [5, 15]. For these reasons we will be leaving them at their default. Section Reference discusses the variation in results due to the stochastic nature of the placement algorithm. !

Router

VPR's router supports three different algorithms:Awkward phrasing, fix breadth_first, which focuses ! solely on routing a design; timing_driven, the default, which tends to use slightly more tracks (5%) than breadth_first while providing much faster routes (2×–10×) with less CPU time; and directed_search, which like breadth_first is routability driven however uses A* to improve runtime. We will be using the default timing_driven algorithm.TODO: Reason? There are a number of options setting algorithm pa- ! rameters, all of which we will leave at their defaults, though we will be changing the route_chan_width parameter as we collect results. route_chan_width specifies the width of the channels in the architecture. If omitted VPR will perform a binary search on channel capacity to determine the minimum channel width.

Chapter 2

Algorithm

For our partitioner, we operate on a netlist in Berkeley Logic Interchange Format (BLIF) format (described in subsection 2.5 after optimisation and technology mapping, but before packing. Our goal is to take an input netlist and transform it into a netlist in the same format, with the same set of outputs for each set of inputs, but with redundant components.

Figure **??** illustrates a typical CAD toolchain with our custom partitioner added and the substeps expanded (c.f. Figure 1.3 for an example without). The below points are more fully expanded in Subsection 2.2.

- Partition - Take an input circuit and split it into multiple smaller circuits, one per file.
- Triplicate - Take an input circuit and transform it into a TMR'd version.
- Join - Take a set of input files, one circuit per file, and join them into one larger circuit by joining corresponding signals.
- Flatten - Use abc to transform a heirarchical circuit into a format supported by VPR.
- Test - Use the verification abilities of abc to verify that the generated circuit is equivalent to the original.

2.1 Data Structures

Basic Types

The following are the basic types, out of which others are built, and which will be referred to. There is generally, but not always, a direct relationship to a C++ primitive. The following are custom complex types, which are further defined below. This is merely a quick description of each.

Name	Closest C++ Equivalent	Description
Integer	int	Whole number
Float	float	Floating point number
Queue	std::list	FIFO queue
List(type)	std::list⟨type⟩	
String	std::string	String object that provides operations to manipulate itself
File	std::iostream	Abstract type to represent simple I/O operations
Map(KeyType → ValueType, DEFAULT: DefaultValue)	std::unordered_map⟨KeyType, ValueType⟩	A map to translate values of type KeyType to values of type ValueType. If the key isn't present, returns DefaultValue

Name	Description
Blif	Parent object, contains all information about a BLIF file and provides useful operations
Model	Represents a circuit within a BLIF file, and provides methods to manipulate said circuit
BlifNode	A circuit element, or node in the DFG representing the circuit
Signal	A signal within a specific circuit, or Model, representing a set of edges with common source

Field Name	Type	Description
masterOutputs	**List(string)**	List of outputs for the original file
masterInputs	**List(string)**	List of inputs for the original file
main	**Model**	The main circuit in the BLIF file

Blif

Contains helper functions to read in a BLIF and represent it as a DFG. The circuit itself is represented as a Model within Blif.

Model

Represents the circuit as a DFG, with a list of BlifNodes and the Signals both between nodes, and the primary inputs/outputs of the circuit. Also contains a mapping from Signal name to Signal.

BlifNode

Contains the names of the input and output Signals, as well as the properties of the node (type, etc). Does not contain direct references to Signals, merely their names.

Field Name	Type	Description
name	**string**	Name of the circuit
signals	**Map(string → Signal, DEFAULT: NULL)**	Map from signal name to Signal object
outputs	**List(Signal)**	List of output Signal objects
inputs	**List(Signal)**	List of input Signal objects
nodes	**List(BlifNode)**	List of all nodes in a circuit
numLatches	**int**	Number of latches within a circuit
numLUTs	**int**	Number of LUTs within a circuit

Field Name	Type	Description
output	**string**	Name of output signal
clock	**string**	Name of clock signal
inputs	**List(string)**	List of input signal names
cost	**int**	How many clock cycles this node contributes to the critical path. 0 for LUTs and 1 for latches.
type	**string**	Type of node, "latch" or "names" (LUT)
contents	**string**	Parameters describing node which are not used by partitioner but required to recreate BLIF file e.g. initial latch state

Field Name	Type	Description
name	**string**	Name of the signal
source	**BlifNode**	Pointer to source node which drives this signal
sinks	**List(BlifNode)**	List of pointers to this node's sinks.

Signal

Contains references to the signal source, and a list of its sinks. Also stores the signal name.

Represents the circuit as a DFG. Contains a list of nodes, map of signal name → Signal*, and lists of primary inputs and outputs for the circuit. Each node contains the names of its input and output signals, allowing the Signal* to be looked up, then the Signal* contains pointers to its source and sink nodes. This allows the DFG to be traversed by going from node, to signal, to node, etc. A BlifNode represents the information in a circuit element declaration within a BLIF file, which includes only the name of its input and output signals. The actual Signal itself is a separate circuit specific construct designed to allow for ease of traversal of the circuit as a DFG. As such, we don't directly point to signals from a BlifNode*, as the Signal depends on the circuit context. TODO: Image showing DFG traversal, and example of blif file and class contents

2.2 Algorithm

Types marked with an * are custom types defined previously in section 2.1.

Main

Partition, Triplicate, Join and Flatten are all implemented in separate programs. Main is responsible for taking an input file and running it through our toolchain to produce a TMR'd output file.

Algorithm 1 Main Algorithm

Variable	Type	Description
$input$	**File**	Input blif file
$targetRecoveryTime$	**float**	Per partition recovery time (in seconds)
$files$	**List(File)**	circuit partitions, one per file
$file$	**File**	
$header$	**string**	string containing the first three lines of the input file
$output$	**File**	output file

1: **procedure** MAIN($input$, $targetRecoveryTime$)
2: $files \leftarrow$ Partition($input$)
3: **for all** $file \in files$ **do**
4: $file \leftarrow$ Triplicate($file$)
5: **end for**
6: $header \leftarrow input.lines[0 \rightarrow 3]$
7: $file \leftarrow$ Join($files, header$)
8: $output \leftarrow$ Flatten($output$)
9: **end procedure**

We're given a blif file as input. In line 2 we partition the input circuit into a number of sub circuits, each in a separate file, as further expanded in Algorithm 2. Then in lines 3-4 for each partition file, we read it in as a black box, triplicate it, insert voting logic, and write it back out. Next in line 6 we extract the original header, which provides the name, inputs and outputs of the original circuit. We then, in line 7, join all the partitions together with the original name, inputs and outputs (in the same order), as the original circuit, and finally line 8 flattens the circuit, i.e. transforms the generated heirarchical netlist into a flat netlist with only one main model, or circuit, and no submodels.

Variable	Type	Description
$file$	**File**	input file
$targetRecoveryTime$	**float**	maximum per partition recovery time (in seconds)
$blif$	**Blif***	In-memory representation of input blif file
$circuit$	**Model***	Main circuit from input file, represented as DFG
$partition$	**Model***	Circuit, which we are adding nodes to, to make our partition
$queue$	**Queue**	FIFO queue of nodes to visit
$visited$	**Map(BlifNode*→ bool)**	Map of whether a BlifNode is visited
$signal$	**Signal***	
$circuit.outputs$	**List(Signal*)**	List of output Signal* of a circuit
$signal.source$	**BlifNode***	Node which drives this Signal*
$queue.size$	**integer**	Number of nodes in queue
$node$	**BlifNode***	
$file$	**File**	
$files$	**List(File)**	
$numPartitions$	**int**	Counter of number of partitions
$signalName$	**string**	Name of a Signal*
$node.inputs$	**List(string)**	List of names of signals which are inputs to this node
$model.signals$	**Map(string → Signal*)**	Map from signal name to Signal* representing it in that Model*

Table 2.1: Variables for Partition

Partition

Given an input file, Partition reads it in, and splits it into a number of smaller subcircuits, each of which has a maximum recovery time of our target recovery time or less. Each subcircuit is then output to its own separate file, each of which is a valid BLIF and circuit on its own.

Algorithm 2 Partition

```
1: procedure PARTITION(file)
2:     blif ← new Blif(file)                                   ▷ Read in file
3:     circuit ← blif.main                                     ▷ The actual circuit within the blif file
4:     partition ← new Model                                   ▷ Empty Circuit
5:     queue ← new Queue                                       ▷ Empty Queue
6:     visited ← new Map(BlifNode → bool, DEFAULT: false)
7:     for all signal ∈ circuit.outputs do
8:         queue.Enqueue(signal.source)
9:     end for
10:    while queue.size > 0 do
11:        node ← queue.Dequeue()
12:        if visited[node] = true then
13:            continue                                        ▷ Handle each node once and only once
14:        end if
15:        visited[node] ← true
16:        partition.AddNode(node)
17:        if partition.RecoveryTime() > targetRecoveryTime then
18:            partition.RemoveNode(node)
19:            MakeIOList(partition, circuit)
20:            file ← partition.WriteToFile()
21:            files ← files + file
22:            numPartitions ← numPartitions + 1
23:            partition ← new Model                           ▷ Empty Circuit
24:            partition.AddNode(node)
25:        end if
26:        for all signalName ∈ node.inputs do
27:            signal ← model.signals[signalName]
28:            queue.Enqueue(signal)
29:        end for
30:    end while
31:    if partition.size > 0 then
32:        MakeIOList(partition, circuit)
33:        file ← partition.WriteToFile()
34:        files ← files + file
35:    end if
36:    return files
37: end procedure
```

Line 2 reads a BLIF into memory, transforming from the BLIF format described in TODO: Reference to the one represented by TODO: Reference. Lines 12-15 ensure that we visit each node only once, and thus that each node is in exactly one partition, by checking if a node has been visited before and if so, skipping it, otherwise marking it as visited and coontinuing. Lines 16/24 inserts the current node into the open partition, cutting any created cycles and updating values such as critical path length as outlined in Algorithm 5. Line 17 tests if the current partition recovery time is greater than our specified limit, with the algorithm used to calculate the recovery time located at Algorithm 4. If the recovery time is greater we execute lines 18-24, where we remove the just added node to bring our recovery time back under the limit, and then write the partition to a file. Line 18 calculates which signals are primary inputs or outputs for the partition, and promotes them accordingly, with more detail given in Algorithm 3. Writing the partition to a file simply involves outputting the name, inputs, outputs, and a list of every node in the partition in BLIF format. RemoveNode, on line 19, merely removes the node from the partition's list of nodes rather than fully reversing everything AddNode does. As WriteToFile simply serialises the inputs, outputs and node list this is all that's required. Lines 31-34 write out the final partially full partition, if there is one. Again, WriteToFile simply outputs the circuit name, list of inputs, outputs and clocks, and list of nodes, with no further processing required.

MakeIOList

Given an original partition and a subpartition, promote any signals which are sourced or sunk outside of the subpartition to a primary input or output of the subpartition. We iterate through every signal in our

Algorithm 3 MakeIOList

Variable	Type	Description
$partition$	**Model***	Partition to create list of primary inputs and outputs for
$originalCircuit$	**Model***	Original model
$signal$	**Signal***	
$signal.source$	**BlifNode***	The driver for the signal
$partition.inputs$	**List(BlifNode*)**	List of primary inputs for the circuit
$partition.signals$	**Map(string $\rightarrow$ Signal*)**	Map from signal name to Signal*
$originalCircuit.signals$	**Map(string $\rightarrow$ Signal*)**	Map from signal name to Signal*
$signal.sinks$	**List(BlifNode*)**	List of sinks for the signal

```
1:  procedure MAKEIOLIST(partition, originalCircuit)
2:      for all signal ∈ partition.signals do
3:          if signal.source = NULL then                    ▷ If this signal has no driver
4:              partition.inputs.Add(signal)
5:          end if
6:          otherSignal ← originalCircuit.signals[signal.name]   ▷ Get the corresponding signal in
    the original circuit
7:          if count(otherSignal.sinks)−count(signal.sinks) > 0 then  ▷ If the signal has more sinks
    in the original circuit than it does in this partition
8:              partition.outputs.Add(signal)
9:          end if
10:     end for
11: end procedure
```

partition. For each one we check if we have a source (line 4), if not it must be a primary input. Similarly, on line 7 we check if we have a sink which is not represented within our partition. If so, promote it to a primary output of the partition.

RecoveryTime

For a given partition, calculate its error recovery time. The derivation of this algorithm and the values used

Algorithm 4 RecoveryTime

Variable	Type	Description
$latency$	**float**	Circuit latency (i.e. time for input to completely propagate to output) in seconds
$clockPeriod$	**Integer**	Period of the circuit, in seconds. This is estimated as $1.8\times$ the clock period of the original circuit
$criticalPath$	**Integer**	Maximum number of steps between an input and an output
$numFF$	**Integer**	Number of Latches in circuit
$numLUT$	**Integer**	Number of look up tables in circuit
$resynchronisationTime$	**Float**	Time, in seconds, that it takes to resynchronise circuit
$detectionTime$	**Float**	Time, in seconds, that it takes to detect an error
$ReconfigureTime$	**Float**	Time, in seconds, that it takes to reconfigure circuit
$communicationTime$	**Float**	Time, in seconds, that it takes to transmit reconfiguration request to controller

1: **procedure** RECOVERYTIME($partition$)
2: $latency \leftarrow clockPeriod \times (criticalpath + 1)$
3: $detectionTime \leftarrow latency$
4: $resynchronisationTime \leftarrow latency$
5: $reconfigurationTime \leftarrow \max(numFF, numLUT)/160 \times 1.48^{-5}$
6: $communicationTime \leftarrow 5 \times 50 \times (numPartitions + 1) \times clockPeriod$
7: $recoveryTime \leftarrow detectionTime + resynchronisationTime + reconfigurationTime + communicationTime$
8: return $recoveryTime$
9: **end procedure**

is fully discussed in Section TODO: Reference. The criticalpath is a measure of the maximum number of latches on a path from input to output. The +1 is to account for the contribution of combinational logic, which may be up to one additional clock cycle of latency.

AddNode

Insert a node into an existing partition, or circuit, while updating appropriate parameters (i.e. maximum path length and signals) which are depended upon by other components (i.e. recovery time calculation and DFG traversal respectively). Additionally, detect any newly created cycles and cut them. This ensures that the circuit is always an acyclic graph with every node reachable. Lines 3-11 update the appropriate

Algorithm 5 AddNode

Variable	Type	Description
$partition$	**Model***	Model* containing DFG representing partition to add node to
$node$	**BlifNode***	Node to add
$signal$	**Signal***	
$signalName$	**string**	
$partition.cutLoops$	**Map(string → string)**	For signals which have been cut, a map of the old to the new name
$partition.signals$	**Map(string → Signal*)**	Map of signal name to Signal*
$signal.sinks$	**List(BlifNode*)**	List of sinks for a Signal*
$signal.source$	**BlifNode***	Source, or driver, for a Signal*
$inCost$	**int**	Maximum number of critical path steps to reach node, not counting the node itself
$explored$	**Map(BlifNode* → boolean)**	Whether a node has been reached yet in the current iteration

```
1:  procedure AddNode(partition, node)
2:      nodes.insert(node)
3:      for all signalName ∈ node.inputs do
4:          signal ← partition.signals[name]
5:          signal.sinks.Add(node)
6:      end for
7:      signal ← partition.signals[node.output]
8:      signal.source ← node
9:      inCost ← 0
10:     for all signalName ∈ node.inputs do
11:         signal ← partition.signals[signalName]
12:         source ← signal.source
13:         if partition.costs[source] > inCost then
14:             inCost ← partition.costs[source]
15:         end if
16:     end for
17:     UpdateCostsAndBreakCycles(partition, node, NULL, node, inCost, explored, costs)
18: end procedure
```

signals, adding the node as a source or sink the node's inputs and outputs so that this node is reachable

within the DFG. Lines 12-19 then update the maximum path length (or latency in clock cycles) while detecting and cutting any newly created cycles.

UpdateCostsAndBreakCycles

Recursively traverse our network to update maximum path lengths to account for our new node and additional paths. While traversing the network, detect and break any cycles we encounter. This turns a possibly cyclic DFG with partially computed path lengths, into an acyclic DFG with fully computed path lengths.

We care about two things. One, the maximum cost to reach a node, and two, detecting and removing any cycles. Given an existing Directed Acyclic Graph (DAG) which we insert a new node into, then

1. The new node is the root node of a subtree within the DAG.
2. Nodes which are not within the subtree cannot have the maximum cost to reach them change (as nothing has changed in any path to them).
3. Any cycles must pass through the new node, as all the new edges are to or from the new node.
4. Correspondingly, without any cycles the root node will only be reached once at the start.

Consider Figure 2.1 where every node is a latch with cost to reach indicated. Our new node (filled in) is added to an existing DAG. Our new node should now be the root of a subtree which includes all nodes reachable from our new node i.e. all nodes except those crosshatched and unreachable from our new node. We now traverse our DFG recursively, updating the maximum cost to reach each node as we travel. Eventually, in our example we reach our newly added node again indicating a cycle. We thus cut the cycle as detailed in subsection 2.2, recurse back a step, and continue until the entire DFG has been traversed, at which point all cycles have been cut, and all nodes have the maximum path length to them updated. Using this information we develop our traversal algorithm. Line 2 demonstrates an optimisation, in that once a path has been checked we need not recheck it unless we have found a more expensive path to it as otherwise nothing will change. Lines 5-8 check if we have detected a cycle. If so, cut it through cutting the signal, which splits the signal into two. A primary output with the same source, and a primary input with the same sinks, as detailed further in subsection 2.2.

Algorithm 6 UpdateCostsAndBreakCycles

Variable	Type	Description
$partition$	**Model***	Model* containing DFG representing partition to add node to
$root$	**BlifNode***	Newly added node
$parent$	**BlifNode***	Node we just came from
$costToReach$	**int**	Maximum number of critical path steps to reach node, not counting the node itself
$explored$	**Map(BlifNode* → boolean)**	Whether a node has been reached yet in the current iteration
$partition.signals$	**Map(string → Signal*)**	Map of signal name to Signal*
$parent.output$	**string**	Name of the signal the parent nodes drives i.e. the signal we reached this node from
$signal$	**Signal***	Signal we reached this node from
$node.cost$	**int**	1 for latches, 0 for LUTs
$costs$	**Map(BlifNode* → int)**	Map of the cost to reach each node
$node$	**BlifNode***	
$signal.sinks$	**List(BlifNode*)**	List of sinks for a Signal*
$cost$	**int**	Number of critical path steps to reach node, including the node itself

1: **procedure** UPDATECOSTSANDBREAKCYCLES($partition, root, parent, node, costToReach, explored$)
2: **if** $explored[node] = true$ and $costs[node] \geq costToReach$ **then** ▷ Already expanded this path, and we haven't found a more expensive route to it. No point continuing down it
3: return
4: **end if**
5: **if** $parent \neq NULL$ and $node = root$ **then** ▷ We have a cycle, as all newly created cycles must go through the new node, and the new node should only ever be reached once at the start without cycles
6: $signal \leftarrow partition.signals[parent.output]$ ▷ The signal edge we came in on
7: CutSignal($partition, signal$)
8: return
9: **end if**
10: $cost \leftarrow costToReach + node.cost$
11: **if** $cost > costs[node]$ **then**
12: $costs[node] = cost$
13: **else**
14: $cost = costs[node]$
15: **end if**
16: **for all** $child \in partition.signals[node.output].sinks$ **do**
17: UpdateCostsAndBreakCycles($root, node, child, cost, explored$)
18: **end for**
19: $explored[node] = true$
20: **end procedure**

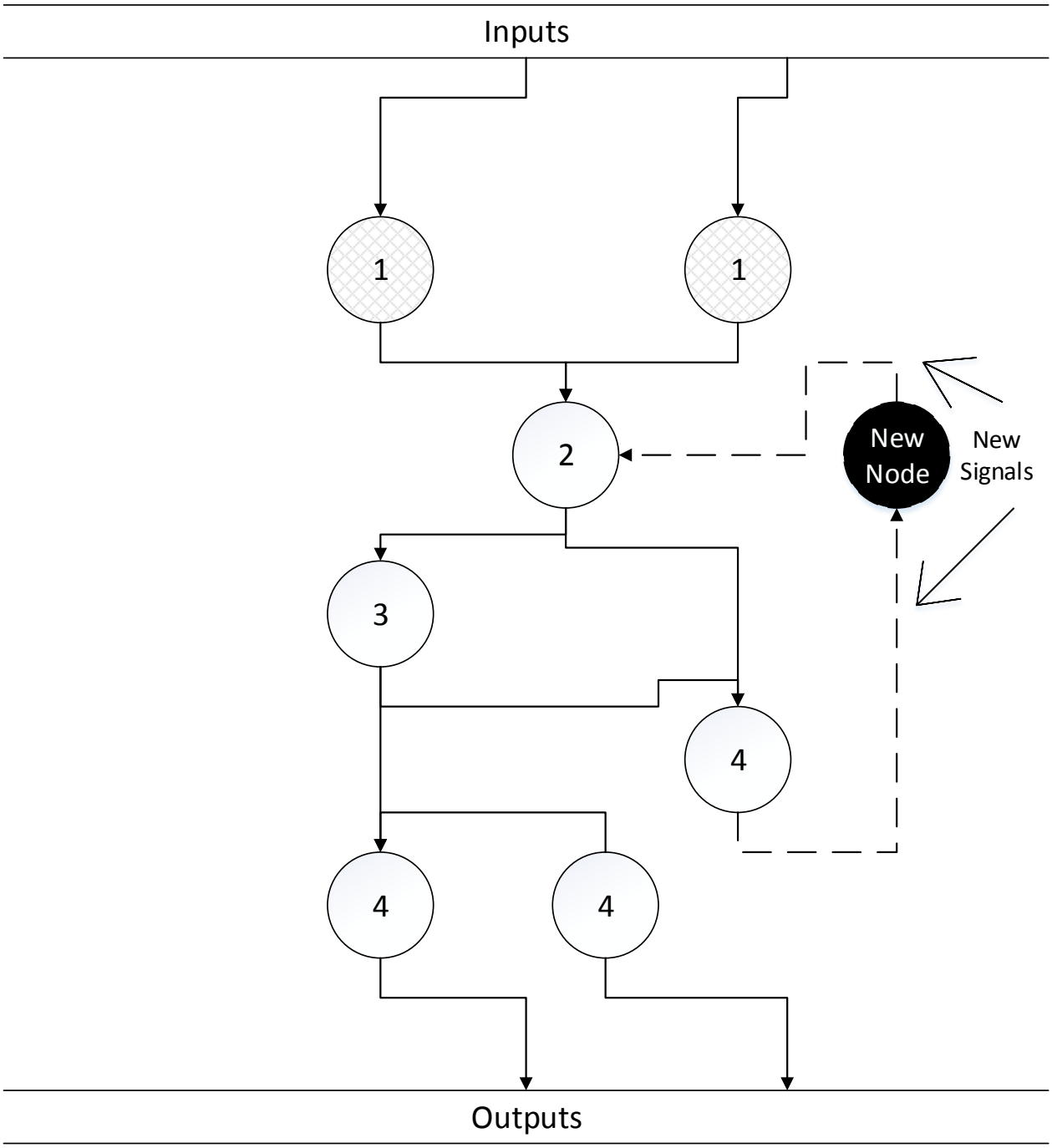

Figure 2.1: AddNode

CutSignal

Given a signal, cut it, by splitting it into two signals. One of which is a primary input with the sinks of the previous signal. One of which is a primary output with the source of the previous signal.

Triplicate

Given a file containing a partition, read it in as a black box, triplicate it, add voter logic, write back out to file.

This method operates on the BLIF in a low level way, dealing with manipulating the actual file contents, rather than operating on an abstract circuit representation, as we transform a flat circuit, into a heirarchical circuit, in which our original flat circuit remains untouched but we insert voting and similar logic around it. We read in our partition circuit and voter circuit. We now create three partition subcircuit and one voter subcircuit definitions. We match up our signal names between them appropriately, and then write out our subcircuit definitions, followed by our partition and voter subcircuits.

This transforms a file from format:

```
1       .name partition
2       .inputs ...
3       contents
```

Into one in format:

```
1       .name TMRPartition
2       .inputs ...
3       .subckt partition
4       .subckt partition
5       .subckt partition
6       .subckt voter
7       .end
8
9       .name voter
10      ...
11      .end
12      .name partition
13      ...
14      .end
```

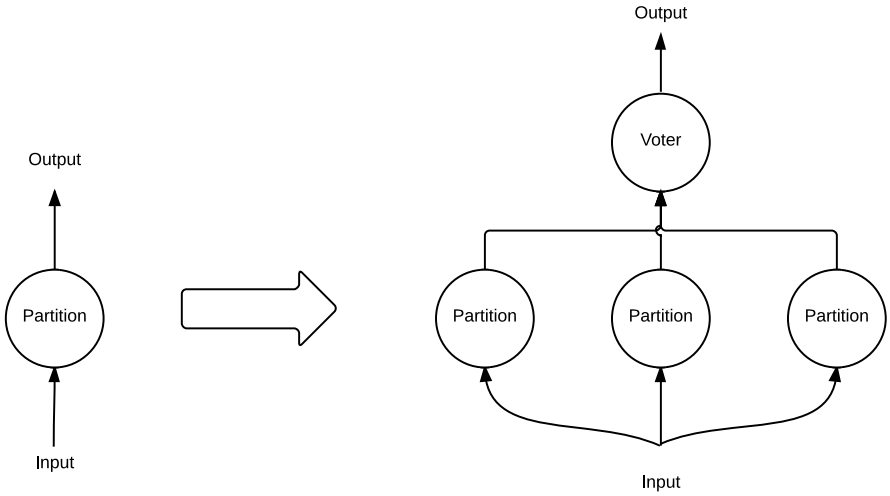

Figure 2.2: Triplicate

Join

Given a list of blif files, concatenates them all together, creates subcircuit definitions to connect them all together, and writes them to a file

This transforms a set of files in format:

```
1       .name partitionN
2       .inputs ...
3       contents
```

Into one file with format:

```
1       .name TMR
2       .inputs ...
3       .subckt partition1
4       .subckt partition2
5       .subckt partition3
6       ...
7       .end
8
9       .name partition1
10      ...
11      .end
12      .name partition2
13      ...
14      .end
15      ...
```

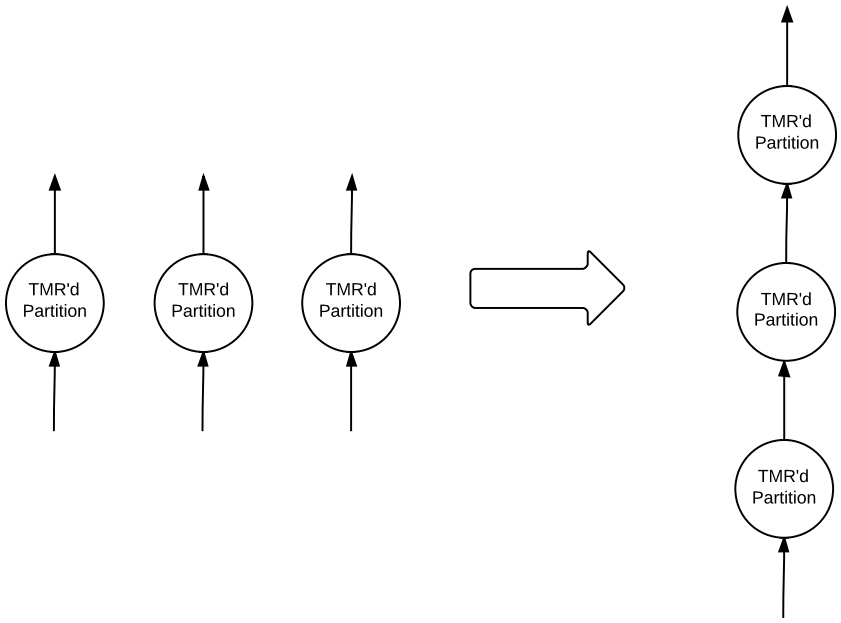

Figure 2.3: Join

Flatten

Given a heirarchical blif file, run it through abc [**?**]link to flatten it, and postprocess if necessary.

Algorithm 7 Flatten

Variable	Type	Description
$file$	**File**	File to flatten

1: **procedure** FLATTEN($file$) ▷ Flattening is currently performed by abc, called with parameters:
2: ./abc -o output -c echo file ▷ Due to bug in abc, clock information is stripped from latches, so we then call grep and sed to fix the output file
3: $latch$ ←split(grep -m 1 'latch' file)
4: **if** $latch$ **then**
5: sed -ri 's/(\.latch.+)(2)/\1 '+latch[3] + ' ' + latch[4] + ' 2/' output
6: **end if**
7: **end procedure**

./abc is provided an input file, given the command to echo the current file, and told to output everything to output. grep is called to search for latches, and return the latch information if there is one. If there is, replace the faulty latch information with the correct information. This assumes that there is only one global clock, all latches are triggered on the same signal (e.g. rising edge, falling etc), and all latches have initial state don't care, which holds true for all provided benchmarks.

Test

abc is also used to optionally test the generated circuit to verify that it is equivalent to the original. It does this by creating a miter circuit, which is derived by pairing inputs for the two circuits, and feeding output pairs into an XOR gate which are then ORd to produce the single output. For any given input, the miter circuit output is 0 if both circuits produce the same set of outputs for the input set, and 1 if the outputs differ, which turns verification into a Boolean Satisfiability Problem (SAT). The circuits are then simplified by merging equivalent nodes and removing redundant while being regularly tested for various inputs. This proceeds until a counter example is found, or the circuit is shown to have constant output 0 for all possible inputs **??**. While SAT is NP-complete, in practice the large amount of redundancy in TMR'd circuits allows allows testing to complete in only a few seconds for any of our benchmarks.

2.3 Performance

The algorithm must visit each node in the input circuit once to add it to a partition, giving a factor of n. Additionally, for each node added to a partition, in the worst case every other node already in the partition must be visited to detect cycles and update costs, making AddNode worst case linear in the

number of nodes in the partition. Making the list of inputs and outputs is linear in the number of signals in the partition. In practice, the number of signals will be approximately equal to the number of nodes (each node drives one signal, plus the number of inputs to the circuit). This gives us worst case $O(n^2)$. Triplicating is linear in the number of inputs and outputs, joining is $O(nk)$ where n is the number of circuits, and k is the number of inputs and outputs for each circuit. In practice, joining, triplicating and flattening are all subsecond, while partitioning and testing are a few seconds. This compares to VPR's running time of up to an hour for some TMR'd benchmark circuits. Add in table of results !

2.4 Design Choices

As much as possible, we would like our implementation to be easily extensible to multiple architectures. The actual partitioner operates on a DFG so it can be mostly architecture agnostic, only requiring the estimation functions to be architecture aware. From initial steps in this thesis we wrote Python scripts capable of performing basic operations on BLIF files which were used as the basis for Triplicating and Joining. Given time the funcionality of each step (partition, triplicate, etc) could all be combined in one program, however it was considered a much lower priority than creating a working reference implementation.

Other design choices include deciding on VPR due to its open nature as discussed earlier in Section 1.3, and how we traverse our DFG. A depth first traversal as we ended up using tends to generate long narrow pipelines within each partition, thus increasing the number of register stages but reducing the number of inputs and outputs for each partition, whereas a breadth first traversal lends itself to fewer register stages for the same number of nodes, however more inputs and outputs (and hence voters) for each partition. A possible future improvement is implementing a more advanced traversal algorithm, for example A* with an appropriate heuristic could allow for more elements per partition. Benchmark results compararing the two options can be found at Reference and add. !

Additionally, we are faced with a choice as to when in the CAD process to partition. The closer to the end of the process the more control we have, and the better our ability to estimate area and timing, but the harder it is to partition. As we are inserting new elements we want to partition before packing/placement to allow VPR to pack and place our inserted elements.

Choice of Language

We are using a combination of languages, mainly Python and C++. Language choice primarily came down to preference regarding familiarity and personal taste although a few other considerations were kept in mind. For BLIF joining and insertion of the voting logic Python was used. BLIF files are plain text and the text parsing to join and insert is computationally simple, so the primary concern was short development time while still being readable and maintainable (although Python's performance on text is still quite reasonable) [19]. For the actual partitioner C++ was chosen for a few reasons. Firstly, it was

expected that the area and time estimations could be quite computationally expensive, so a lower level compiled language was chosen for performance reasons [19]. Secondly, VPR is written in C, so using C or C++ allowed for easy code reuse, or merging the partitioner and VPR. Our reason for choosing C++ over C was that we preferred an object oriented language as we felt it would be easier to maintain, and would better lend itself to our goal of extensibility, as well as its libraries making our implementation much easier.

2.5 Input File Format

The BLIF file format is a textual format which describes an arbitrary sequential or combinational network of logic functions [21]. Of the full BLIF specification, VPR only supports a subset of, and hence our partitioner is also designed to only support that same subset.

```
1       .model voter
2       .inputs in1 in2 in3
3       .outputs out1 out 2
4       .clock clock
5       .names in1 in2 in3 out1
6       11- 1
7       1-1 1
8       -11 1
9       .latch in1 out2 re clock 1
10      ...
11      commands
12      ...
13      .end
```

Listing 2.1: BLIF file layout

Model name:	.model ⟨Name⟩	The name of the model.
Input List:	.inputs {Signal}	The model inputs.
Output List:	.outputs {Signal}	The model outputs.
Clock List:	.clock {Signal}	The model clocks.
		Commands
LUT:		.names {InputSignals} ⟨OutputSignal⟩ {Line}
Latch:		.latch ⟨InputSignal⟩ ⟨OutputSignal⟩ [Field ClockSignal] [Field]
Optional End Marker:		.end

{Name} indicates 1 or more of Name. ⟨Name⟩ indicates a compulsory field. [Name] indicates an optional field. A combinational logic element (.name) is followed by one or more lines describing the

logic function it implements. However, our partitioner only cares about node type and the signals (named with Signal above) as it builds and traverses the DFG. All other element information is stored and written back out when the node is written. Likewise for *Field*s.

VPR only supports flat BLIF files, so only one module declaration is allowed per BLIF file. **abc!** (**abc!**) can be used to flatten BLIF files for use by VPR.

Chapter 3

Results

3.1 Benchmarking Procedure

These results were collected by running benchmark circuits through an automated test suite written in Python by the author. For each benchmark circuit, and each target recovery time, 10 repetitions were performed, due to the variation in reported values due to the random nature of placement. The original circuit is run through VPR to collect base results, then the circuit is run through our partitioner to TMR it. The TMR'd version is then verified by abc as being functionally equivalent to the orignal, and then run through VPR to collect TMR'd results. Each run of VPR used a randomly generated seed for the placer. The mean of the reported values across the 10 repetitions was then taken. The benchmarks used were the 20 largest MCNC LGSynth93 circuits, as provided by the open source VTR project Reference ! and described in table 3.1. The set of target recovery times used is $10^{-3}, 2.5 \times 10^{-4}, 7.5 \times 10^{-5}$s. The voter used is a simple 3-input LUT, which uses one BLE per output signal from each partition.

Target Architecture

VPR allows us to specify a custom architecture for it to run against in an XML format. We opted for the default architecture detailed in [15] consisting of a grid of CLBs each consisting of ten fully interconnected BLEs, and each BLE having a latch and 6-LUT as ilustrated in Figure 3.1. Table 3.2 details the number of primitives (latches and LUTs per CLB. Primarily of interest is that each BLE has 6 inputs and 1 output and each CLB has 33 inputs and 10 outputs.

3.2 Sanity Check

The following results are for the tseng circuit at a target recovery time of 10^{-4}s. The reported values can be compared to each other as a manual sanity check. Compare Area usage. Compare Recovery Time. Compare Partition Size.

	Number of:			
Name	Inputs	Outputs	Latches	LUTs
alu4	14	8	0	4574
apex2	38	3	0	5637
apex4	9	19	0	3805
bigkey	229	197	672	5294
clma	62	82	99	25177
des	256	245	0	5018
diffeq	64	39	1131	4521
dsip	229	197	672	4283
elliptic	131	114	3366	10920
ex1010	10	10	0	13804
ex5p	8	63	0	3255
frisc	20	116	2658	10733
misex3	14	14	0	4205
pdc	16	40	0	13765
s298	4	6	24	5796
s38417	29	106	4389	18232
s38584.1	38	304	3780	18835
seq	41	35	0	5285
spla	16	46	0	11116
tseng	52	122	1155	3260

Table 3.1: Benchmark circuits used

Component	Number	Notes
Flip Flop	1 per BLE	Shown as FF on Diagram
6-LUT	1 per BLE	
MUX	1 per BLE	
BLE	10 per CLB	
Crossbar	1 per CLB	
CLB	Autosized by VPR	

Table 3.2: Architecture Elements

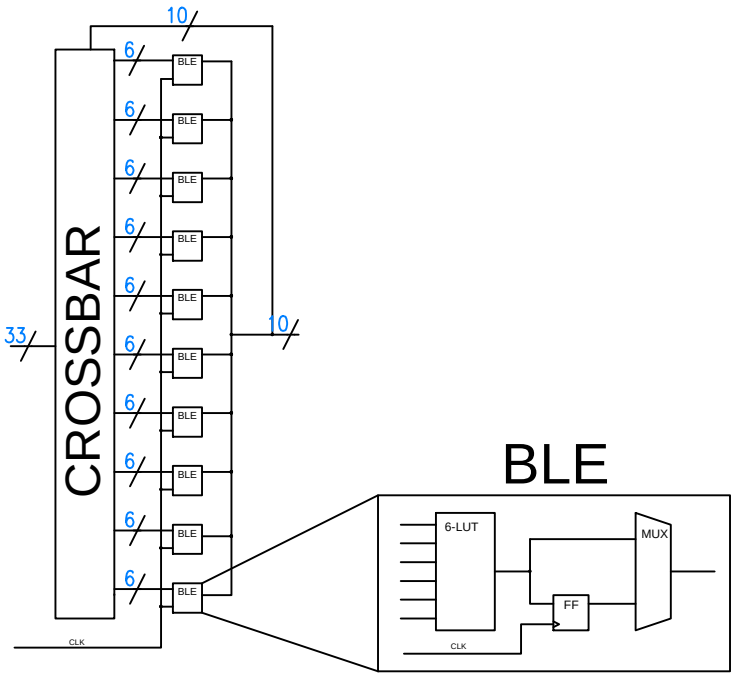

Figure 3.1: CLB Architecture

3.3 Stochastic Nature of Placement

As VPR's placer uses simulated annealing which contains a random factor, there was variation between different runs, potentially extremely large such as the example in table Add in. The number of runs was arbitrarily set at 10, as it is large enough that one outlier won't sway the results too significantly, however small enough that collection of results could occur in a reasonable amount of time. 10 runs for one set of parameters would take around one third to one half of a day to finish on the server used (8× Intel Xeon X7560 CPUs at 2.27GHz).

3.4 Area

As expected, area usage is slightly greater than tripled, which corresponds to results in literature [4]. The number of BLEs used is equal to three times to original, plus the total voter area. The larger the number of partitions, the greater the area usage due to the additional voters required.

3.5 Operating Frequency

In general, the more partitions the slower the resulting circuit. This result is unsurprising, as increasing the number of voters increases the number of signals to be routed pushing average wire length upwards.

Average slowdown is around the Value mark, though it varies considerably from circuit to circuit. For our recovery time calculations, as they required an estimate of the final circuit clock period we used an estimate of $1.8\times$ the original circuit's clock period. As we can see from the results, in the general case this factor is sufficiently conservative, and we can likely get away with a lower value, say 1.5 for most cases.

3.6 Recovery Time

Chapter 4

Limitations and Future Work

Our algorithm implementation is still just a first pass at the problem to evaluate it's feasibility. There is still much work to be done.

Some notable limitations are that our implementation operates on BLIF files and targets a theoretical simplified architecture. In practice, it would be ideal to use and target industry standard tools, formats and architectures. There are a number of assumptions and approximations made as part of the implementation, especially in the calculation of recovery time. Improving the accuracy of approximations allows the partitioner to find better solutions. And lastly, the partitioner itself makes no attempt to find an optimal solution. Partitions may be closed off before they're full, or partitions may be unbalanced with some having many more voters or a much longer path length than others. The traversal algorithm can be updated with a heuristic and the capability of backtracking to find denser partitions. However, the limiting factor tends to be the partition size, and when (as in the benchmark circuits), there are many more LUTs than latches, the ability to reduce the number of partitions through clever partitioning is extremely limited.

Chapter 5

Conclusion

The algorithm shows promise. Though there is still much work to be done the intial results collected in this thesis indicate that the partitioning method described by reference and implemented by this thesis is capable of providing effective fault tolerance with overhead not too much greater than a typical TMR solution which TMRs the entire circuit, and scrubs regularly. !

Chapter 6

Benchmarking

6.1 Overview

For benchmarking we use 20 MCNC benchmarks (detailed in Table 3.1) obtained as part of the Verilog To Routing (VTR) project[1] which we will be using to evaluate the performance of our partitioner and our TMR scheme in general. Additionally, we're looking for ways of estimating area usage and timing information from a BLIF file or DFG, without needing to actually place and route the partial circuit after each iteration, as doing so is computationally prohibitive. Here to the end of section gets rewritten To start with we made simple test circuits to compare to our benchmarks by triplicating each entire benchmark and adding in simple voter logic. As progress is made on the partitioner we can start collecting results from further partitioned circuits; however triplicating the entire circuit should be sufficient for rough approximations provided $elements_{circuit} >> elements_{voter}$.

To make the test circuits we created a small Python script which, given an input circuit and input voter circuit, triplicates the circuit and adds voting logic. It creates a hierarchical BLIF file, that is, it contains nested subcircuits, which are then passed through an external program called **ABC!** (**ABC!**) [**?**] to flatten it into a format VPR can read.

Expected Results

As is well described in literature (e.g. [4]), the area usage should increase by a factor of slightly more than three. There are three copies of each component, plus additional components for the voting circuitry. Maximum frequency is expected to decrease slightly due to the additional components increasing wire length and crowding routing channels however this is likely to vary depending on circuit.

[1] `http://code.google.com/p/vtr-verilog-to-routing/`

6.2 Methodology

To start with, we wanted to collect rough estimates on the impact of partitioning a circuit to provide a baseline with which to compare our partitioning algorithm, and to develop the rough estimates needed for our partitioning algorithm. To that end we first created a simple Python script to take an arbitrary input circuit, triplicate it, and insert arbitrary voter logic. These triplicated circuits were then placed and routed by VPR, as were the original benchmarks, and the results compared.

Width	Num. Latches	Num. LUTs	FPGA Width	Channel Width	Num. Wire Segments	Used Area	Frequency	CPU Time
Auto Width	300%	301%	169%	119%	106%	301%	93%	405%
200 Width	300%	301%	169%	N/A	110%	301%	85%	385%
60 Width	300%	301%	169%	N/A	113%	302%	86%	444%

Table 6.1: Median values for specified channel widths as a percentage of non TMR equivalent

Name	Num. Latches	Num. LUTs	FPGA Width	Num. Wire Segments	Used Area	Frequency	CPU Time
pdc 200 width	N/A	300%	176%	104%	301%	75%	425%
tseng 200 width	300%	312%	169%	126%	308%	102%	388%

Table 6.2: Increase in circuits with maximum and minimum frequency slowdown

Just to fix formatting. Temporary VPR is used with our architecture file (described in Section **??**) and the command line options

```
1       VPR architecture.xml circuit.blif --full_stats[ --route_chan_width x]
```

where x is the width of the routing channels and - -full_stats tells VPR to be more verbose in its output. As mentioned earlier, if - -route_chan_width is excluded then VPR determines the minimum channel width needed to successfully route the circuit [15]. We then place and route our benchmark circuits and our partitioned circuits. VPR itself then reports the area usage, critical path time (inverse of the frequency), and other statistics we analysed. Unfortunately VPR does not report the number of register stages however our partitioner will, as it needs to calculate the number of steps for its time estimation function.

6.3 Results

The results listed in Tables 6.1 and 6.2 highlight information of interest in a few key circuits, rather than including page after page of tables. Any aggregate statistics (e.g. median) are calculated on the entire result set, not just the results included. No collected results were considered to be outliers and the only exclusions from the median calculation are those where the operation was not able to be completed, so there is no data. These tables list the median characteristics of the TMR versions of our benchmark circuits as a percentage of the original (100% is the same, 200% is double, 50% is half); additionally, they detail the time taken to pack, place and route.

6.4 Discussion

Our simple voter circuit consists of one 3-LUT per output. Therefore we expect the number of logic elements (latches and combinational logic) to be exactly three times larger, with an additional 3-LUT per original circuit output. As shown in Table 6.1 our triplicated circuits are just slightly over three times as large. Circuit area should be roughly tripled as well, which again, matches, with the width increasing by $1.69 \approx \sqrt{3}$ and the used area increasing by just over triple. The partitioned circuits require slightly larger channels, in order to route the extra wires needed, and the additional elements and wires lead to slightly more segments per wire, and a slightly lower maximum frequency. Of note is that the time to place and route the partitioned circuits was much higher, taking around four times longer.

Circuits were 15% slower on average, with a worst case of 25% overall and a best case (in 200 width circuits) of a 2% speedup. For minimum channel routing the smallest median slowdown was observed as on average the minimum channel width needed for partitioned versions was higher, giving the router more flexibility. For 60 width circuits some were unable to be routed, therefore the results do not represent all circuits. For those reasons the reported statistics are taken from the 200 width circuits.

The speedup, while small, is unusual. It is likely due to the packer having more options, and due to the larger available area (as the packer will only increase the number of CLBs, and hence FPGA area used, when it can no longer fit new primitives in the current block).

Chapter 7

Partitioning Algorithm

All this section gets replaced with new algorithm description !

7.1 Estimating Restrictions

As mentioned earlier, in order to partition our circuit we need a method of calculating the partition's (including voter logic) recovery time, which is based on circuit area (affects time to reconfigure), number of register stages (affects time to detect errors and resynchronise), and frequency (affects time to detect errors and resynchronise). Calculating the number of register stages is accomplished while traversing the DFG. Area and timing information are more difficult to determine as they rely on the placement and routing of the circuit. Placing and routing each partial partition every step as we traverse is not computationally feasible in a reasonable amount of time, as placement and routing are relatively slow processes and one of our goals is for our partitioning stage to be approximately as fast as the other stages. Therefore, we need a way of estimating them. To do so we have collected preliminary benchmark information for a number of test circuits and analysed them for patterns allowing us to accurately estimate area and timing from a given circuit without placing and routing.

Results for Time and Area Estimation

Figure 7.1 illustrates the relationship between used circuit area and the number of the most common primitive. In every benchmark circuit there were more combinational logic elements than any other primitive, hence we looked at the relationship with the number of combinational logic elements. Table 7.1 duplicates what was shown in Table 6.2, and is shown again for convenience. It details the increase in circuit characteristics between the TMR and non TMR versions of the circuit, as a percentage of the original (100% is no change, 200% is double, and so on) that displayed the greatest decrease in maximum frequency.

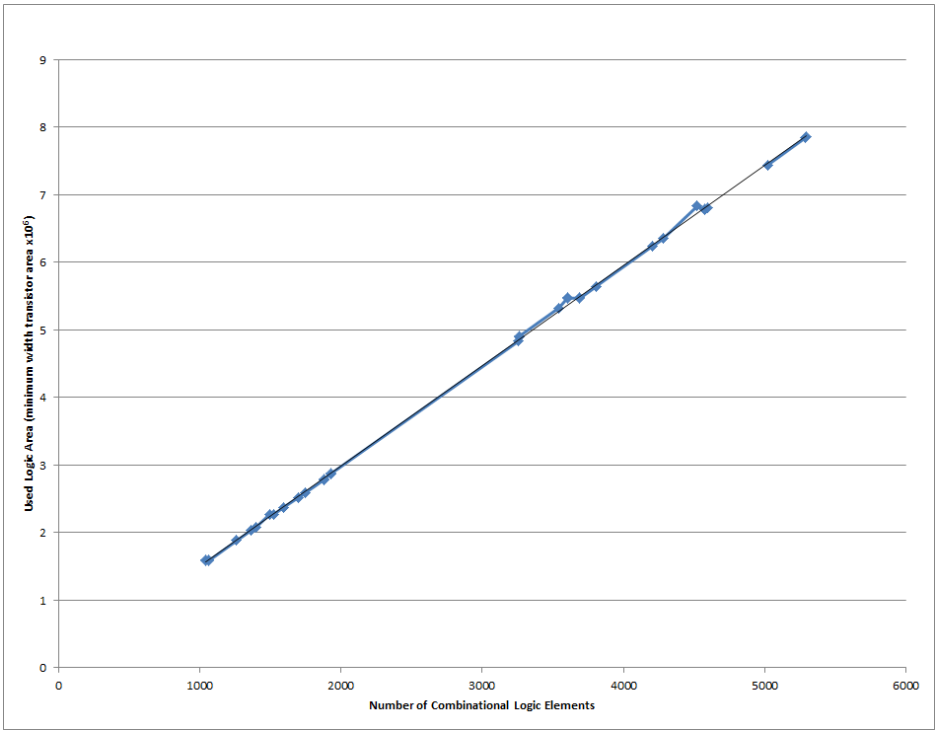

Figure 7.1: Circuit Area compared to number of Logic Elements

Name	Num. Latches	Num. LUTs	FPGA Width	Num. Wire Segments	Used Area	Frequency	CPU Time
pdc 200 width	N/A	300%	176%	104%	301%	75%	425%

Table 7.1: Circuit characteristics of benchmark with greatest frequency slowdown, expressed as a percentage of non TMR base

Discussion of Time and Area Estimation

As shown in Figure 7.1 the area usage can be accurately estimated, as there is a clear relationship between the number of nodes and the area usage. The architecture we are using has one latch and one LUT per BLE, so for our supported logic elements the number of BLEs used is close to linear in $max(num_{latch}, num_{names})$. VPR's packer can be either timing or area driven. Currently we are using default settings (mostly area driven) giving us the linear relationship shown in Figure 7.1; however even when completely timing driven the packer still tries to fill every CLB [14].

After we have a basic partitioning algorithm, an area of further investigation is the impact of changing VPR's settings on the benchmark results, and the accuracy of our estimation functions.

Timing information, on the other hand, is harder to estimate with no obvious pattern, with maximum frequency appearing independent of the number of nodes. In Section 6.3 we saw that the median

slowdown was 15% with a 25% worst result. Conversely, for a few rare cases the partitioned version is actually faster. Initially we will do a rough place and (optionally) route of the original circuit to determine a base time, then multiply it by an experimentally determined slowdown factor to obtain an estimate for the frequency. Initially we are using a slowdown factor of 2 (so half speed after partitioning) which easily encompasses all test circuits we've tried. We can then modify this factor by hand to examine if the impact of it on the final partition's performance warrants improving our estimation function.

Chapter 8

What next

8.1 Progress

The initial partitioner implementation is still in progress. We anticipate a basic working version by November 2012, and then will spend the next months collecting results and improving the partitioner. Done:

- Can read a BLIF file into a DFG.
- Can traverse a circuit represented as a DFG
- Have basic area and timing estimation functions.
- Can triplicate an arbitrary circuit (in a single BLIF file) and insert arbitrary voter logic (stored in another BLIF file).
- Initial benchmarks.

To Do:

- Write DFG to BLIF.
- Incorporate Python scripts into partitioning toolchain.
- Benchmark initial partitioning algorithm.
- Improve partitioner benchmarks.
- Investigate the effect of changing VPR's default parameters upon our results.
- Combine functionality of Python scripts and C++ partitioner into one program.
- Incorporate that single program into VTR's design flow, likely as part of VPR.

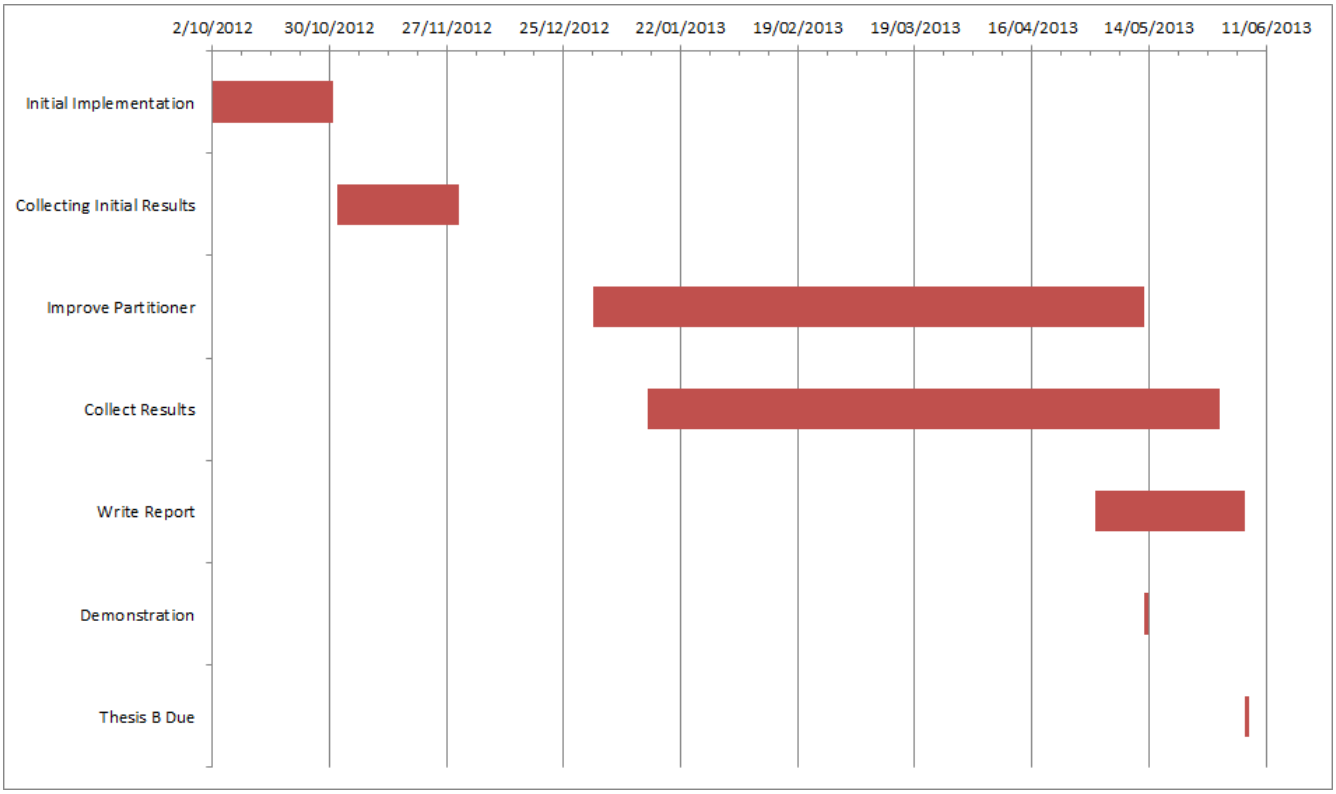

Figure 8.1: Schedule

8.2 Schedule

Figure 8.1 illustrates our anticipated schedule from the beginning of October 2011 until Thesis B is due. The rest of the year is allocated towards an initial partitioner implementation and preliminary results. December is set aside for Christmas holidays, and then most of 2012 will be used for collecting results and further refining the partitioning algorithm on the basis of the collected results.

Chapter 9

Conclusion

We are currently on track with our initial schedule, and expect to begin collecting results on our partitioner implementation, rather than the effects of generic TMR, at the end of this year. During the Christmas holidays progress will likely be quite limited however as we are very close to a working implementation it is believed to be achievable. Our results collected so far reflect only TMR in general, rather than our specific implementation, and they match those of literature and our expectations. We expect slightly worse performance from our partitioner due to additional logic being inserted, but not significantly so.

Appendix A

Results

This appendix tabulates the data used to calculate the relationships discussed in this thesis.

Name	Num. Latches	Num. LUTs	FPGA Width	Channel Width	Av. No. Wire Segments	Frequency (MHz)	CPU Time (s)
alu4	0	1522	15	200	4.76391	225	34.566
alu4TMR	0	4574	25	200	5.29148	188	132.41
apex2	0	1878	16	200	5.5124	216	47.45
apex2TMR	0	5637	29	200	6.21459	172	197.825
apex4	0	1262	14	200	5.0436	249	31.272
apex4TMR	0	3805	23	200	5.33318	204	119.002
bigkey	224	1699	16	200	3.70506	427	56.61
bigkeyTMR	672	5294	27	200	4.93838	377	193.388
clma	33	8365	34	200	5.62286	115	379.801
clmaTMR	99	25177	59	200	6.2762	103	2146.4
des	0	1591	16	200	4.07107	262	98.709
desTMR	0	5018	27	200	3.9862	229	263.883
diffeq	377	1494	15	200	3.0611	157	60.103
diffeqTMR	1131	4521	25	200	3.44041	156	204.691
dsip	224	1362	14	200	3.823	433	60.372
dsipTMR	672	4283	24	200	4.74885	377	177.405
elliptic	1122	3602	23	200	4.2743	134	123.967
ellipticTMR	3366	10920	39	200	5.15534	130	513.637
ex1010	0	4598	25	200	5.31938	176	146.81
ex1010TMR	0	13804	44	200	5.4995	134	655.814
ex5p	0	1064	13	200	4.95796	240	30.659
ex5pTMR	0	3255	22	200	5.2736	187	112.023
frisc	886	3539	23	200	5.52549	94.3	144.196
friscTMR	2658	10733	39	200	5.82234	90.1	525.145
misex3	0	1397	14	200	4.93	244	35.739
misex3TMR	0	4205	24	200	5.46202	198	136.961
pdc	0	4575	25	200	7.21792	175	167.232
pdcTMR	0	13765	44	200	7.51339	131	711.155
s298	8	1930	17	200	4.76794	124	47.789
s298TMR	24	5796	29	200	4.83777	116	185.169
s38417	1463	6042	30	200	3.53974	158	241.471
s38417TMR	4389	18232	51	200	3.78557	149	942.7
s38584.1	1260	6177	30	200	3.67662	206	263.313
s38584.1TMR	3780	18835	52	200	4.36338	157	1199.39
seq	0	1750	16	200	5.31333	253	50.624
seqTMR	0	5285	27	200	6.23725	193	184.467
spla	0	3690	23	200	6.44786	190	122.311
splaTMR	0	11116	39	200	6.75377	152	496.416
tseng	385	1046	13	200	3.04212	161	30.561
tsengTMR	1155	3260	22	200	3.82465	164	118.583

Table A.1: Results for 200 width channels

Name	Num. Latches	Num. LUTs	FPGA Width	Channel Width	Av. No. Wire Segments	Frequency (MHz)	CPU Time (s)
alu4	0	1522	15	60	4.79098	241	22.625
alu4TMR	0	4574	25	60	5.38017	193	101.828
apex2	0	1878	16	60	5.53926	212	34.256
apex2TMR	0	5637	29	60	6.34397	164	153.485
apex4	0	1262	14	60	5.13079	241	20.928
apex4TMR	0	3805	23	60	5.66967	198	90.166
bigkey	224	1699	16	60	3.79333	421	43.024
bigkeyTMR	672	5294	27	60	5.12677	363	154.662
clma	Could Not Route						
clmaTMR	Could Not Route						
des	0	1591	16	60	4.15635	257	50.68
desTMR	0	5018	27	60	4.07778	230	141.366
diffeq	377	1494	15	60	3.20978	151	28.392
diffeqTMR	1131	4521	25	60	3.60614	148	115.085
dsip	224	1362	14	60	3.84115	434	36.32
dsipTMR	672	4283	24	60	4.87989	368	118.515
elliptic	1122	3602	23	60	4.76756	137	101.398
ellipticTMR	3366	10920	39	60	5.74891	133	475.005
ex1010	Could Not Route						
ex1010TMR	Could Not Route						
ex5p	0	1064	13	60	5.29429	241	18.899
ex5pTMR	Could Not Route						
frisc	886	3539	23	60	6.17131	94.7	107.33
friscTMR	Could Not Route						
misex3	0	1397	14	60	4.99571	241	21.286
misex3TMR	0	4205	24	60	5.64103	197	91.433
pdc	Could Not Route						
pdcTMR	Could Not Route						
s298	8	1930	17	60	4.62137	122	27.868
s298TMR	24	5796	29	60	4.75444	118	120.257
s38417	1463	6042	30	60	3.66998	160	172.413
s38417TMR	4389	18232	51	60	3.87309	153	758.585
s38584.1	1260	6177	30	60	3.83166	202	195.832
s38584.1TMR	3780	18835	52	60	4.67375	159	944.364
seq	0	1750	16	60	5.30778	245	32.426
seqTMR	0	5285	27	60	6.56298	188	149.187
spla	0	3690	23	60	6.46323	188	86.03
splaTM	Could Not Route						
tseng	385	1046	13	60	3.22621	161	20.384
tsengTMR	1155	3260	22	60	3.93092	164	79.889

Table A.2: Results for 60 width channels

Name	Num. Latches	Num. LUTs	FPGA Width	Channel Width	Av. No. Wire Segments	Frequency (MHz)	CPU Time (s)
alu4	0	1522	15	34	5.61203	196	88.236
alu4TMR	0	4574	25	48	5.6293	182	245.343
apex2	0	1878	16	48	5.78099	204	80.968
apex2 TMR	0	5637	29	60	6.3913	167	885.343
apex4	0	1262	14	48	5.74387	175	55.509
apex4 TMR	0	3805	23	58	5.59716	181	357.909
bigkey	224	1699	16	42	4.00538	422	84.037
bigkey TMR	672	5294	27	48	5.46703	351	314.02
clma	33	8365	34	64	5.9249	111	826.48
clma TMR	99	25177	59	74	6.81963	94.3	6225.16
des	0	1591	16	46	4.46904	248	85.209
des TMR	0	5018	27	44	4.43131	229	329.551
diffeq	377	1494	15	38	3.67617	152	53.137
diffeq TMR	1131	4521	25	44	3.94535	156	238.817
dsip	224	1362	14	40	4.14675	446	86.123
dsip TMR	672	4283	24	38	5.10172	377	207.014
elliptic	1122	3602	23	50	5.19297	133	289.63
elliptic TMR	3366	10920	39	60	5.74707	133	1562.75
ex1010	0	4598	25	64	5.33384	172	401.434
ex1010 TMR	0	13804	44	62	5.70191	131	1399.9
ex5p	0	1064	13	50	5.64865	229	53.45
ex5p TMR	0	3255	22	62	6.03046	174	452.114
frisc	886	3539	23	56	6.66421	96.2	429.658
frisc TMR	2658	10733	39	66	6.5103	90.1	1383.44
misex3	0	1397	14	42	5.74857	233	60.019
misex3 TMR	0	4205	24	50	5.86212	190	368.648
pdc	0	4575	25	64	7.8308	156	397.958
pdc TMR	0	13765	44	72	7.74884	121	1005.6
s298	8	1930	17	30	5.16031	117	2620.11
s298 TMR	24	5796	29	34	4.97929	119	425.303
s38417	1463	6042	30	42	4.02152	158	376.671
s38417 TMR	4389	18232	51	50	3.96346	147	7381.12
s38584.1	1260	6177	30	44	4.22808	200	459.989
s38584.1 TMR	3780	18835	52	56	4.69062	156	2790.9
seq	0	1750	16	46	5.86111	207	105.526
seq TMR	0	5285	27	58	6.68624	190	448.058
spla	0	3690	23	54	7.08891	144	357.396
spla TMR	0	11116	39	66	6.92343	145	1320.57
tseng	385	1046	13	34	3.63807	163	49.618
tseng TMR	1155	3260	22	42	4.36026	163	183.167

Table A.3: Results for autosized width channels

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