

OPL1000

ULTRA-LOW POWER 2.4GHZ WI-FI + BLUETOOTH SMART SOC

Data Sheet

Non-NDA Version



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| 05/17/2018 | 0.1 | <ul style="list-style-type: none">Initial Release |
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1. GENERAL DESCRIPTION

The OPL1000 SoC features a fully integrated 2.4GHz radio transceiver and baseband processor for Wi-Fi 802.11b and Bluetooth® Smart applications. The SoC can be used as a standalone application-specific communication processor or as a wireless data link in hosted MCU systems where ultra-low power is critical. The OPL1000 supports flexible memory architecture for storing profiles, stacks and custom application codes, and can be updated using Over-The-Air (OTA) technology. Qualified Bluetooth Smart protocol stack and Wi-Fi TCP/IP stack are stored in a dedicated ROM. The OPL1000 is equipped with dual processors, ARM® Cortex®-M0 and M3, for handling different processes. All software runs on the ARM® Cortex®-M0 processor while more intensive application-specific activities run on the ARM® Cortex®-M3 processor. The OPL1000 can be connected to any external MCU through SPI, I2C or UART interfaces and sensors or other devices through GPIOs. The transceiver interfaces directly to the antenna and is fully compliant with the Wi-Fi 802.11b and Bluetooth 5.0 BLE standards. With integrated antenna switch, RF balun, power amplifier (PA) and low noise amplifier (LNA), the OPL1000 allows both Wi-Fi and Bluetooth Smart to minimize PCB design area and external component requirement.

2. FEATURES

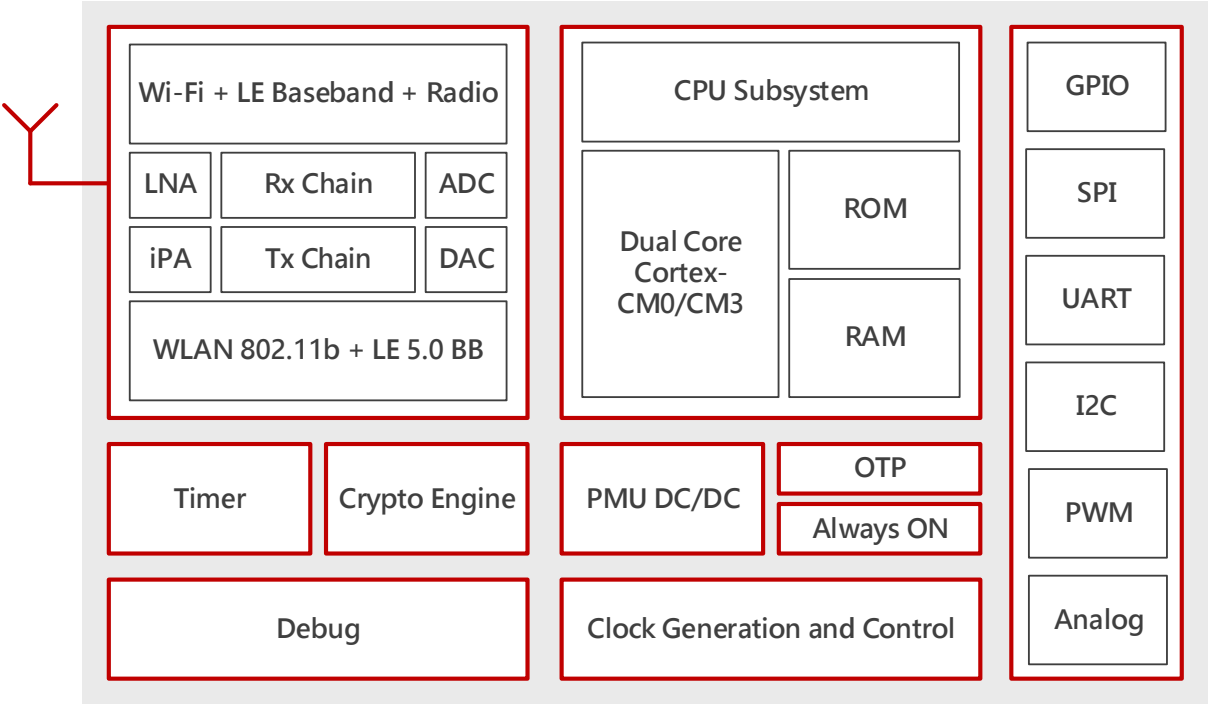
The OPL1000 complies with ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

- Processors
 - ARM® Cortex®-M3 Application Processor
 - ARM® Cortex®-M0 Link Controller
- Wi-Fi
 - 802.11 b up to 11Mbps
 - Supports STA mode
 - WPA/WPA2 security supported
 - Automatic beacon scanning and discovery
 - Built-in TCP/IP stack
- Bluetooth Smart
 - Compliant with Bluetooth 5.0 BLE specifications w/ 2Mbps rate capability
 - Supports Slave Mode
 - Built-in BLE stack
 - All GATT-based profiles supported
- HW Crypto Engine
 - AES-128/256 bits Encryption
 - P-256 ECDH (Elliptic Curve Diffie-Hellman) Key Generation
 - SHA2
 - TRNG
- Power Management
 - Integrated Buck DC-DC converter
- General Purpose, Capture and Sleep timers
- FW OTA (Over-The-Air) update support
- Digital Interfaces
 - General purpose I/Os: 24
 - Two UARTs with hardware flow control up to 3Mbps
 - Three SPI+™ interfaces
 - One I2C bus at 100 kHz, 400 kHz

- Analog Interfaces
 - 10-bit Auxiliary ADC inputs up to 16 channels
 - Four 16mA LED drivers
 - Six PWMs
- Radio Transceiver
 - Fully integrated 2.4 GHz CMOS transceiver
 - Single wire antenna: no external matching and no external T/R switch required
- Package
 - 48-pin QFN, 6 mm x 6 mm

3. BLOCK DIAGRAM

Figure 1: OPL1000 Block Diagram

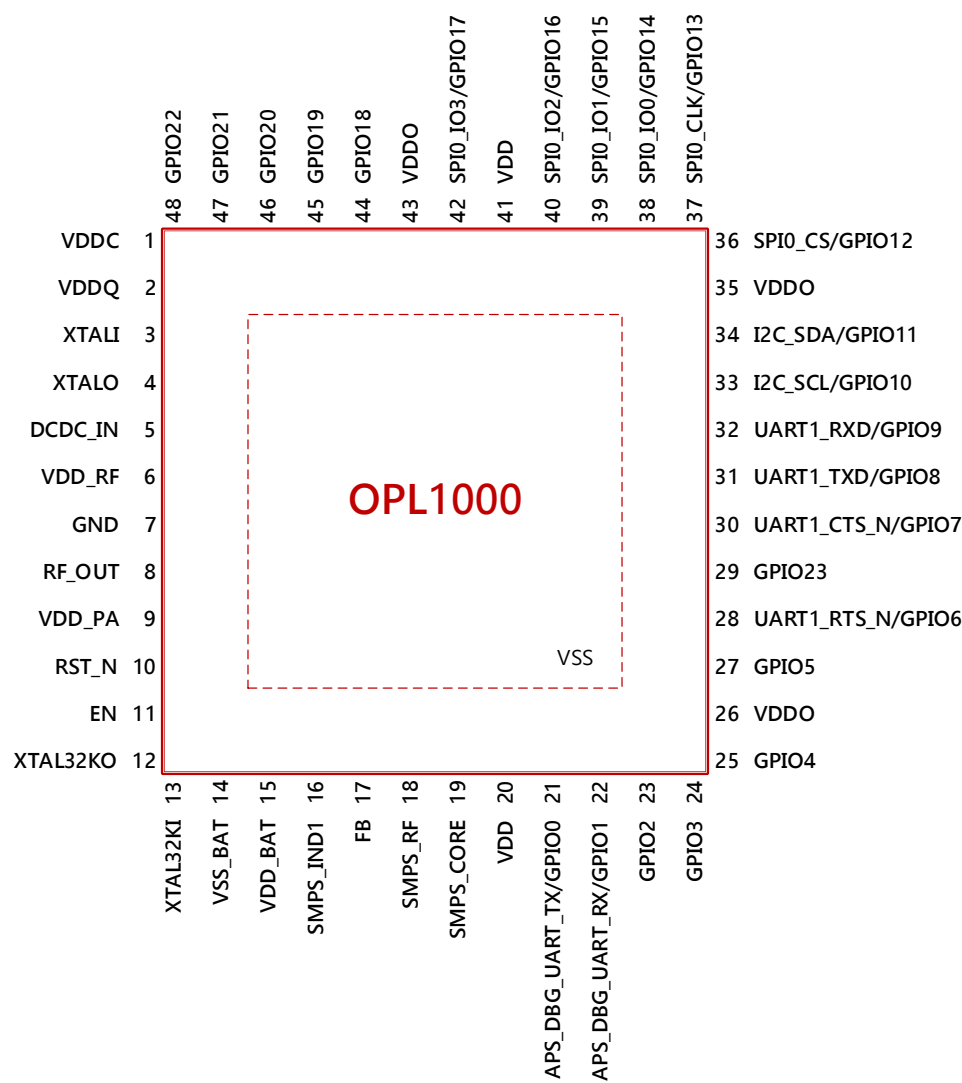


4. PIN DEFINITIONS

4.1. Pin Layout

Figure 2 lists the pin-out assignments for the 48-pin QFN package.

Figure 2: OPL1000 Pin Layout



4.2. Pin Description

The table below lists the pin name and functional descriptions of the OPL1000.

Table 1: OPL1000 Pin Description

| Pin Name | Type | Location | Function Description |
|--------------------------------------|------|----------|--|
| VDDC | P | 1 | Digital core power output |
| VDDQ | P | 2 | OTP power supply for programming mode |
| XTALI | I | 3 | External crystal input pin |
| XTALO | O | 4 | External crystal output pin |
| DCDC_IN | P | 5 | Analog LDO supply input |
| VDD_RF | P | 6 | RF LDO output. Connects with external capacitor to ground. |
| GND | P | 7 | Ground |
| RF_OUT | IO | 8 | RF input/output with on-chip T/R switch |
| VDD_PA | P | 9 | PA power supply with external capacitor |
| RST_N | I | 10 | Reset input signal |
| EN | I | 11 | Enable input |
| XTAL32KO | O | 12 | External 32K crystal output pin |
| XTAL32KI | I | 13 | External 32K crystal input pin |
| VSS_BAT | G | 14 | Ground |
| VDD_BAT | P | 15 | Power supply |
| SMPS_IND1 | P | 16 | DC-DC power converter inductor pin |
| FB | I | 17 | Feedback pin |
| SMPS_RF | P | 18 | DC-DC converter output |
| SMPS_CORE | P | 19 | DC-DC converter output |
| VDD | P | 20 | Digital core power |
| APS_DBG_UART_TX / GPIO0 ⁺ | IO | 21 | APS UART serial data transmit |

| Pin Name | Type | Location | Function Description |
|---|------|----------|---|
| APS_DBG_UART_RX / GPIO1 [†] | IO | 22 | APS UART serial data receive |
| GPIO2 [†] | IO | 23 | General Purpose Input/Output |
| GPIO3 [†] | IO | 24 | General Purpose Input/Output |
| GPIO4 [†] | IO | 25 | General Purpose Input/Output |
| VDDO | P | 26 | Power supply for IO pad |
| GPIO5 [†] | IO | 27 | General Purpose Input/Output |
| UART1_RTS_N / GPIO6 [†] | IO | 28 | UART Request to Send (default) / General Purpose Input/Output |
| GPIO23 [†] | IO | 29 | General Purpose Input/Output |
| UART1_CTS_N / GPIO7 [†] | IO | 30 | UART Clear to Send (default) / General Purpose Input/Output |
| UART1_TXD / GPIO8 [†] | IO | 31 | UART serial data transmit (default) / General Purpose Input/Output |
| UART1_RXD / GPIO9 [†] | IO | 32 | UART serial data receive (default) / General Purpose Input/Output |
| I2C_SCL / GPIO10 [†] | IO | 33 | I2C serial clock line (default) / General Purpose Input/Output |
| I2C_SDA / GPIO11 [†] | IO | 34 | I2C serial data line (default) / General Purpose Input/Output |
| VDDO | P | 35 | Power supply for IO pad |
| SPI0_CS / GPIO12 [†] | O | 36 | SPI Chip Select (default) / General Purpose Input/Output |
| SPI0_CLK / GPIO13 [†] | O | 37 | SPI serial clock (default) / General Purpose Input/Output |
| SPI0_IO0 / GPIO14 [†] | IO | 38 | SPI input/output (default) / General Purpose Input/Output |
| SPI0_IO1 / GPIO15 [†] | IO | 39 | SPI input/output (default) / General Purpose Input/Output |
| SPI0_IO2 / GPIO16 [†] | IO | 40 | SPI input/output (default) / General Purpose Input/Output |

| Pin Name | Type | Location | Function Description |
|-----------------------------------|------|----------|--|
| VDD | P | 41 | Digital core power |
| SPI0_IO3 / GPIO17 [†] | IO | 42 | SPI input/output (default) / General Purpose Input/Output |
| VDDO | P | 43 | Power supply for IO pad |
| GPIO18 [†] | IO | 44 | General Purpose Input/Output |
| GPIO19 [†] | IO | 45 | General Purpose Input/Output |
| GPIO20 [†] | IO | 46 | General Purpose Input/Output |
| GPIO21 [†] | IO | 47 | General Purpose Input/Output |
| GPIO22 [†] | IO | 48 | General Purpose Input/Output |
| VSS | P | E-Pad | Common Ground |

[†] Multi-function pins. Please refer to the Pin Multiplexing Table below for the multi-functions provided.

Table 2: OPL1000 Pin Multiplexing Table

| Pin | Loc. | Signal Name | Signal Dir. | Signal Description |
|-------|------|------------------|-------------|---|
| GPIO0 | 21 | SPI2_IO3 | IO | SPI input/output |
| | | I2C_SCL | IO | I2C serial clock line |
| | | UART0_CTS_N | I | UART Clear to Send |
| | | UART1_TXD | O | UART serial data transmit |
| | | APS_DBG_UART_TXD | O | APS UART serial data transmit for debug |
| GPIO1 | 22 | SPI2_IO2 | IO | SPI input/output |
| | | I2C_SDA | IO | I2C serial data line |
| | | UART0_RTS_N | O | UART Request to Send |
| | | UART1_RXD | I | UART serial data receive |
| | | APS_DBG_UART_RXD | I | APS UART serial data receive for debug |
| GPIO2 | 23 | SPI2_IO1 | IO | SPI input/output |
| | | SPI2_MISO | I | SPI Master Input Slave Output |
| | | I2C_SDA | IO | I2C serial data line |
| | | UART0_TXD | O | UART serial data transmit |
| GPIO3 | 24 | SPI2_IO0 | IO | SPI input/output |
| | | SPI2_MOSI | O | Master Output Slave Input |
| | | I2C_SCL | IO | I2C serial clock line |
| | | UART0_RXD | I | UART serial data receive |
| GPIO4 | 25 | SPI2_CLK | O | SPI serial clock |
| | | I2C_SCL | IO | I2C serial clock line |
| | | UART1_TXD | O | UART serial data transmit |
| GPIO5 | 27 | SPI2_CS | O | SPI Chip Select |
| | | I2C_SDA | IO | I2C serial data line |
| | | UART1_RXD | I | UART serial data receive |
| GPIO6 | 28 | SPI1_CS | O | SPI Chip Select |
| | | I2C_SCL | IO | I2C serial clock line |

| Pin | Loc. | Signal Name | Signal Dir. | Signal Description |
|--------|------|-------------|-------------|-------------------------------|
| GPIO7 | 30 | UART1_RTS_N | O | UART Request to Send |
| | | UART0_TXD | O | UART serial data transmit |
| | | SPI1_CLK | O | SPI serial clock |
| | | I2C_SDA | IO | I2C serial data line |
| | | UART1_CTS_N | I | UART Clear to Send |
| GPIO8 | 31 | UART0_RXD | I | UART serial data receive |
| | | SPI1_IO0 | IO | SPI input/output |
| | | SPI1_MOSI | O | Master Output Slave Input |
| | | I2C_SDA | IO | I2C serial data line |
| | | UART0_CTS_N | I | UART Clear to Send |
| GPIO9 | 32 | UART1_TXD | O | UART serial data transmit |
| | | SPI1_IO1 | IO | SPI input/output |
| | | SPI1_MISO | I | SPI Master Input Slave Output |
| | | I2C_SCL | IO | I2C serial clock line |
| | | UART0_RTS_N | O | UART Request to Send |
| GPIO10 | 33 | UART1_RXD | I | UART serial data receive |
| | | SPI1_IO2 | IO | SPI input/output |
| | | I2C_SCL | IO | I2C serial clock line |
| | | UART0_TXD | O | UART serial data transmit |
| GPIO11 | 34 | UART1_RXD | I | UART serial data receive |
| | | SPI1_IO3 | IO | SPI input/output |
| | | I2C_SDA | IO | I2C serial data line |
| | | UART0_RXD | I | UART serial data receive |
| GPIO12 | 36 | UART1_TXD | O | UART serial data transmit |
| | | SPI0_CS | O | SPI Chip Select |
| | | I2C_SCL | IO | I2C serial clock line |
| | | UART1_CTS_N | I | UART Clear to Send |
| | | UART0_TXD | O | UART serial data transmit |

| Pin | Loc. | Signal Name | Signal Dir. | Signal Description |
|--------|------|-------------|-------------|-------------------------------|
| GPIO13 | 37 | SPIO_CLK | O | SPI serial clock |
| | | I2C_SDA | IO | I2C serial data line |
| | | UART1_RTS_N | O | UART Request to Send |
| | | UART0_RXD | I | UART serial data receive |
| GPIO14 | 38 | SPIO_IO0 | IO | SPI input/output |
| | | SPIO_MOSI | O | Master Output Slave Input |
| | | I2C_SDA | IO | I2C serial data line |
| | | UART1_TXD | O | UART serial data transmit |
| GPIO15 | 39 | SPIO_IO1 | IO | SPI input/output |
| | | SPIO_MISO | I | SPI Master Input Slave Output |
| | | I2C_SCL | IO | I2C serial clock line |
| | | UART1_RXD | I | UART serial data receive |
| GPIO16 | 40 | SPIO_IO2 | IO | SPI input/output |
| | | I2C_SCL | IO | I2C serial clock line |
| | | UART0_TXD | O | UART serial data transmit |
| | | UART1_RXD | I | UART serial data receive |
| GPIO17 | 42 | SPIO_IO3 | IO | SPI input/output |
| | | I2C_SDA | IO | I2C serial data line |
| | | UART0_RXD | I | UART serial data receive |
| | | UART1_TXD | O | UART serial data transmit |
| GPIO18 | 44 | UART1_TXD | O | UART serial data transmit |
| | | PWM5 | O | Pulse-width modulated O/P |
| | | I2C_SDA | IO | I2C serial data line |
| | | UART0_CTS_N | I | UART Clear to Send |
| | | SPI2_CS | O | SPI Chip Select |
| GPIO19 | 45 | UART1_RXD | I | UART serial data receive |
| | | PWM4 | O | Pulse-width modulated O/P |
| | | I2C_SCL | IO | I2C serial clock line |

| Pin | Loc. | Signal Name | Signal Dir. | Signal Description |
|--------|------|-------------|-------------|-------------------------------|
| GPIO20 | 46 | UART0_RTS_N | O | UART Request to Send |
| | | SPI2_CLK | O | SPI serial clock |
| | | UART0_TXD | O | UART serial data transmit |
| | | PWM3 | O | Pulse-width modulated O/P |
| | | I2C_SCL | IO | I2C serial clock line |
| | | UART1_CTS_N | I | UART Clear to Send |
| | | UART1_RXD | I | UART serial data receive |
| | | SPI2_IO0 | IO | SPI input/output |
| GPIO21 | 47 | SPI2_MOSI | O | Master Output Slave Input |
| | | UART0_RXD | I | UART serial data receive |
| | | PWM2 | O | Pulse-width modulated O/P |
| | | I2C_SDA | IO | I2C serial data line |
| | | UART1_RTS_N | O | UART Request to Send |
| | | UART1_TXD | O | UART serial data transmit |
| | | SPI2_IO1 | IO | SPI input/output |
| | | SPI2_MISO | I | SPI Master Input Slave Output |
| GPIO22 | 48 | SPI2_IO2 | IO | SPI input/output |
| | | PWM1 | O | Pulse-width modulated O/P |
| | | I2C_SDA | IO | I2C serial data line |
| | | UART1_TXD | O | UART serial data transmit |
| GPIO23 | 29 | SPI2_IO3 | IO | SPI input/output |
| | | PWM0 | O | Pulse-width modulated O/P |
| | | I2C_SCL | IO | I2C serial clock line |
| | | UART1_RXD | I | UART serial data receive |

For detailed configuration, please refer to the application note.

5. FUNCTIONAL DESCRIPTIONS

5.1. CPU and Memory

5.1.1. CPU

The OPL1000 contains two low-power ARM® 32-bit Cortex-M0/M3 microprocessors with the following features:

- 3-stage pipeline to support clock frequencies up to 176 MHz
- 16/32-bit Instruction Set to provide high code-density
- 32 interrupt vectors from 64 interrupt sources

Main CPU interfaces include:

- Cortex-M0/M3 RAM/ROM Interface for instruction and data
- Cortex-M0/M3 AHB/APB Interface for fast peripheral access
- Interrupt with external and internal sources
- SWD (Serial Wire Debug) interface for debugging

5.1.2. External Flash

The OPL1000 supports 4 x 16 MB of external QSPI Flash with hardware encryption based on AES to protect developer's programs and data.

The OPL1000 accesses external QSPI Flash through a high speed, quad-line SPI interface with the following features:

- Up to 16MB of external Flash are memory mapped into the CPU code space, with 8-, 16- and 32-bit accesses supported for code execution
- Up to 8MB of external Flash/SRAM are memory mapped into the CPU data space, with 8-, 16- and 32-bit accesses supported for data read on Flash/SRAM and data write on SRAM

5.2. Timer

5.2.1. 32-bit Timer

There are two general-purpose timers embedded in the OPL1000.

The timers include the following features:

- A 32-bit time-base counter
- Count down time-base counter
- Halt and resume of time-base counter
- Interrupt held until cleared
- Software-controlled instant reload
- Interrupt generation

5.2.2. Watch Dog Timer

The OPL1000 has two watchdog timers: one in Cortex-M0 and the other in Cortex-M3. These watchdog timers are provided for recovery from an unforeseen fault causing the application program to abandon its normal sequence. The watchdog timers are based on a 32-bit down-counter that is initialized from the Reload Register. A timeout value can be set for each system individually.

If the interrupt is not cleared by the time the counter reaches the count value of zero, the watchdog module asserts the reset signal.

The OPL1000 watchdog timers have the following features:

- Two system watchdogs, each can be configured or disabled separately
- Programmable time period for each system
- 32-bit counter

If the boot process from an SPI Flash does not complete within a predetermined time period, the watchdog will reboot the entire system.

5.3. Radio

The OPL1000 radio consists of the following main blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter

5.4. Wi-Fi Media Access Controller (MAC)

MAC controls the transmission and reception of 802.11 frames.

Supported features include:

- 802.11b features
- Station (STA) mode
- Infrastructure mode
- Passive & active scanning
- RTC/CTS, NAV, IFS, TSF
- Power save mode
- MIB statistics

5.5. Wi-Fi PHY

PHY interacts with the 2.4GHz radio and the MAC engine. It processes data from the MAC engine to make them better adapted to the channel condition for transmission. On the receive side, PHY is responsible for recovering and decoding the receive data with all sorts of channel impairments.

Supported features include:

- Long & optional short 802.11b preambles
- Automatic Gain Control (AGC)
 - Channel quality statistics

5.5.1. Wi-Fi Firmware

The OPL1000 Wi-Fi Firmware provides the following functions:

- Infrastructure BSS Station mode support
- WPA/WPA2-Personal

5.6. Bluetooth Low Energy

The OPL1000 integrates Bluetooth Low Energy (LE) link controller and Bluetooth baseband, which carry out the baseband protocols and other low-level link routines, such as modulation/demodulation, packet processing, bit stream processing, frequency hopping, etc.

5.6.1. Bluetooth Low Energy Radio and Baseband

The OPL1000 LE Radio and Baseband support the following features:

- Bluetooth Link Controller
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening, and transmit pulse shaping
- AFH
- Power management for low power applications
- SMP with 128-bit and 256-bit AES

5.6.2. Bluetooth Interface

The OPL1000 Bluetooth interface provides an interface to UART HCI.

5.6.3. Bluetooth Stack

The Bluetooth stack of the OPL1000 is compliant with Bluetooth v5.0 BLE specifications.

5.6.4. Bluetooth Link Controller

The link controller supports up to eight LE links. Supported features include:

- Advertising
- Multiple connections
- Asynchronous data reception and transmission
- Adaptive frequency hopping and channel assessment
- Connection parameter update
- Data length extension
- Link layer encryption
- LE Ping

5.7. Network Stack Support

The OPL1000 has all necessary network stacks embedded, including:

- TCP/UDP/IPv4/IPv6
- ICMP/ARP
- IGMP
- DNS client / DHCP client / HTTP client
- TLS
- SNTP/TFTP
- Socket interface

6. INTERFACES

The OPL1000 provides various control interfaces for easy access to network stack from customer applications.

6.1. General Purpose Input/Output (GPIO)

Twenty-four (24) General Purpose IO pins are provided for various peripheral and input or output functions configurable by control registers.

6.2. Peripheral Transport Subsystem (PTS)

Functions supported in this module include UART, Serial Peripheral Interface (SPI), I2C, and Pulse Width Modulation (PWM).

6.2.1. UART

The UART transport supports baud rates of 9600, 14400, 19200, 38400, 57600, 115200, 230400, 460800, 921600, and 1500000 bps.

While auto-baud is not needed, the hardware flow control signals RTS & CTS should be supported. The UART should operate correctly with the external UART so long as the combined baud rate error of the two devices is within $\pm 5\%$.

Note that, to support firmware code download in production line, the UART IO signals should not be shared with the SPI IO signals.

6.2.2. Serial Peripheral Interface (SPI)

There are three SPI interfaces supported in the OPL1000. These SPI interfaces each support master modes at a maximum speed of 44 Mbps, a four-signal interface, and quad-data lines (six-signal line) for high throughput transfer.

One default SPI is used to interface to external flash for firmware/application code download.

In Quad mode operation, four bits are used for output and input simultaneously, and the most significant bit (MSB) is always `sdataOut[3]/sdataIn[3]`. In Dual mode operation, two bits are used for output and input simultaneously, and the most significant bit (MSB) is always `sdataOut[1]/sdataIn[1]`. In single bit operation, only `sdataOut[0]` and `sdataIn[0]` are used.

Example quad-SPI flash devices include SST26VF016/SST26VF032, MPC5606S/MPC5645S, and N25Q128A.

6.2.2.1. External Serial Flash

In one usage case, firmware boot code determines if valid code and system configuration are stored in the serial flash before loading them to internal SRAM for execution. If there is no valid signature in the serial flash, code download from an external host to the serial flash can occur if the UART interface is detected and correct escape sequence received from it. In the OPL1000 MP chip, internal ROM will contain valid code so that the external serial flash will only contain customer application code and maybe system static and dynamic configuration information as well.

The OPL1000 provides native support for flash devices including but not limited to the following:

- Atmel®: AT25BCM512B
- MXIC®: MX25V512ZUI-20G
- MXIC®: MX25V8035F
- GIGA-DEVICE®: GD25Q80C
- WINBOND®: W25Q80DV

6.2.2.2. External Display Controller

SPI should be able to run at 10Mbps or above to support for example the Apple Watch OLED type graphic display having 312x390 pixels at 24-bit per/pixel. Three- or Four-wire SPI may be needed for this SSD1355 Solomon System.

6.2.3. I2C

The two-wire I2C serial interface consists of a serial data line (SDA) and a serial clock (SCL) supporting both master mode and slave mode.

6.2.3.1. Features

The I2C supports the following features:

- Three speeds: Standard mode (0 to 100 kb/s), Fast mode (≤ 400 kb/s), and High-speed mode (≤ 3.4 Mb/s)
- 7- or 10-bit addressing

6.2.3.2. Definition of Bits in First Byte

Table 3: Definition of Bits in First Byte

| Slave Address | R/W Bit | Description |
|---------------|---------|---|
| 0000 000 | 0 | General Call Address to store data in the receive buffer and to issue a General Call interrupt. |
| 0000 000 | 1 | START byte. |
| 0000 001 | X | CBUS address. DW_apb_i2c ignores these accesses. |
| 0000 010 | X | Reserved. |
| 0000 011 | X | Reserved. |
| 0000 1xx | X | High-speed master code. |
| 1111 1xx | X | Reserved. |
| 1111 0xx | X | 10-bit slave addressing. |

6.2.4. AUXADC

The OPL1000 contains a 10-bit ADC supporting 16 analog channels – these channels share IO pins with digital GPIOs. Taking ADC sample is controlled by internal firmware driver with the setting of the start conversion signal and with the subsequent reading of the ADC output sample when conversion is completed. Periodic sampling is supported by firmware through the same procedure mentioned above. Besides the 16 analog channels, the ADC can also measure internal reference voltages for calibration purpose. If system battery voltage is fed to VDD_BAT pin, then it can be measured as one internal reference, and the battery level reading can be obtained without using any of the 16 analog channels.

6.2.5. Pulse Width Modulation (PWM)

There are six PWM channels supported in the OPL1000, each with 10 bits to support 1/1000 resolution. The PWM uses baseband LPO clock as the clock source, and can perform LED flashing and other control functions where the flashing (ramp up/down) can be disabled.

There are two operation modes: regular PWM and LED flashing. The latter contains the following states:

- Dull state:
LED shows the lowest brightness; one extreme of this state is the case where the PWM remains in idle state with a constant zero outputted.
- Ramp up state:
LED goes between the highest and the lowest brightness, the PWM output duty cycle increases in delta units, hence the brightness of the LED.
- Bright state:
LED shows the highest brightness, and stays that way until a programmable brightness is set.
- Ramp down state:
LED goes between the highest and the lowest brightness, the PWM output duty cycle decreases in delta units, hence the brightness of the LED.

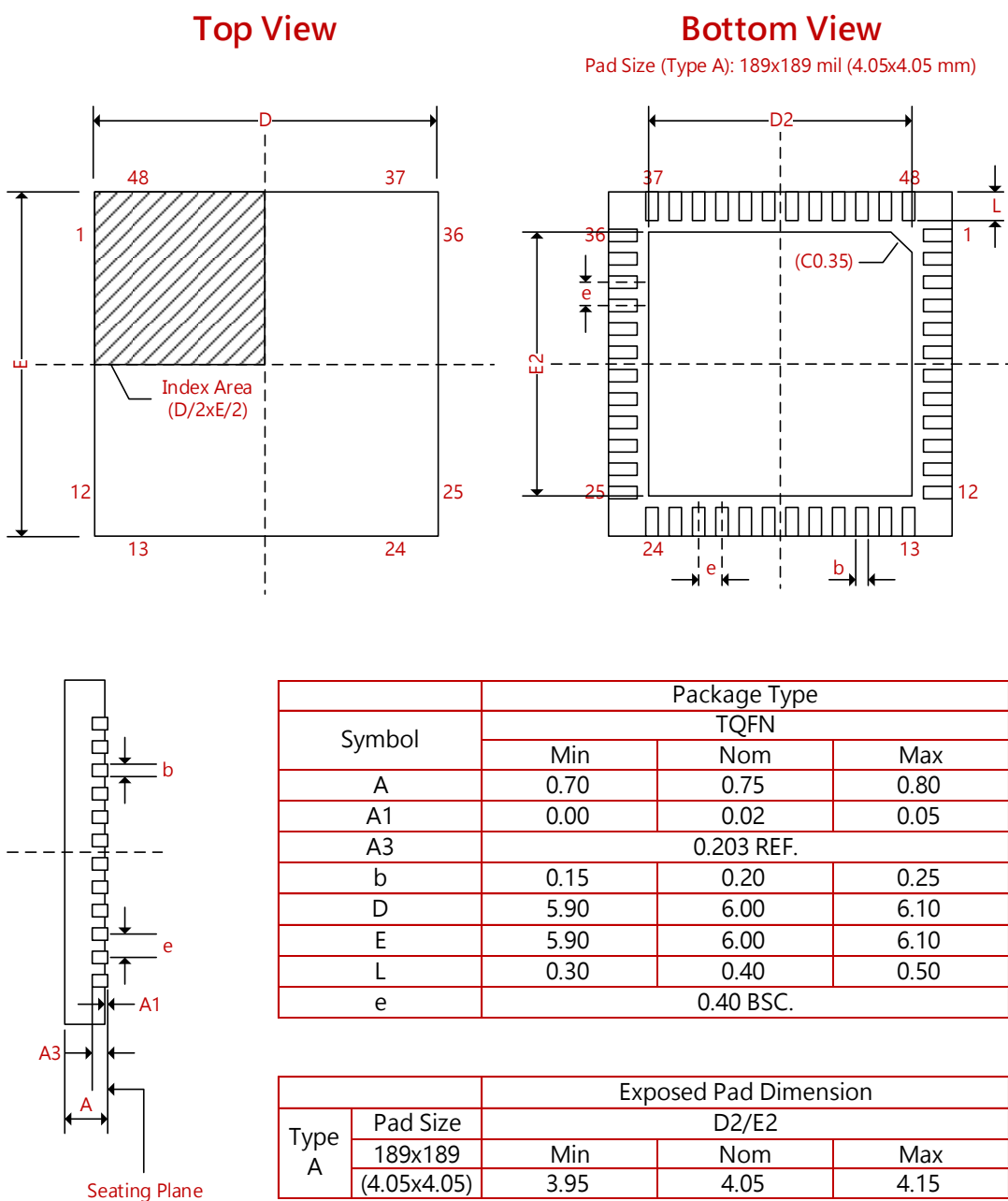
7. SECURITY

Industry leading hardware-based security accelerator is included in the OPL1000. The supported features include the following:

- Software API support:
 - AES Encryption/Decryption
 - AES-CMAC
 - AES CCM
 - TRNG
 - ECDH Key Pair Generation
 - DH Key
 - HMAC-SHA1
 - SHA2
- Wi-Fi security support:
 - 802.11i-2007
 - WPA-PSK (TKIP) / WPA2-PSK (AES) / Mix Mode
- LE security support:
 - Security manager
 - Improved privacy with low power consumption (LE Privacy 1.2 and Secure Connections)
 - P256 Key Pair (ECDH Key Pair)

8. PACKAGE INFORMATION

Figure 3: OPL1000 QFN48 Packaging Drawing



9. ORDERING INFORMATION

| Part Number | Package | Description | Ambient Operating Temperature |
|---------------------------|-----------|--|-------------------------------|
| OPL1000TKQGT [†] | 6x6mm QFN | 2.4GHz single band Wi-Fi 802.11b+LE 5.0 | -30 to 70°C |

[†] "T" for "Tape & Reel"

CONTACT

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