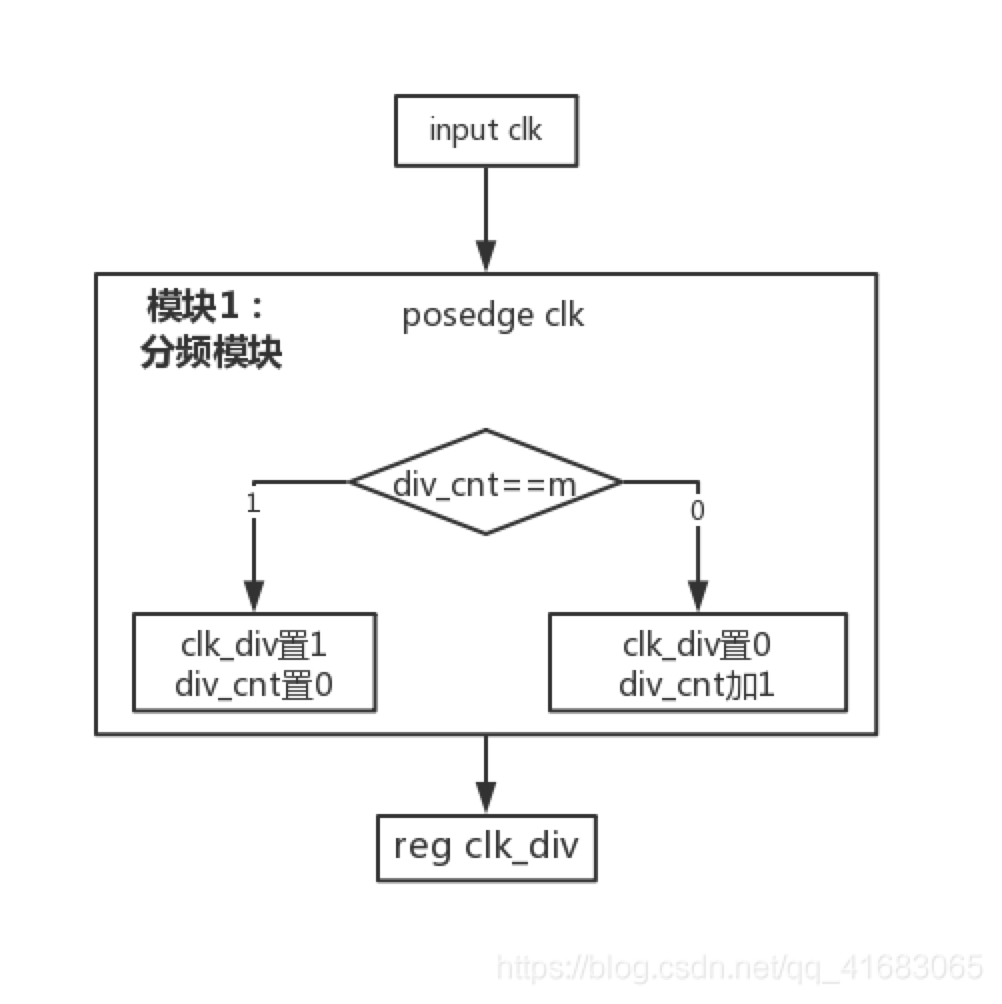
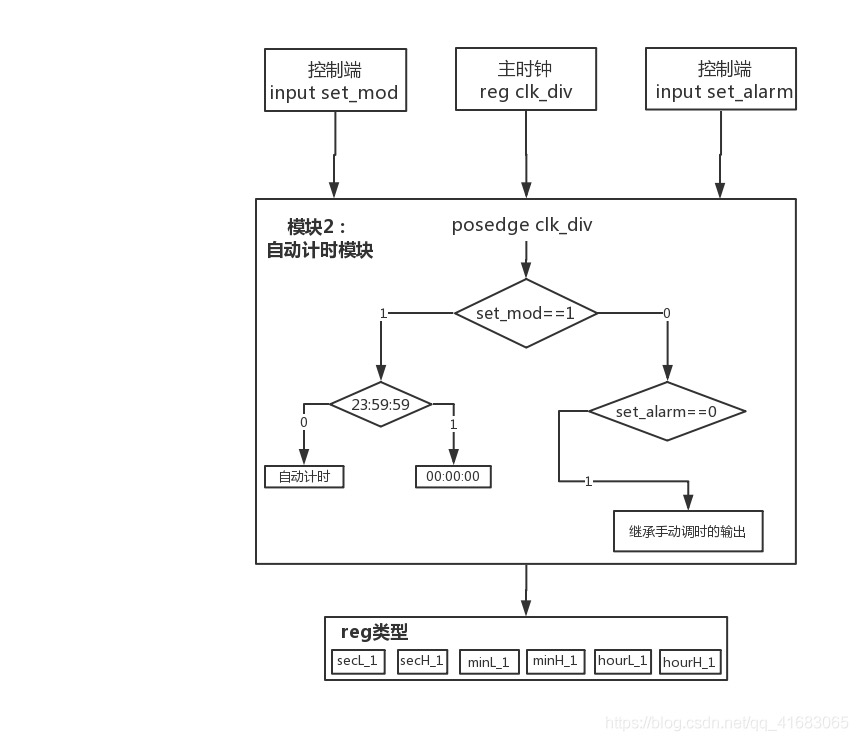
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| --- | --- | --- | --- | --- | --- |
| **学 期** | 2020-2021第一学期 | **班 级** | 190741 | **组 号** | 24 |
| **学 院** | 计算机学院 | **学 号** | 19030419 | **姓 名** | 王昕 |
| **专 业** | 计算机类 | **学 号** | 19074104 | **姓 名** | 王佳玮 |
| **题 目** | 实验12：实用电路 | | | | |

1. **原理**





1. **电路实现（电路图或Verilog程序）**

Verilog程序代码：

module clock\_074124(clk\_50mhz,en,set,clr,swc,swr,a,b,c,d,e,f,g,ds

,s0,s1,m0,m1,h0,h1,data,s,m,h,s\_in,m\_in,h\_in

);

output [3:0]s0,s1,m0,m1,h0,h1,data;

output [5:0]s,m,h,s\_in,m\_in,h\_in;

input clk\_50mhz,en,set,clr;

input [3:0]swc;

output a,b,c,d,e,f,g;

output [3:0]swr;

output [7:0]ds;

wire clk\_1hz,clk\_50hz;

wire [2:0]select;

wire [3:0]s0,s1,m0,m1,h0,h1,data,data\_time,data\_set,key,key\_temp,swr,key0,key1,key2,key3,key4,key5,key6,key7;

wire [5:0]s,m,h,s\_in,m\_in,h\_in,s\_set,m\_set,h\_set,s\_last,m\_last,h\_last;

wire [7:0]ds;

parameter zero=0;

frequency\_divider\_074124 (clk\_50mhz,en,clk\_1hz,,clk\_50hz,);

jpsm\_074124 (clk\_50hz,set,swc,key\_temp,swr,);

jpfd\_074124 (clk\_50hz,set,key\_temp,key,flag);

shift\_register\_8\_074124 (flag,set,key,,1'b0,1'b1,,,,,,,,,key0,key1,key2,key3,key4,key5,key6,key7);

multiplexers\_074124(data\_set,set,select,key0,key1,key2,key3,key4,key5,zero,zero);

decoder\_074124 (key4,key5,h\_set);

decoder\_074124 (key2,key3,m\_set);

decoder\_074124 (key0,key1,s\_set);

assign s\_in=(set?s\_set:s\_last);

assign m\_in=(set?m\_set:m\_last);

assign h\_in=(set?h\_set:h\_last);

timecounter\_074124 (en,clr,s,m,h,clk\_50mhz,s\_in,m\_in,h\_in);//实验用1hz

assign s\_last=s;

assign m\_last=m;

assign h\_last=h;

encoder\_074124 (s,s0,s1);

encoder\_074124 (m,m0,m1);

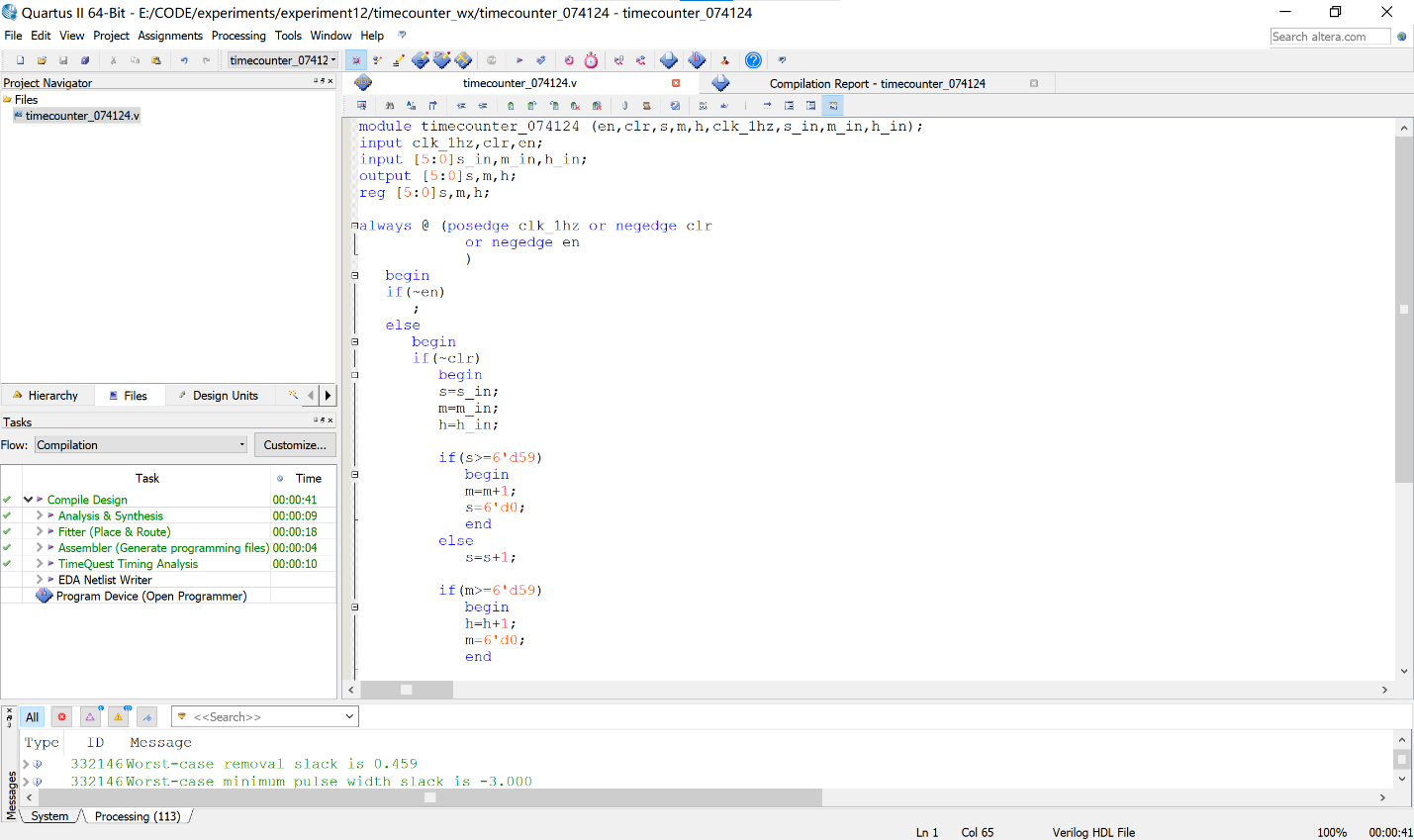
encoder\_074124 (h,h0,h1);

multiplexers\_074124(data\_time,en&(~set),select,s0,s1,m0,m1,h0,h1,zero,zero);

dtsm\_074124(clk\_50mhz,ds,select);//实验用1khz

assign data=(set?data\_set:data\_time);

led\_g074124 (data,a,b,c,d,e,f,g);

endmodule

顶层模块