Jennifer Brana

Undergraduate, University of Portland

brana23@up.edu | jenniferbrana.github.io | JenniferBrana | jenniferbrana

Research Interests

My research interests lie in computer architecture and sustainable computing, particularly the design of heterogeneous architectures and memory systems.

Research areas: computer architecture; heterogeneous architectures; memory system design; caching; sustainability.

Education

University of Portland — *Portland, OR*

B.S. in Computer Science — *Aug. 2019 - PRESENT*

- Minor in Computer Engineering.

Professional Experience

Computer Organization Research Group (CORGi) — *Carnegie Mellon University*

Undergraduate Research Assistant — *May 2022 - Present*

- Designed novel non-inclusive hierarchical cache coherence protocol to simplify the integration of cache-attached accelerators.
- Researched methods to reduce the verification complexity and minimize the impact of accelerator integration in the cache hierarchy.
- Verified protocols using the Murphi model checker and built discrete-event cache simulator using Python to model protocol behaviour.
- Generated fully concurrent protocols using HieraGen then implemented protocols in cycle-level simulator for performance analysis.

Team Lift — *Portland, OR*

Senior Capstone — *Aug. 2022 - Present*

- Worked in a team of five students to design a cyber-physical system to monitor and control an irrigation system in Karonga, Malawi.
- Explored methods to deploy and connect a network of sensors and computation nodes in an environment lacking basic infrastructure.

University of Portland — *Portland, OR*

Research Assistant — *Jan. 2022 - May 2022*

- Investigated CPU specialization methods to increase the performance and efficiency of Viterbi Decoding.
- Simulated processor architecture using gem5 and modeled processor power consumption using McPat.
- Performed low-level algorithm optimizations using RISC-V assembly language and in-line assembly.

University of Portland — *Portland, OR*

Undergraduate Research Assistant — *May 2021 - August 2021*

- Researched EEG-based view of comprehension of truth statements to understand how humans process undefined statements.
- Assembled hardware framework for conducting experiments and developed synchronization mechanisms for system components.

ConnectPV — *San Diego, CA*

Engineering/Operations Intern — *May 2020 - August 2020*

- Designed parts and product drafts for solar combiner boxes using SolidWorks.
- Analyzed product line capabilities and communicated with suppliers to implement a new Materials Requirements Planning system.

Publications

Kobold: Simplified Cache Coherence for Cache-Attached Accelerators — *WDDSA @ MICRO 2022*

Jennifer Brana, Brian C. Schwedock, Yatin A. Manerkar, Nathan Beckmann

Talks and Posters

Kobold: Simplified Cache Coherence for Cache-Attached Accelerators — *WDDSA @ MICRO, 2 Oct. 2022*

Kobold: Simplified Cache Coherence for Cache-Attached Accelerators — *SRC @ MICRO, 3 Oct. 2022*

Comparison of Computer Architecture Specialization Methods for Performance and Power Efficiency — *University of Portland Founders' Day, 12 April 2022*

Service & Leadership

Tau Beta Pi — *University of Portland*

Chapter President — *2021 - 2022*

- Responsible for planning meetings and activities to engage club members ranging from career development to design competitions.

Society of Women Engineers — *University of Portland*

Mentor — *2020 - Present*

- Mentored freshman girls in the engineering program.

Tutoring Working Group — *University of Portland*

Student Representative — *2021*

- Worked with faculty members to redesign the tutoring program for the Shiley School of Engineering following the Covid-19 pandemic to increase freshman and sophomore retention rates.

Teaching

University of Portland

Theory of Computation (CS 357)	*Grader, Fall 2022*
Digital Systems Design (EE 332)	*Tutor, Spring 2022*
Signals & Systems (EE 262)	*Tutor, Spring 2022*
Logic Design (EE 231)	*Grader and Tutor, Fall 2021*
Electrical Circuits (EE 261)	*Tutor, Fall 2021-Spring 2022*
Electrical Circuits Lab (EE 271)	*Lab Assistant, Spring 2021*

Skills

Programming Languages	C, C++, Python, Java, Assembly, MATLAB, Verilog HDL, LaTeX
Parallel Programming	Experience in parallel/GPU computing using CUDA C/C++, OneTBB
Computer Architecture Tools	Experience using gem5, McPat, Murphi model checker, CACTI
Other	Proficiency with Unix, SSH, Git/Github, Xcode, VSCode. Experience in Agile