HW 4

1)

Draw a circuit diagram showing the structural equivalent for each of the two register implementations above. You may use primitives such as the D Flip-Flop, MUX, decoder, and basic logic gates.

6)

Decoder

The decoder selects which register of the register file is being written to. Here is the full definition:

```
module decoder1to32
(
output[31:0]    out,
input           enable,
input[4:0]      address
);
    assign out = enable<<address;
endmodule
```

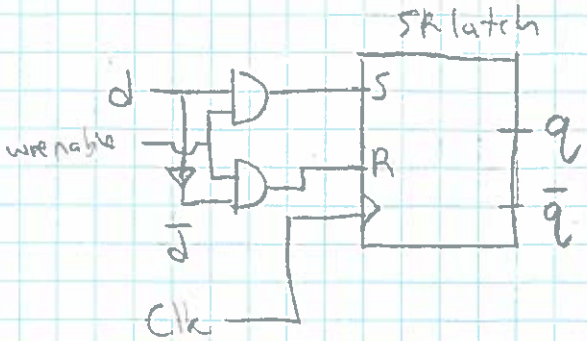
Deliverable 6

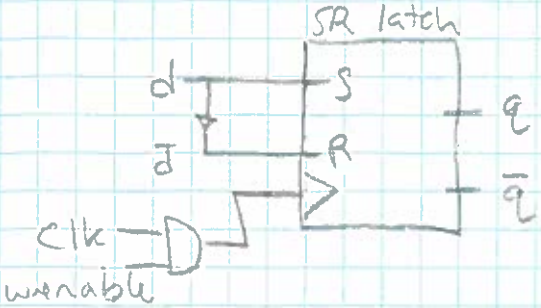
Provide a brief written description of how the above module works. How does this behavioral Verilog result in a decoder?

This module outputs the enable shifted by the magnitude of the address. If enable is on, then the address index will turn on (set equal to 1) only the appropriate register. If enable is off, 0 shifted by some number of zeroes will still leave everything off.

HW4 CompArch

Deliverable 1





DON'T GATE THE CLOCK