Chapter 3 Branch Loop, and IO Port

Andrew Leung

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Sections

- 3.1 Loop and Jump Instructions
- 3.2 IO PORT
- 3.3 Time Delay Generation and Calculation

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Branch instruction and Looping

- Looping in PIC
- Loop inside loop
- Other conditional jumps
- All conditional branches are short jumps
- Calculating the short branch address
- Unconditional branch instruction

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Loop in PIC

- Repeat a sequence of instructions or a certain number of times
- Two ways to do looping
 Using DECFSZ instruction
 Using BNZ\BZ instructions

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DECFSZ instruction Example: Write a program to a)Clear WREG b)Add 3 to WREG ten times and place the result in COUNT EQU 0x25 MOVLW d'10° MOVWF COUNT MOVLW AGAIN ADDLW DECFSZ COUNT, F GOTO AGAIN MOVWF PORTB Andrew Leung

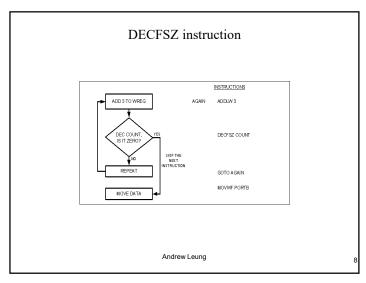
DECFSZ instruction

•Decrement file register, skip the next instruction if the result is equal 0

•DECFSZ fileRef, d

•GOTO instruction follows DECFSZ

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DECFSZ instruction

What is the maximum number of times that the loop in the previous example can be repeated?

Solution:

Since COUNT holds is an 8-bit register, it can hold a maximum of FFH, therefore the loop can be repeated a maximum of 256 times by setting COUNT=0.

Thus, COUNT=0H, FFH, FEH, ..., 2, 1, 0 (total 256 times)

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Using BNZ\BZ

Example:

AGAIN

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Write a program to

a)Clear WREG

b)Add 3 to WREG ten times and place the result in

COUNT EQU 0x25

MOVLW d'10°

MOVWF COUNT MOVLW 0

ADDLW 3

DECF COUNT, F

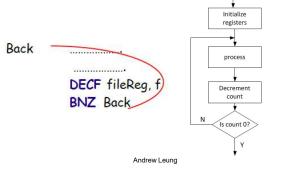
BNZ AGAIN MOVWF PORTB

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Using BNZ\BZ

Supported by PIC18 families Early families such as PIC16 and PIC12 doesn't support these instruction

These instructions check the status flag



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DECFSZ instruction

What is the maximum number of times that the loop in the previous example can be repeated?

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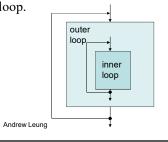
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Nested Loop

- A single loop is repeated 256 times in maximum.
- If we want to repeat an action more times than 256, we use a loop inside a loop.

• This is called nested loop.

- For Example:
 - The inner loop is 256
 - The outer loop is 2
 - Total 256*2=512



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Other Conditional jumps

All of the 10 conditional jumps are 2-byte instructions

•They requires the target address

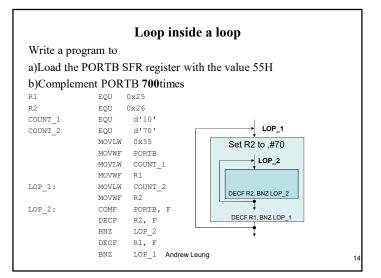
1 byte address (short branch address)

Relative address

- •Recall: MOVF will affect the status Reg.
- •In the BZ instruction, the Z flag is checked. If it is high, that is equal 1, it jumps to the target address.

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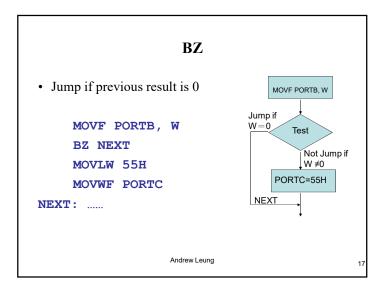


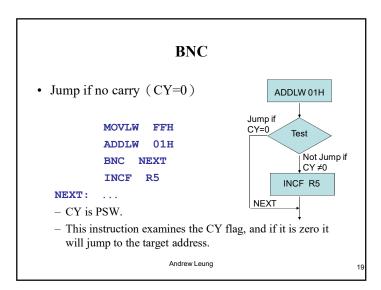
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Flags Bits and Decision

k	Branch relative if Carry
k	Branch relative if Not Carry
k	Branch relative if Negative
k	Branch relative if Not Negative
k	Branch relative if Overflow
k	Branch relative if Not Overflow
k	Branch relative if Zero
k	Branch relative if Not Zero
	k

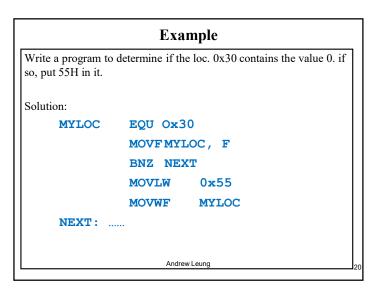
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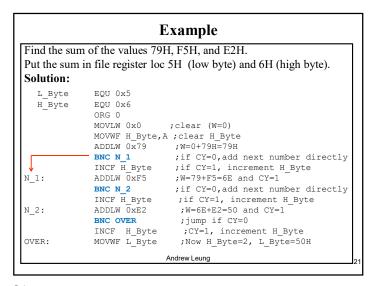




BNZ • Jump if previous is not zero MOVF PORTB, W Jump if MOVF PORTB, W W ≠ 0 BNZ NEXT Not Jump if W = 0 MOVLW 55H PORTC=55H MOVWF PORTC NEXT NEXT: ... - This instruction examines the contents of the ACC and jumps if ACC is not 0.

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Relative Address Calculation in conditional brances
                              Instructions
Example:
       000000 0E00
                             MOVLW 0x0
                     00004
                             MOVWF H_Byte
       000002 6E06
                     00005
       000004 0F79
                     00006
                             ADDLW 0x79
       000006 F301
                     00007
                             BNC N 1
       000008 2A06
                     00008
                             INCF H_Byte,F
       00000A 0FF5
                     00009 N_1 ADDLW 0xF5
       00000C E301
                     00010
       00000E 2A06
                     00011
                             INCF H Byte,F
                     00012 N 2 ADDLW 0xE2
       000010 0FE2
                              BNC OVER
       000012 E301
                     00013
                           INCF H_Byte,F
       000014 2A06
                     00014
                    00015 OVER MOVWF L Byte
       Ω00Ω16, 6Ε05
Why in ROM Loc the content is E301?
Ans:
E3 is opcode for BNC
When CPU is executing BNC N 1, the PC=00008.
The target address is 000A. The difference (000A-0008) is +2. So, the
displacement in instruction is 01.
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```

Relative Address Calculation in conditional brances Instructions

- The conditional jump is a jump in which control is transferred to the target location if it meets the required condition.
 - BZ, BNC...
 - The target address cannot be farther than -256 / +254 from the current program counter

How to know the target address is out of range or not?

Ans: Assembler will tell you

How to solve the problem if our conditional jump needs to

a target address which is farther than -256 / +254 from the program counter.

In condition branch, the instruction is

8 bit Opcode	8 bit signed number (for displacement)

Target address=PC+2 x(8 bit signed number)

The relative displacement is a common used technique in many processor.

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```
Relative Address Calculation in conditional brances
                         Instructions
Example:
0000
       0E00
                      MOVLW 0x0
0002
       6E06
                      MOVWF H Byte, A
0004
      0F79
                     ADDLW 0x79
0006
      E3XX
                      BNC N 1
8000
      0000
000A
       0000
                      NOP
       2A06
                      INCF 0x6, F, ACCESS
000C
000E
       0FF5
                N 1: ADDLW 0xf5
0010
       E301
                      BNC N 2
0012
      2A06
                      INCF 0x6, F, ACCESS
0014
       0FE2
                N 2: ADDLW 0xe2
0016
       E301
                      BNC Over
0018
                      INCF 0x6, F, ACCESS
001A
       6E05 Over: MOVWF 0x5,
000E-0008=06, 6/2=3 \Rightarrow E303
                          Andrew Leuna
```

Relative Address Calculation in conditional brances Instructions Example: 0000 MOVLW 0x0 MOVWF H_Byte, A 0002 6E06 0004 ADDLW 0x79 0006 E303 BNC N 1 0008 000A 000C INCF 0x6, F, ACCESS 000E 0FF5 N 1:ADDLW 0xf5 0010 BNC N_2 0012 INCF 0x6, F, ACCESS 0014 0FE2 N 2:ADDLW 0xe2 0016 BNC N 1 0018 INCF 0x6, F, ACCESS 001A 6E05 Over: MOVWF 0x5, 000E-0018=-10, -10/2=-5, -5 is signed format is FB=>E3FB Andrew Leung

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GOTO

• a 4-byte instruction



The address is A_{20} ----- A_10

• Jump to anywhere in the program memory

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Jump Instructions

The unconditional jump is a jump in which control is transferred unconditionally to the target location. The target address is directly coded in the instruction

•There are two unconditional jumps:

GOTO (Long Jump)BRE (Short Jump)

- Examples in textbook

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BRA

- a 2-byte instruction
 - The first 5 bits are the opcode
 - The next 11 bits form a signed number displacement, which (need to times 2 first) is added to the PC to get the target address.

In condition branch, the instruction is

5 bit Opcode 11 bit signed number (for displacement)

Target address=PC+2 x(11 bit signed number)

Limited range: -2048 to 2046 bytes of the relative address of the current PC value

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CALL and RCALL

- CALL: 4 bytes
 Call a subroutine in anywhere format is similar to GOTO
- RCALL: 2 bytes
 - Call a subroutine who address should be within Similar to BRA
 - Relative address

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The Process of Calling a Subroutine

- After execution of the called subroutine, the CPU must know where to comback to.
- The process of calling a subroutine:
 - A subroutine is called by CALL instructions.
 - The CPU pushes the PC onto the stack (in PIC18 it is a hardware stack).
 - The CPU copies the target address to the PC.
 - The CPU fetches instructions from the new location.
 - When the instruction RETURN is fetched, the subroutine ends.
 - The CPU pops the return address from the stack.
 - The CPU copies the return address to the PC.
 - The CPU fetches instructions from the new location.

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The Flow of Control Involving a Procedure

Calling program unit

Procedure

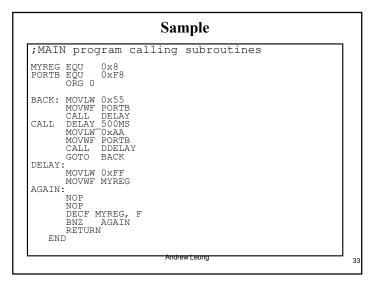
Return

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Sample
; MAIN program calling subroutines $\operatorname{\textsc{ORG}}$ 0
MAIN:
            CALL
                         SUBR 1
            CALL
                         SUBR 2
           SJMP
                          HERE
         end of MAIN
SUBR 1:
           RETURN
        -end of subroutine 1
SUBR 2:
END
             ; end of the Lasm file
```

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PIC18 Parallel Ports • I/O ports are available in PIC18 to interact, monitor and control peripherals. LED 7-Segment LED

Sections

3.1 Loop and Jump Instructions

3.2 IO PORT

3.3 Time Delay Generation and Calculation

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PIC18 Parallel Ports

- The number of ports in the PIC18 family depends on the number of pins on the chip.
- PIC18F4520 has five ports: Port A-E
- Different ports have different number of pins:
 - Port A: 7 pins
 - Port B, C, D: 8 pins
 - Port E: 3 pins

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PIC18 Parallel Ports

- The behaviour of each port is controlled by two special function registers (SFRs):
 - PORTx indicates the voltage levels on the pins of the device
 - TRISx data direction register
- e.g., For Port B, we have PORTB and TRISB

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TRISx and PORTx SFRs

• e.g., output the hex value 0x26 to Port C

clrf TRISC
movlw 0x26
movwf PORTC

• e.g., Read the current value of Port D into WREG register

setf TRISD
movf PORTD, W

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TRISx and PORTx SFRs

- Each of the Ports A-E can be used for input and output.
- TRISx SFR is used for designating the direction of a port
 - 0 for output (e.g., Controlling LED state)
 - 1 for input (e.g., Key scan)
- e.g., To output data to Port B:
 - Write 0s to TRISB SFR
 - Write data to PORTB SFR

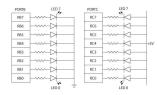
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Interfacing with LED

- Two ways of connecting LEDs to I/O ports:
 - Common Cathode: LED cathodes are grounded and logic 1 from the I/O port turns on the LEDs.
 - Common Anode: LED anodes are connected to the power supply and logic 0 from the I/O port turns on the LEDs.

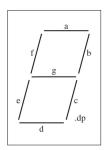


Common Cathode Common Ar Active high Andrew Leung Active low

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Interfacing with 7-Segment LED

- Often used to display BCD numbers (1 through 9) and a few alphabets
- A group of eight LEDs physically mounted in the shape of the number eight plus a decimal point
- Each LED is called a segment and labeled as 'a' through 'g'.



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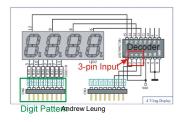
Interfacing with 7-Segment LED · In a common cathode sevensegment LED All cathodes are connected together to ground and the From Data Lines Through an Interfacing Device anodes are connected to data • Logic 1 turns on a segment. Example: To display digit 1, all segments except b and c should be off. Byte 00000110 = 06H will Common Cathode display digit 1. Andrew Leung

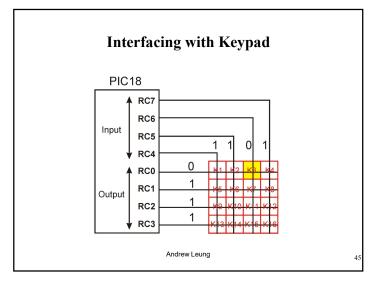
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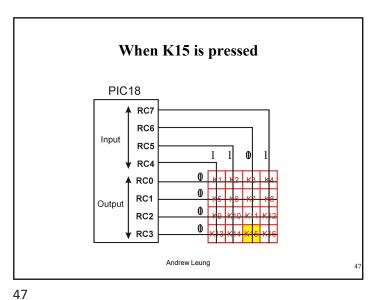
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Interfacing with 4-digit 7-Segment LED

- Decoder selects the position where digit pattern is displayed.
- Use time multiplexing if we need to display all four digits.







When K5 is pressed PIC18 RC6 Input RC5 ₩ RC4 RC0 RC1 Output RC2 ₩ RC3 Andrew Leung

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PICkit3

- Device Programmer Burn assembled code into the device FLASH.
- In-circuit debugger allow real-time interactions with the board even when debugging.



I/O ports and bit-addressability

- Often need to access individual bit of the port instead of the entire 8 bits.
- PIC18 provides instructions that alter individual bits without altering the rest of the bits in the port.
- Most common bit-oriented instructions:

Function Instructions bsf fileReg, bit Bit Set fileReg bcf fileReg, bit Bit Clear fileReg Bit Toggle fileReg btg fileReg, bit Bit test fileReg, skip if clear btfsc fileReg, bit Andrew Bit test fileReg, skip if set btfss fileReg, bit

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Checking the state of an I/O port

- btfsc (bit test file, skip if clear) and btfss (bit test file, skip if set) are used to make branching decision based on the status of a given bit.
- e.g., btfsc PORTD, 2 skips the next instruction if Bit 2 of Port D equals 0.
- e.g., btfss PORTD, 2 skips the next instruction if Bit 2 of Port D equals 1.

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bsf, bcf and btg

- bsf fileReg, bit
 - e.g., bsf PortB, 5 sets Bit 5 of Port B to be 1
- · bcf fileReg, bit
 - e.g., bcf PortB, 5 sets Bit 5 of Port B to be 0.
- · btg fileReg, bit
 - e.g., btg PortB, 5 toggles Bit 5 of Port B (i.e., sets it to 1 if the current value is 0 & vice versa)

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Example: btfss

• e.g., Write a program to (a) keep monitoring RB2 bit until it becomes high (b) When RB2 becomes high, write 45H to Port C

bsf TRISB, 2; set RB2 as input clrf TRISC; set Port C as output movlw 0x45 Again: btfss PORTB, 2 bra Again movwf PORTC

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Example: btfss

- e.g., Write a program to check RB2.
 - If RB2 = 0, send the letter 'N' to Port D
 - If RB2 = 1, send the letter 'Y' to Port D

bsf TRISB, 2; set RB2 as input clrf TRISD; set Port D as output Again: btfss PORTB, 2 bra Over movlw A'Y' movwf PORTD bra Again
Over: movlw A'N' movwf PORTD bra Again
Over: movlw A'N' movwf PORTD bra Again

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Sections

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Example: btfsc

• e.g., Perform the same function using btfsc

bsf TRISB, 2; set RB2 as input clrf TRISD; set Port D as output Again: btfsc PORTB, 2 bra Over movlw A'N' movwf PORTD bra Again
Over: movlw A'Y' movwf PORTD bra Again
bra Again

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Time Delay

- We have written a delay subroutine in Ex3-8.
- How to calculate exact delays?
- How to generate various time delay?

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Machine Cycle

- For the CPU to execute an instruction takes a certain number of clock cycles.
- In the PIC18 family, these clock cycles are referred to as *instruction cycles*.
- In PIC18, 4 clock cycles=1 machine cycle
- Different instructions take need different machine cycles

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Example

For a PIC18 system of 4MHz11.0592 MHz, find how long it takes to execute each of the following instructions.

(a) MOVLW (b) DECF (c) MOVWF (d) ADDLW (e) NOP (f) GOTO (g) CALL (h) BNZ

Solution:

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The machine cycle for a system of 11.0952 MHz is 1.085 μs. Table A-1 shows machine cycles for each instructions.

Instruct	Machine cycles	Time to execute
(a) MOVLW	1	$1 \times 1 \mu s = \mu s$
(b) DECF	1	$1 \times 1 \mu s = \mu s$
(c) MOVWF	1	$1 \times 1 \mu s = \mu s$
(d) ADDLW	1	$1 \times 1 \mu s = \mu s$
(e) NOP	1	$1x1 \mu s = \mu s$
(b) GOTO	2	$2x1 \mu s = \mu s$
(c) CALL	2	$2x1 \mu s = \mu s$
(d) BNZ	1 or 2	1 or 2 μs
		p, and takes 1 MC when wewinamgis clear if jump)

Example

The following shows crystal frequency for three different PIC18 based systems. Find the period of the machine cycle in each case. (a)4 MHz (b) 16 MHz (C) 20 MHz

Solution:

(a)4/4=1MHz, 1MC=1 µs (microsecond)

(b) 16/4 MHz = 4 MHz

machine cycle (MC) = 1/4MHz= 0.25μ s

(c) 20 MHz/4 = 5 MHz

 $MC = 1/5 \text{ MHz} = 0.2 \,\mu\text{s}$

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MC

1

1

1

1

2

1

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Example

Find the size of the delay in the following program, if the crystal frequency is 4 MHz.

MYREG EQU 0x08

DELAY: MOVLW 0xFF
MOVWF MYREG

AGAIN: NOP

DECF MYREG, F
BNZ AGAIN
RETURN

[(255 × 5)+1+1+1] × 1 μs = 1278 μs .

Note that BNZ takes two MCs if it jump, and take only one when falling through the loop. The actual time is $1277 \mu s$.

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Example
Find the size of the delay in the following program, if the crystal
frequency is 4 MHz.
        EQU 0x7
R3
        EQU 0x8
DELAY
       MOVLW
                 D'250'
        MOVWF R3
HERE
        NOP
        NOP
        DECF R3, F
       RETURN
For HERE loop, the delay is 5x250=1250µs. The AGAIN loop repeats the HERE loop
200 times. Therefore, we have 200x1250=250 000 μs. (without overhead)
Overhead=5x200-200+1+1+1-1
The delay = 250 \text{ ms} + 0.8 \text{ ms} = 250.8 \text{ ms}
```

You are able to (1/2)

- Code PIC18 Assembly language instructions using loops
- Code PIC18 Assembly language conditional jump instructions
- Explain conditions that determine each conditional jump instruction
- Code GOTO/BRA jump instructions for unconditional jumps

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Example Write a PIC18 code to generate 1 second delay. The crystal frequency is 10 MHz. 10 MHZ => 1 MC = 400 ns. '1 second' needs 2,500,000 MCs If we have a basic loop with 5 MC. That means, we may need to execute this basic loop 500,000 times. 500,000 can be decompose as 20x100x250 MOVLW D'20' MOVWF BACK MOVLW D'100' MOVWF R3 AGAIN MOVLW D'250' MOVWF R2 NOP NOP DECF R4, F BNZ BACK RETURN END Andrew Leung

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You are able to (2/2)

- Calculate target addresses for jump instructions
- Code PIC subroutines
- Code PIC IO ports
- Discuss crystal frequency versus machine cycle
- Code PIC programs to generate a time delay

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