Library of Congress Cataloging-in-Publication Data on file.

Vice President and Editorial Director, ECS: Marcia J. Horton
Acquisitions Editor: Michael McDonald
Senior Managing Editor: David A. George
Production Editor: Irwin Zucker
Art Editor: Greg Dulles
Manufacturing Manager: Alexis Heydt-Long
Manufacturing Buyer: Lisa McDowell
Marketing Manager: Tim Galligan

About the Cover: The cover background is a photo of the Intel® Core™2 Duo processor / Intel® Core™2 Extreme processor die provided courtesy of Intel Corporation.



© 2008 Pearson Education, Inc. Pearson Prentice Hall Pearson Education, Inc. Upper Saddle River, NJ 07458

All rights reserved. No part of this book may be reproduced, in any form or by any means, without permission in writing from the publisher.

Pearson Prentice Hall® is a trademark of Pearson Education, Inc.

Altera and Flex 10K are trademarks of Altera Corporation, Advanced Micro Devices, AMD, Athlon, and 3DNow! are trademarks of Advanced Micro Devices, Inc. Verilog is a registered trademark of Cadence Design Systems, Inc. Freescale and Altivec are trademarks of Freescale Semiconductor, IBM and PowerPC are trademarks of IBM Corporation, Intel, Intel Core, and MMX are trademarks of Intel Corporation, GAL and PAL are trademarks of Lattice Semiconductor Corporation. Mentor Graphics, Model Technology, and ModelSim are trademarks of Mentor Graphics Corporation. PowerPoint is registered trademark of the Microsoft Corporation. RAMBUS and RDRAM are registered trademarks of RAMBUS, Inc. Cell, Sony and Playstation are trademarks of Sony Corporation. Toshiba is a trademark of Toshiba Corporation. Xilinx and Spartan are registered trademarks of Xilinx, Inc.

The author and publisher of this book have used their best efforts in preparing this book. These efforts include the development, research, and testing of the theories and programs to determine their effectiveness. The author and publisher make no warranty of any kind, expressed or implied, with regard to these programs or the documentation contained in this book. The author and publisher shall not be liable in any event for incidental or consequential damages in connection with, or arising out of, the furnishing, performance, or use of these programs.

Printed in the United States of America

12 11

X-JSPAF1-E1-O NAZI

Pearson Education Ltd., London
Pearson Education Australia Pty. Ltd., Sydney
Pearson Education Singapore, Pte. Ltd.
Pearson Education North Asia Ltd., Hong Kong
Pearson Education Canada, Inc., Toronto
Pearson Educación de Mexico, S.A. de C.V.
Pearson Education—Japan, Tokyo
Pearson Education Malaysia, Pte. Ltd.
Pearson Education, Inc., Upper Saddle River, New Jersey

CONTENTS

Preface □ Chapter 1	3	xii
DIGITAL SYST	TEMS AND INFORMATION	ina tanàna io dia mandra di senara quimbar, any mandra dia senara da
1-1	Information Representation	4
	The Digital Computer	(
	Beyond the Computer	,
	More on the Generic Computer	1:
1-2	Number Systems	13
	Binary Numbers	14
	Octal and Hexadecimal Numbers	16
	Number Ranges	17
1-3	Arithmetic Operations	18
	Conversion from Decimal to Other Bases	20
1-4	Decimal Codes	23
	BCD Addition	24
1-5	Alphanumeric Codes	25
	ASCII Character Code	20
	Parity Bit	20
1-6	Gray Codes	28
1-7	Chapter Summary	3.
	References	33
	Problems	33
□ Chapter 2	35	\$
COMBINATION	NAL LOGIC CIRCUITS	35
2-1	Binary Logic and Gates	3.
	Binary Logic	36
	Logic Gates	38

D i

2-2	Boolean Algebra	39
- -	Basic Identities of Boolean Algebra	42
	Algebraic Manipulation	44
	Complement of a Function	47
2-3	Standard Forms	48
,·	Minterms and Maxterms	49
	Sum of Products	52
	Product of Sums	54
2-4	Two-Level Circuit Optimization	54
- •	Cost Criteria	55
	Map Structures	56
	Two-Variable Maps	59
	Three-Variable Maps	61
2-5	Map Manipulation	65
	Essential Prime Implicants	65
	Nonessential Prime Implicants	67
	Product-of-Sums Optimization	68
	Don't-Care Conditions	70
2-6	Pragmatic Two-Level Optimization	72
2-7	Multiple-Level Circuit Optimization	76
2-8	Other Gate Types	81
2-9	Exclusive-OR Operator and Gates	85
	Odd Function	86
2-10	High-Impedance Outputs	88
2-11	Chapter Summary	90
	References	90
	Problems	91
□ Chapte	r 3 97	
Combina	TIONAL LOGIC DESIGN	97
3-1	Design Procedure	97
3-2	Beginning Hierarchical Design	104
3-3	Technology Mapping	107
3-4	Verification	111
	Manual Logic Analysis	111
	Simulation	113
3-5	Combinational Functional Blocks	113
3-6	Rudimentary Logic Functions	115
	Value-Fixing, Transferring, and Inverting	115
	Multiple-Bit Functions	116
	Enabling	119

3-7	Decoding	121
	Decoder and Enabling Combinations	124
	Decoder-Based Combinational Circuits	126
3-8	Encoding	127
	Priority Encoder	129
	Encoder Expansion	130
3-9	Selecting	131
	Multiplexers	131
	Multiplexer-Based Combinational Circuits	136
3-10	Chapter Summary	138
	References	140
	Problems	140
□ Chapter 4	149	ower or believe of the latest security to the latest security to
ARITHMETIC 1	Functions and HDLs	149
4-1	Iterative Combinational Circuits	150
4-2	Binary Adders	151
	Half Adder	151
	Full Adder	152
	Binary Ripple Carry Adder	153
4-3	Binary Subtraction	155
	Complements	157
	Subtraction Using 2s Complement	158
4-4	Binary Adder-Subtractors	159
	Signed Binary Numbers	161
	Signed Binary Addition and Subtraction	163
	Overflow	165
4-5	Other Arithmetic Functions	167
	Contraction	167
	Incrementing	1.69
	Decrementing	170
	Multiplication by Constants	170
	Division by Constants	172
	Zero Fill and Extension	172
4-6	Hardware Description Languages	173
- *	Hardware Description Languages	173
	Logic Synthesis	175
4-7	HDL Representations—VHDL	176
	Behavioral Description	186

4-8	HDL Representations—Verilog	187	☐ Chapter 6
4.0	Behavioral Description	195	Cor nowen Dr
4-9	Chapter Summary	196	SELECTED DE
	References Problems	196 197	6-1
	Problems	197	
□ Chapter 5	207		
		207	6-2 6-3
SEQUENTIAL (207	6-4
5-1	Sequential Circuit Definitions	208	6-5
5-2	Latches CD = 1 CD Latches	210	6-6
	SR and \overline{SR} Latches	211	6-7
~ a	D Latch	214	
5-3	Flip-Flops	215	6-8
	Master–Slave Flip-Flops	216	
	Edge-Triggered Flip-Flop	218	
	Standard Graphics Symbols	219	
	Direct Inputs	221	6-9
5-4	Sequential Circuit Analysis	222	
	Input Equations	223	
	State Table	224	
	State Diagram	227	
	Sequential Circuit Simulation	229	☐ Chapter 7
5-5	Sequential Circuit Design	230	
	Design Procedure	231	REGISTERS AN
	Finding State Diagrams and State Tables	231	7-1
	State Assignment	238	
	Designing with D Flip-Flops	240	7-2
	Designing with Unused States	243	7-3
	Verification	245	7-4
5-6	Other Flip-Flop Types	247	7-5
	JK and T Flip-Flops	247	
5-7	State-Machine Diagrams and Applications	250	
	State-Machine Diagram Model	250	
	Constraints on Input Conditions	253	7-6
	Design Applications Using State-Machine Diagrams	256	, 0
5-8	HDL Representation for Sequential Circuits—VHDL	264	
5-9	HDL Representation for Sequential Circuits—Virible	272	
5-10	Chapter Summary	278	
5-10	References	279	
	Problems	280	
	rionenis	7911	

Chapter	6	29	5
---------	---	----	---

Chapter		
SELECTED D	ESIGN TOPICS	295
6-1	The Design Space	295
	Integrated Circuits	296
	CMOS Circuit Technology	296
	Technology Parameters	302
6-2	Gate Propagation Delay	304
6-3	Flip-Flop Timing	306
6-4	Sequential Circuit Timing	308
6-5	Asynchronous Interactions	310
6-6	Synchronization and Metastability	312
6-7	Synchronous Circuit Pitfalls	318
6-8	Programmable Implementation Technologies	319
	Read-Only Memory	322
	Programmable Logic Array	323
	Programmable Array Logic Devices	327
6-9	Chapter Summary	329
	References	329
	Problems	330
<u>.</u>		
□ Chapter 7	335	
REGISTERS A	ND REGISTER TRANSFERS	335
7-1	Registers and Load Enable	336
i i i	Register with Parallel Load	337
7-2	Register Transfers	339
7-3	Register Transfer Operations	341
7-4	A Note for VHDL and Verilog Users Only	344
7-5	Microoperations	344
	Arithmetic Microoperations	345
	Logic Microoperations	347
i,	Shift Microoperations	349
7-6	Microoperations on a Single Register	350
	Multiplexer-Based Transfers	350
	Shift Registers	353
	2	353 357
	Shift Registers	

Other Counters

363

7-7	Register-Cell Design	366
7-8	Multiplexer and Bus-Based Transfers	
	for Multiple Registers	372
	Three-State Bus	374
7-9	Serial Transfer and Microoperations	375
	Serial Addition	377
7-10	Control of Register Transfers	378
	Design Procedure	380
7-11	HDL Representation for Shift Registers	
	and Counters—VHDL	395
7-12	HDL Representation for Shift Registers	
	and Counters—Verilog	398
7-13	Microprogrammed Control	399
7-14	Chapter Summary	402
	References	402
	Problems	402
☐ Chapter 8	413	
Memory Bas	ZICS	413
8-1	Memory Definitions	413
3-2	Random-Access Memory	414
- -	Write and Read Operations	416
	Timing Waveforms	417
	Properties of Memory	419
3-3	SRAM Integrated Circuits	419
)- - 3	Coincident Selection	422
3-4	Array of SRAM ICs	425
3-5	DRAM ICs	429
, ,	DRAM Cell	429
	DRAM Bit Slice	431
3-6	DRAM Types	435
, 0	Synchronous DRAM (SDRAM)	436
	Double-Data-Rate SDRAM (DDR SDRAM)	439
	RAMBUS® DRAM (RDRAM)	439
» ¬	Arrays of Dynamic RAM ICs	439
8-7 8-8	Chapter Summary	441
o-0	References	441
		441
	Problems	441

□ Chapter 9 443

COMPUTEI	R DESIGN BASICS	443
9-1	Introduction	444
9-2	Datapaths	444
9-3	The Arithmetic/Logic Unit	447
	Arithmetic Circuit	448
	Logic Circuit	450
	Arithmetic/Logic Unit	451
9-4	The Shifter	453
	Barrel Shifter	454
9-5	Datapath Representation	455
9-6	The Control Word	* 458
9-7	A Simple Computer Architecture	464
	Instruction Set Architecture	464
	Storage Resources	465
	Instruction Formats	466
	Instruction Specifications	468
9-8	Single-Cycle Hardwired Control	471
	Instruction Decoder	472
	Sample Instructions and Program	474
	Single-Cycle Computer Issues	477
9-9	Multiple-Cycle Hardwired Control	478
	Sequential Control Design	482
9-10	Chapter Summary	489
	References	490
	Problems	490
□ Chapte	r 10 497	
INSTRUCT	TION SET ARCHITECTURE	497
10-1	Computer Architecture Concepts	497
10-1	Basic Computer Operation Cycle	498
	Register Set	× 499
10-2	Operand Addressing	499
10-2	Three-Address Instructions	500
_	Two-Address Instructions	501
	One-Address Instructions	501
	Zero-Address Instructions	502

10-3	Addressing Modes	506		Control Organization	300
	Implied Mode	507		Data Hazards	563
	Immediate Mode	507		Control Hazards	570
	Register and Register-Indirect Modes	508	11-4	The Complex Instruction Set Computer	574
	Direct Addressing Mode	508		ISA Modifications	575
	Indirect Addressing Mode	510		Datapath Modifications	577
	Relative Addressing Mode	510		Control Unit Modifications	577
	Indexed Addressing Mode	511		Microprogrammed Control	579
	Summary of Addressing Modes	511		Microprograms for Complex Instructions	582
10-4	Instruction Set Architectures	513	11-5	More on Design	586
10-4	Data-Transfer Instructions	514		Advanced CPU Concepts	586
10-3	Stack Instructions	515		Recent Architectural Innovations	589
		517	11-6	Chapter Summary	592
10.7	Independent versus Memory-Mapped I/O	518		References	593
10-6	Data-Manipulation Instructions	518		Problems	593
	Arithmetic Instructions	519			
	Logical and Bit-Manipulation Instructions	520		10 507	
10.5	Shift Instructions		☐ Chapter	12 597	
10-7	Floating-Point Computations	522	Assilianova Signila et monta a signimuni et monta a signimuni et monta a signimuni et monta a signimuni et mon	TPUT AND COMMUNICATION	597
	Arithmetic Operations	523	\$56\$EFF\$66\$EFF\$65555555		597
	Biased Exponent	524 525	12-1	Computer I/O	598
	Standard Operand Format	525	12-2	Sample Peripherals	598
10-8	Program Control Instructions	527		Keyboard Hard Drive	599
	Conditional Branch Instructions	528			601
	Procedure Call and Return Instructions	530		Liquid Crystal Display Screen	604
10-9	Program Interrupt	531		I/O Transfer Rates I/O Interfaces	604
	Types of Interrupts	533	12-3	I/O Bus and Interface Unit	605
	Processing External Interrupts	534			606
10-10	Chapter Summary	535		Example of I/O Interface	608
	References	536		Strobing	609
	Problems	537	10.4	Handshaking Serial Communication	611
			12-4		612
	11 542			Synchronous Transmission The Keyboard Povisited	612
☐ Chapte	r 11 543			The Keyboard Revisited A Packet-Based Serial I/O Bus	613
DICC	CICC Community Property Living	543	10.5	Modes of Transfer	617
	CISC CENTRAL PROCESSING UNITS		12-5	Example of Program-Controlled Transfer	618
11-1	Pipelined Datapath	544		Interrupt-Initiated Transfer	620
	Execution of Pipeline Microoperations	548	10.6	<u>.</u>	620
11-2	Pipelined Control	549	12-6	Priority Interrupt	621
	Pipeline Programming and Performance	551		Daisy Chain Priority Parallel Priority Hardware	623
11-3	The Reduced Instruction Set Computer	553	10.7	· · · · · · · · · · · · · · · · · · ·	624
	Instruction Set Architecture	554	12-7	Direct Memory Access	625
	Addressing Modes	557		DMA Controller	627
	Datapath Organization	557		DMA Transfer	027

12-8	Chapter Summary References Problems	628 628 629
□ Chapter 13	633	
MEMORY SYS	TEMS	633
13-1	Memory Hierarchy	633
13-2	Locality of Reference	636
13-3	Cache Memory	638
	Cache Mappings	640
	Line Size	645
	Cache Loading	647
	Write Methods	647
	Integration of Concepts	648
	Instruction and Data Caches	651
	Multiple-Level Caches	651
13-4	Virtual Memory	652
	Page Tables	654
	Translation Lookaside Buffer	656
	Virtual Memory and Cache	658
13-5	Chapter Summary	658
	References	659
	Problems	659
INDEX		663

PREFACE

The objective of this text is to serve as a cornerstone for the learning of logic design, digital system design, and computer design by a broad audience of readers. This fourth edition marks the decade point in the evolution of the text contents. Beginning as an adaptation of a previous book by the first author in 1997, it continues to offer a unique combination of logic design and computer design principles with a strong hardware emphasis. Over the years, the text has followed industry trends by adding new material such as hardware description languages, removing or de-emphasizing material of declining importance, and revising material to track changes in computer technology and computer-aided design.

In the fourth edition, revisions address pedagogical considerations as well as industrial trends. Sixty "real world" examples and problems, most drawn from design problems for products encountered in contemporary day-to-day life, motivate interest and provide practice in solution formulation. Changes in chapter organization permit instructors to more easily tailor the degree of technology coverage, accommodating both electrical and computer engineering and computer science audiences.

The organizational changes begin with the combining of the introduction to design from Chapter 3 and the functional block material from Chapter 4 into a new Chapter 3. The design science content from the old Chapter 3 is now distributed over multiple chapters on an "as needed" basis and is accompanied by illustrations. Hardware description language coverage for combinational circuits has been combined in Chapter 4 with that for arithmetic circuits to balance chapter size. Material on technology from the old Chapter 3, including timing and programmable logic, appears in a new Chapter 6 and can be selectively covered and scheduled by the instructor as appropriate for the course syllabus. The placement of this material in Chapter 6 permits earlier coverage of sequential circuits for those with lesser technology-related needs and provides the more extensive background needed for some of the topics covered. Further, technology topics fit better within digital system design rather than within basic logic design material presented earlier in the text. Chapter 6 also contains new information on CMOS circuits and asynchronous interaction between systems including synchronization of inputs and metastability.

Chapter 8 has been eliminated along with the algorithmic state machine (ASM) to streamline the treatment of design of complex sequential circuits and control units. Concepts from Chapter 8 are split between Chapter 5 (Sequential Circuits) and Chapter 7 (Registers and Register Transfers). A new state machine