life.augmented

ST8500 training

Summary

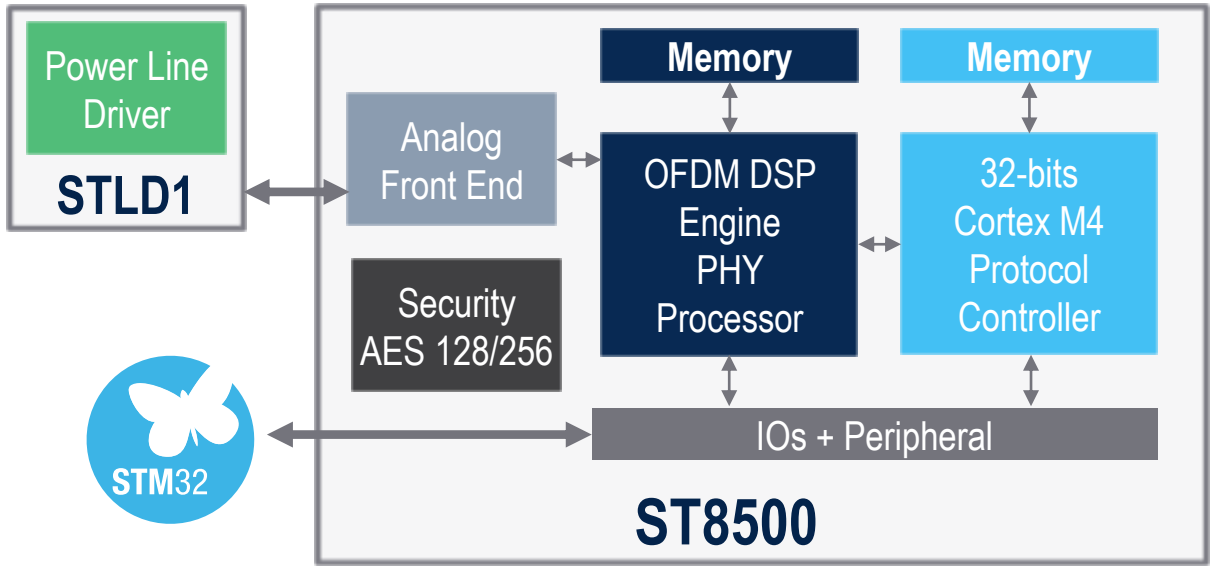
- ST8500 platform overview
- Hybrid PLC&RF technology
- ST8500 development ecosystem
- EVALKITST8500-1 overview
- EVLKST8500GH868 / 915 overview
- ST8500 evaluation - Quick Start
  - G3-PLC Evaluation Package content
  - G3-PLC Graphical User Interface
    - Node tree and G3LIB configuration
    - G3-PLC PHY Layer mode
    - G3-PLC IPv6 Layer mode

ST PLC state-of-the-art solution: ST8500 platform

life.augmented

ST PLC state-of-the-art solution: **ST8500 + STLD1**

Programmable, ultra-low power and compact PLC solution



Certified Turn-key Multi-Standard PLC protocols

- Programmable, certified protocol standards: G3-PLC, PRIME…
- OFDM robust modulations with sophisticated correction coding
- Full 500 kHz band coverage for increased performance & reliability
- 6LoWPAN and IPv6 supported

Secure, robust and modular system architecture

- ST8500 AES 128/256-bit engine for secure data encryption and anti-tampering
- Broad range of STM32 external host controllers for any application
- Low distortion, high current capability **STLD1** Power Line Driver with up to 36 V p-p, 1.5 A rms output for robust communication even in high attenuating, low impedance network

Low-power and compact solution

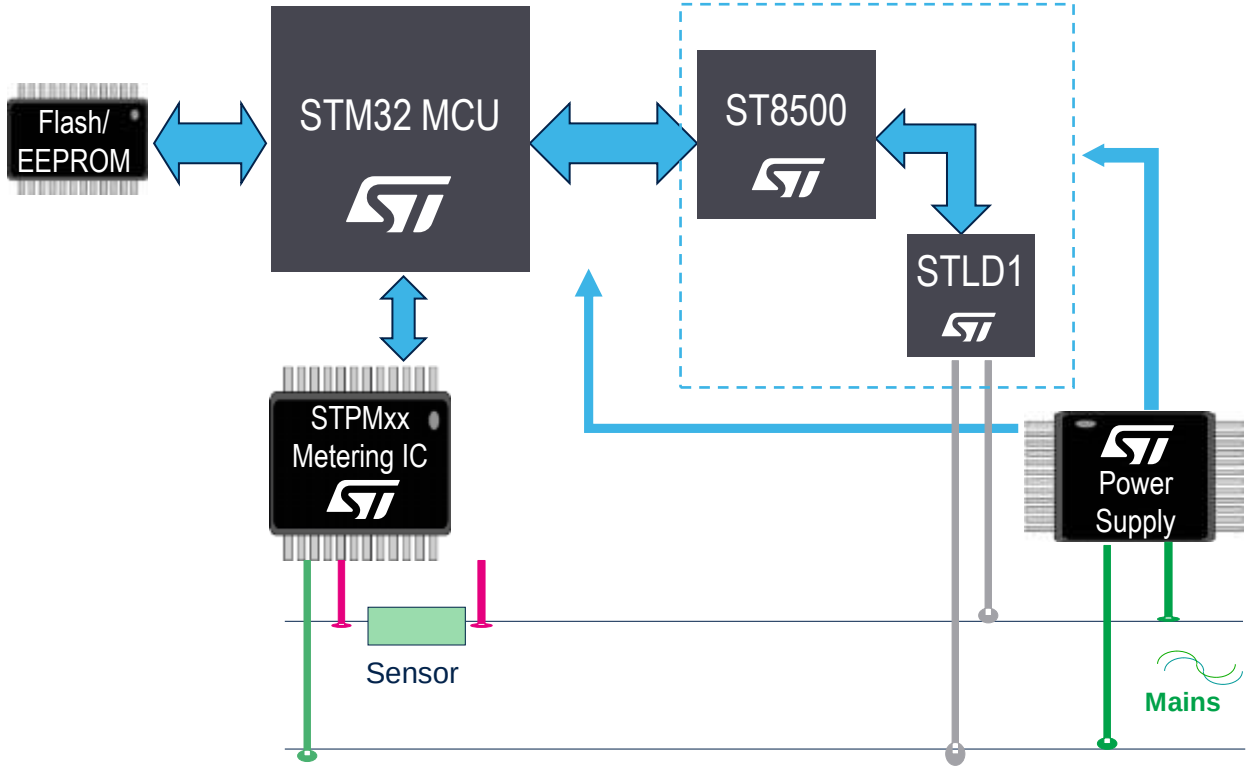
- Lowest Power Consumption in RX mode: 100 mW typ
- QFN 7x7 mm package for PCB optimization
- Extended Industrial temperature -40°C to 105°C

KEY APPLICATIONS

Powerline communication for remote management

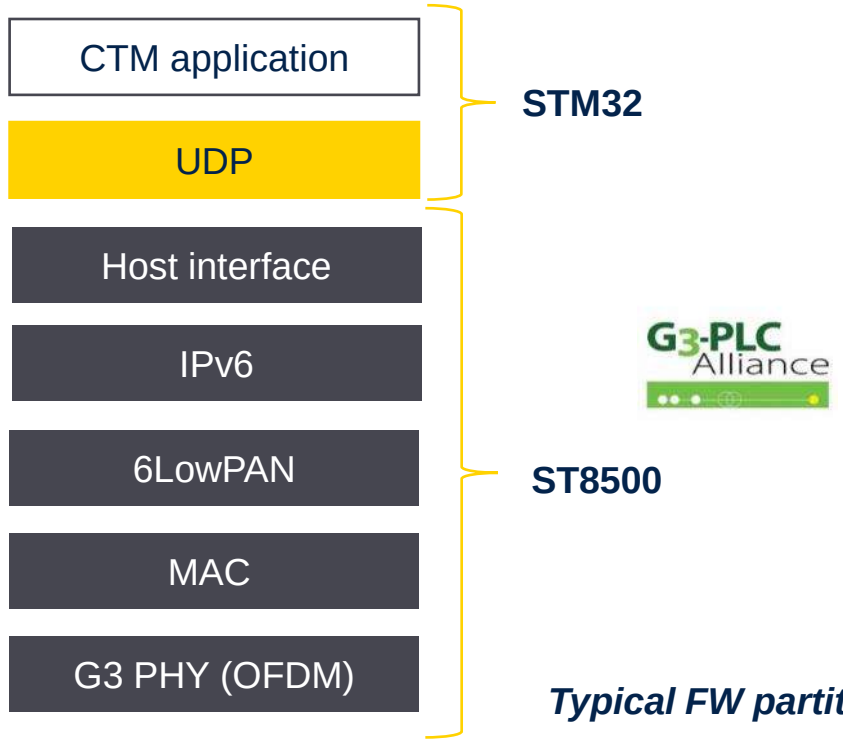
- Smart Metering / Smart Grid
- Smart Home & Smart Building
- Smart City, Smart Street lighting
- Smart Infrastructure, Smart Railways
- Industrial IoT

ST8500 in a typical Smart Energy application



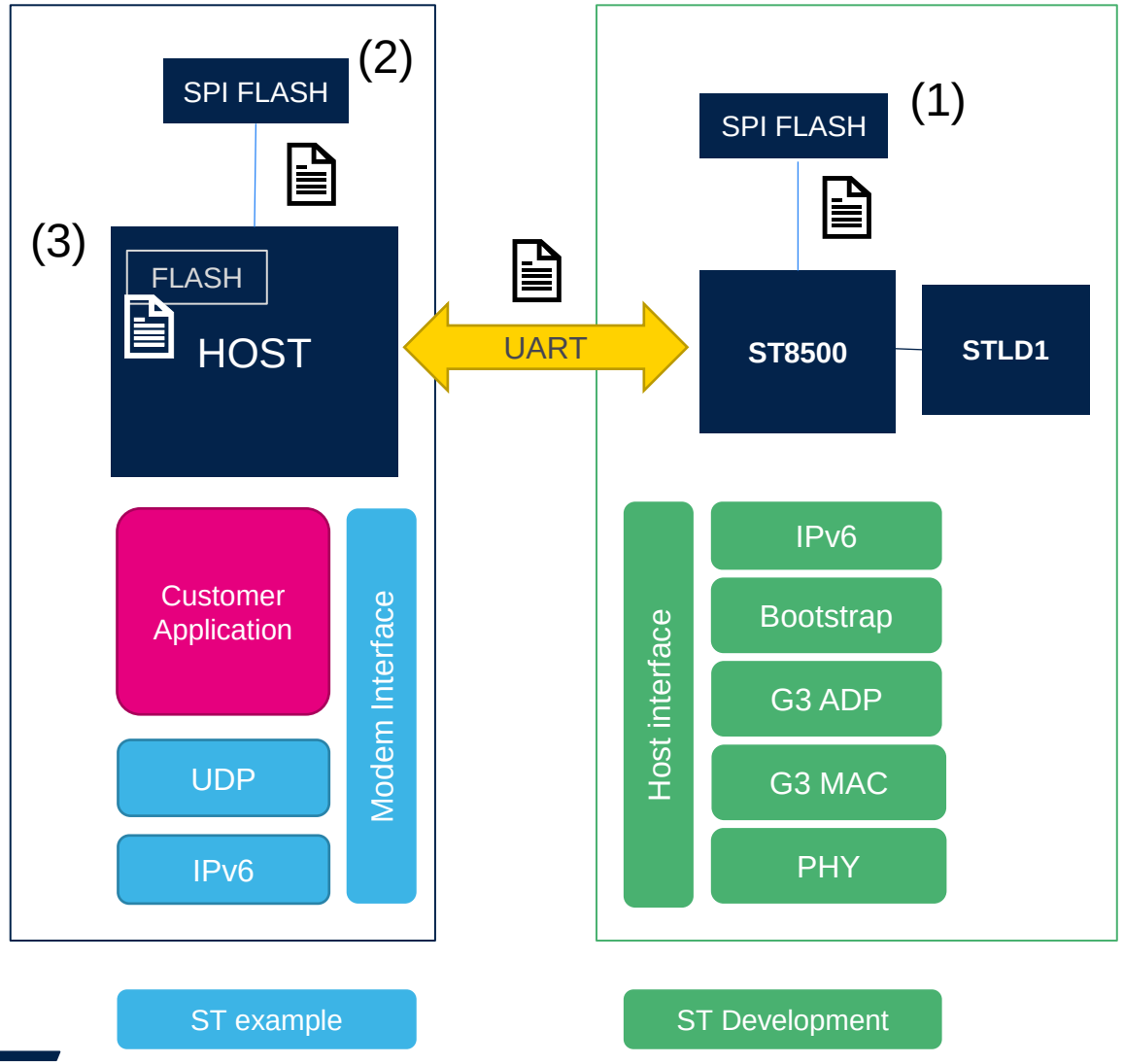
Benefits from ST modular architecture:

- Full flexibility, separated functional domains
- Best-in class components for each function
- Consolidated, ready to go BoM
- Certified, multi-million field proven / deployed PLC solution



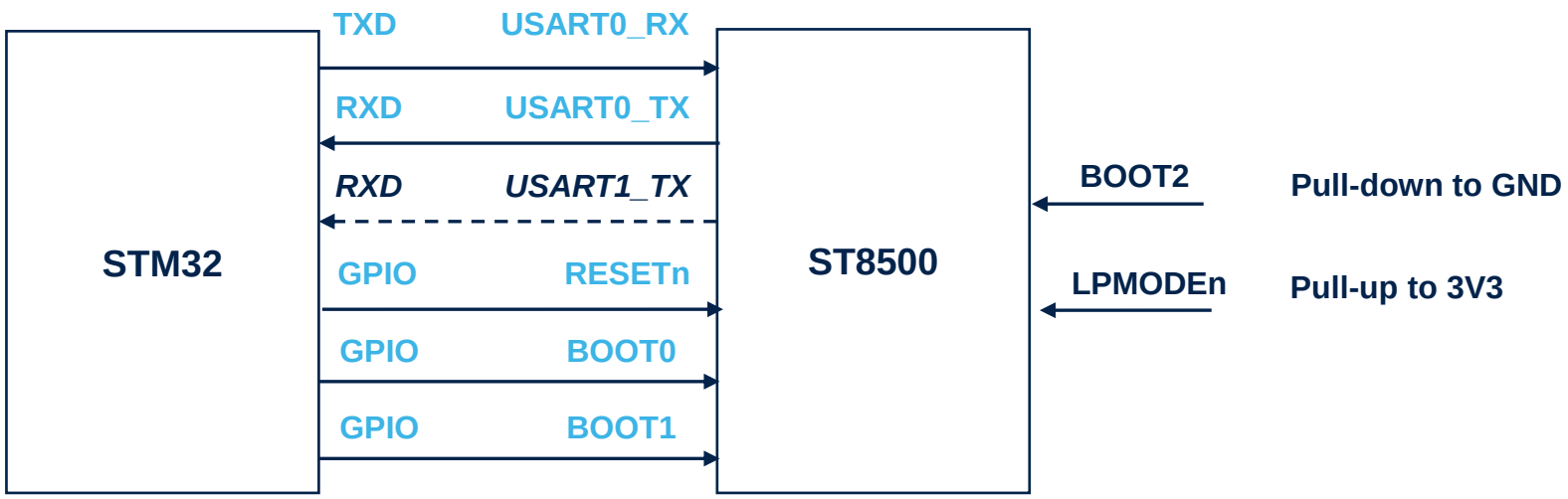
Typical FW partitioning

ST8500 : Host / modem G3-PLC FW partitioning



- ST8500 is RAM based (code + data) ➔ PE and RTE images shall be loaded at boot time
- ST8500 images (up to 350 kB) can be stored in:
  - (1) SPI FLASH connected to ST8500
  - (2) SPI FLASH connected to STM32
  - (3) Host controller internal FLASH
- Boot time (typ) vs image download mode:
  - ST8500 SPI FLASH (case 1) ➔ <1 sec
  - UART (case 2,3) ➔ 5 sec @ 920 kbps
- ST8500 G3 starts by default in ADP (6LoWPAN) mode
  - It can be configured by API
- Flexible UDP/IP implementation:
  - on ST8500 side
  - on STM32 side

Typical host MCU configuration for ST8500



Host MCU resources:

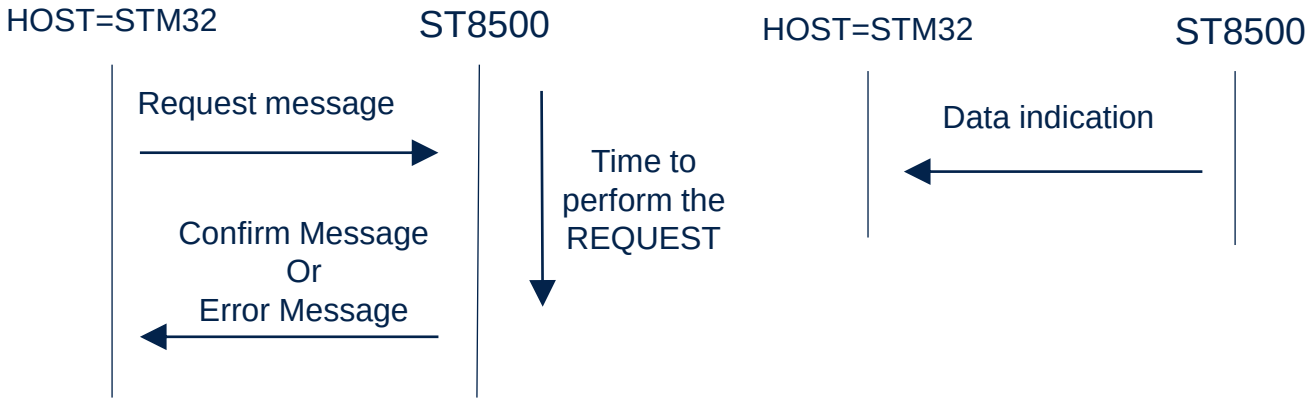
- ❑ 3x GPIOs
- ❑ 1x UART *(+1 optional UART TX for debug trace)*
- ❑ UDP application example:
  - ❑ ~95 KB Flash
  - ❑ ~36 KB Ram

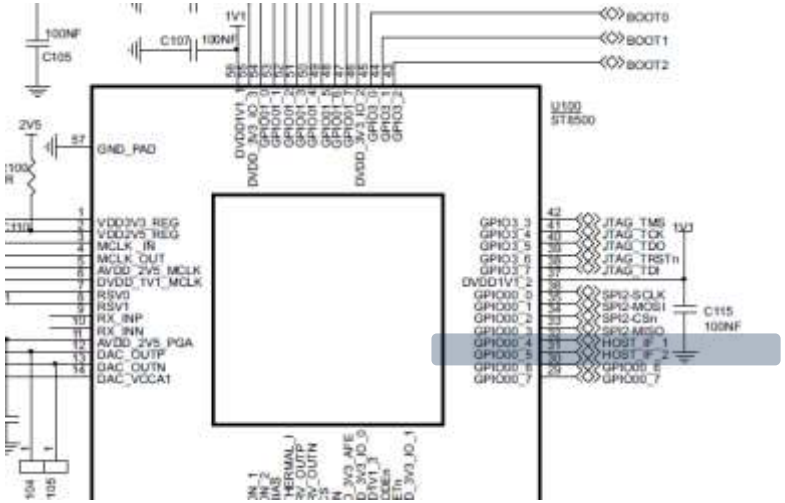
ST8500 Boot modes

Table 2. Boot modes

Boot2	Boot1	Boot0	Boot ID	Boot mode
0	0	0	0x0	Boot from UART host interface
0	0	1	0x1	Boot from SPI host interface
0	1	0	0x2	Boot from SPI external Flash (large configuration)
0	1	1	0x3	Boot from SPI external Flash (small configuration)
1	0	0	0x4	Reserved
1	0	1	0x5	Reserved
1	1	0	0x6	Reserved
1	1	1	0x7	Reserved

UART Host Interface: Request/Confirm & Indication





- Both the modem and the host controller can send messages asynchronously on UART
- Handshake is guaranteed by
  - Confirm message to Host controller in case the Request message is received and processed normally
  - Error message to Host controller in case the Request message was not correctly received

UART Host Interface: G3-PLC

- No HW handshake, 2 wire UART between Host and ST8500
- Baud rates from 9600 bps to 921 kbps:
  - During download, set at 921 kbps
  - During on-field operations, set at 230 kbps

Table 4. Host Interface Command Messages Formats

Request Message Format										
Synchro Field		**Control Field**		**Security Field**		**Message Payload Field**			**Check**	
0x16	0x16	CMD_ID	MSG_LEN	SEC_MODE	COUNTER	MSG_0	...	MSG_{LEN-1}	TAG	CRC
2 Bytes		1 Byte	2 Bytes	1 Byte	4 Bytes	MSG_LEN Bytes			0/8 Bytes	2 Bytes
Confirm and Indication Message Format										
Synchro Field		**Control Field**		**Security Field**		**Message Payload Field**			**Check**	
0x16	0x16	CMD_ID	MSG_LEN	SEC_MODE	COUNTER	Error Code	MSG_1	... MSG_{LEN-1}	TAG	CRC
2 Bytes		1 Byte	2 Bytes	1 Byte	4 Bytes	1 Byte	MSG_LEN-1 Bytes		0/8 Bytes	2 Bytes

- Reference
  - The commands of Host Interface (HI) for G3-PLC is described into

    ST-G3-PLC_Solutions_AN.pdf

ST8500 + STLD1 power consumption

- Current measured in TX and RX by power domain
  - Overall power is given without taking into account the DC-DC efficiency

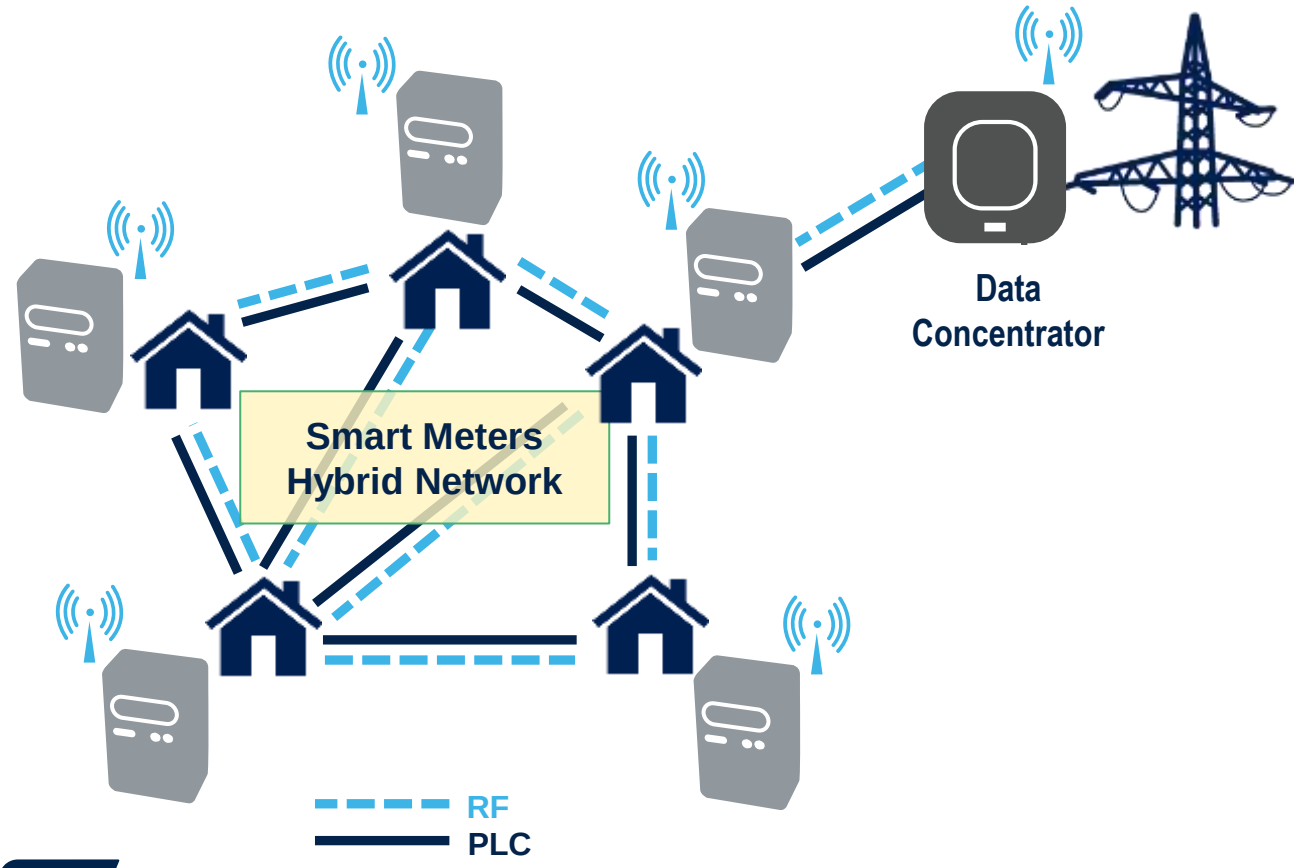
Mode	ST8500 by power domain				STLD1
	+1V1	+2V5	+3V3	Total	+15V
TX	45 mA	18 mA	8 mA	121 mW	40 mA + (load dependent)
RX	46 mA	10 mA	6 mA	96 mW	1 mA

Hybrid PLC+RF technology evolution

life.augmented

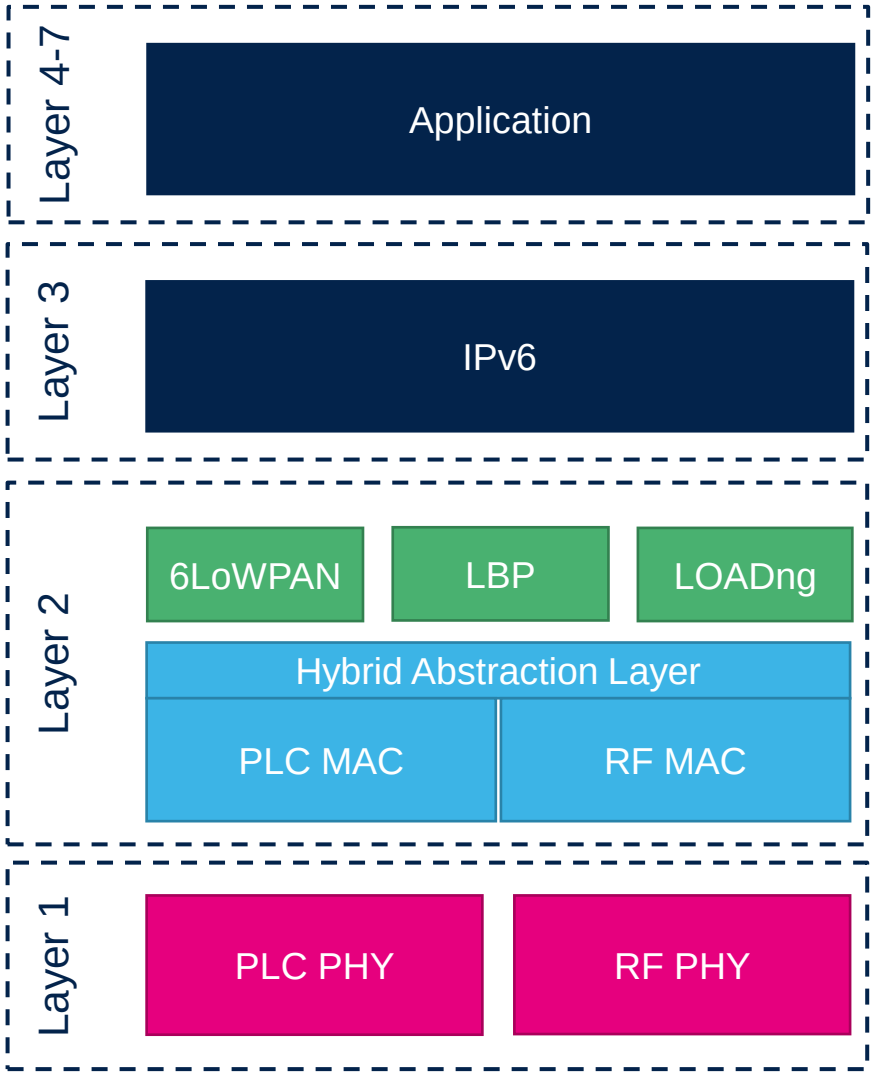
New hybrid PLC+RF technology

Expanding PLC capabilities



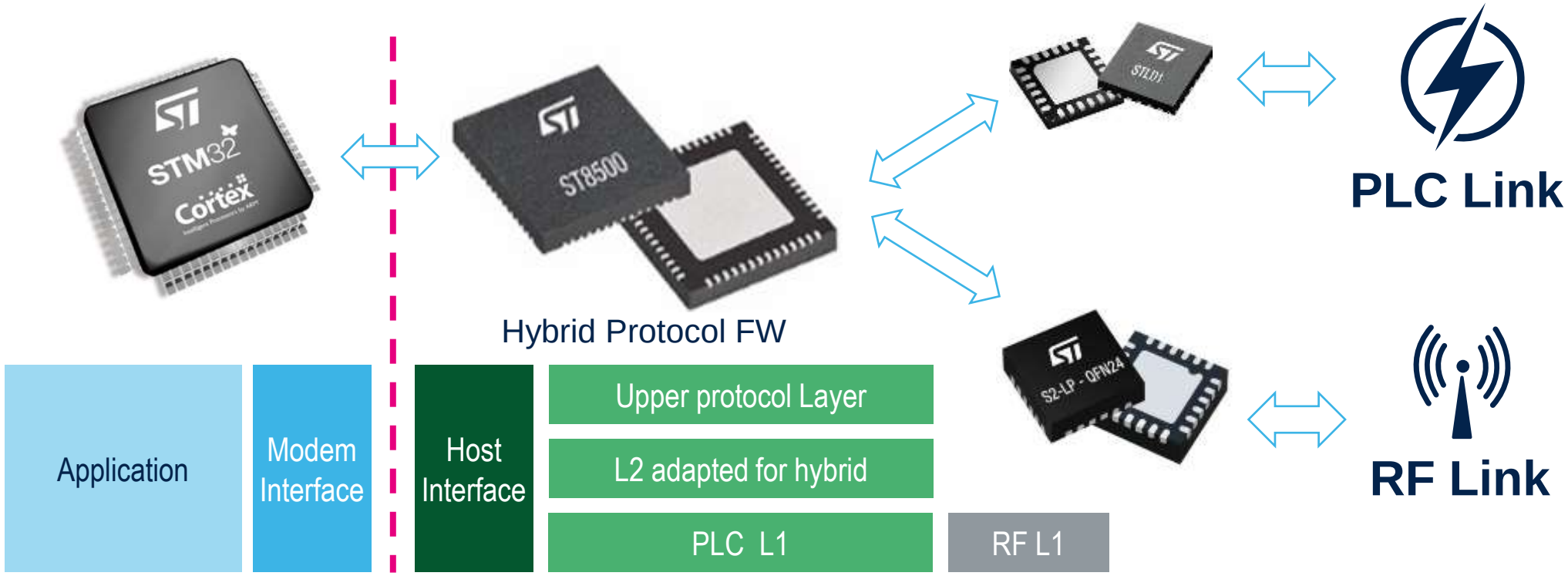
- Challenging network topologies
  - Rural area networks
  - MV/LV transformer bypass
  - Particularly harsh noise/impedance conditions
- Need to extend to other Smart Grid services (e.g. DER)
- Solution: **fully hybrid** PLC + RF Network
  - Each node has PLC and RF connectivity
  - The route is built with a **hop-by-hop automatic selection** of the best between PLC and RF media (dynamically adjusted)
- Boosting Key Performance Indicators to **100**%

Hybrid PLC + RF technology: Optimal standard-based integration



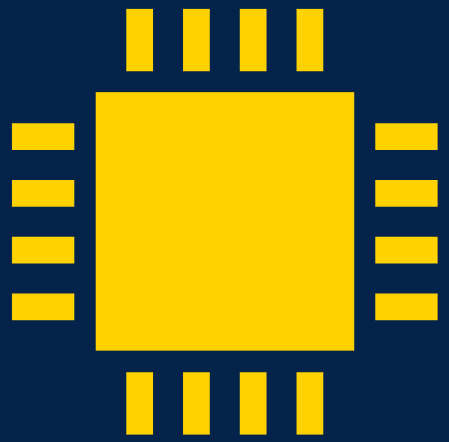
- G3-PLC technology first to adopt this standard-based fully-integrated hybrid approach
  - G3-PLC already based on IEEE 802.15.4-2007
- Layer 1 extension: added FSK RF PHY from IEEE 802.15.4-2015/17
- Layer 2 integration:
  - 2 separate MAC Layers (CSMA, ACK, …)
  - Hybrid Abstraction Layer to deal with common lower layer procedures
  - Hop-by-hop PLC or RF media selection
- Status:
  - Specification and interoperability process completed
  - Certification process available from end 2020
- For more info, visit https://g3-plc.com/what-is-g3-plc/g3-plc-hybrid-plcrf/

ST8500 + S2-LP hybrid PLC-RF turn-key solution



- ST8500 as PLC modem and PLC-RF Hybrid protocol processor
- Turn-key firmware for ST8500 automatic selection of RF Sub-GHz link or PLC link depending on network quality conditions
- Based on 6LoWPAN and IPv6
- Modular solution leveraging on whatever STM32 application host

ST8500 development ecosystem



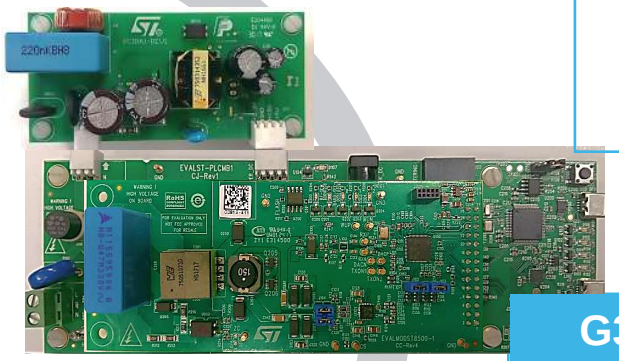
life.augmented

ST8500 ecosystem

Evaluation boards

- **EVALKITST8500-1**
  - ✓ Ready-to-use, full-performance PLC node for AC applications
- **EVLKST8500GH868 / 915**
  - ✓ Modular development kit for hybrid PLC+RF solutions based on NUCLEO

New!



Design Resources

- Documentation available:
  - ✓ Datasheets
  - ✓ Schematics
  - ✓ BoM
  - ✓ PCB layout
  - ✓ Design Guides

G3-PLC Protocol FW packages

- **G3-PLC** single binary **CEN A/B/FCC** + Device/Coordinator
- **Hybrid G3-PLC** with RF expansion
- G3-PLC Application Note
- Graphical User Interface
- STM32 driver

New!

G3-PLC SW Package for non-metering applications

- Package to address non-metering connectivity solutions
- Downloadable from st.com:
  - ✓**STSW-SGKITGUI**: GUI for PC
  - ✓**STSW-ST8500G3**: G3-PLC images and STM32 FW

PRIME PLC Protocol FW packages

- **PRIME 1.3.6** and **1.4 (Service Node** and **Base Node)**
- PRIME Application Note
- Graphical User Interface

Application-specific SW packages

- **ST8500 SmartSolar FW** (dual mode SUNSPEC + nPSK)
- Windows PC test tool (command line)
- User Manuals

New!

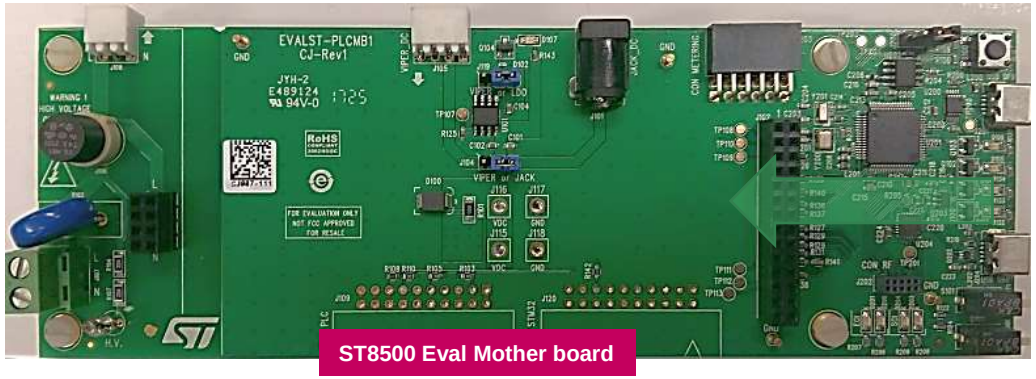
EVALKITST8500-1 overview

life.augmented

EVALKITST8500-1: modularity

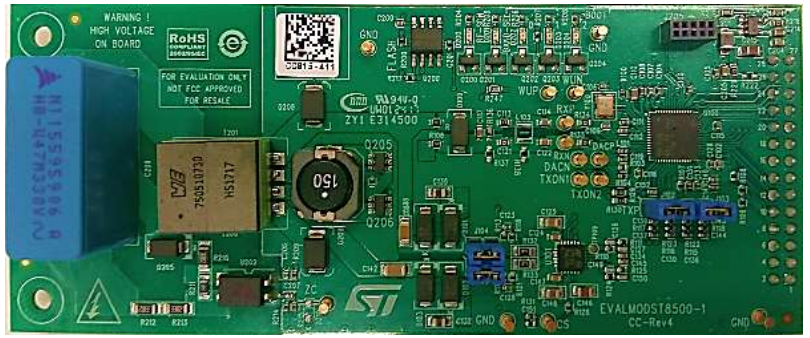
- Full-performance PLC connectivity module
  - Enable CENELEC/FCC band selection thru FW control (patented automatic HW tuning)
- Module approach for easy and future-proof evaluation
  - ST8500 UART host connection to the STM32 mother board, with USB-UART conversion for PC access
  - Additional module interface for future development of HW add-ons

VIPER26H Power Supply module

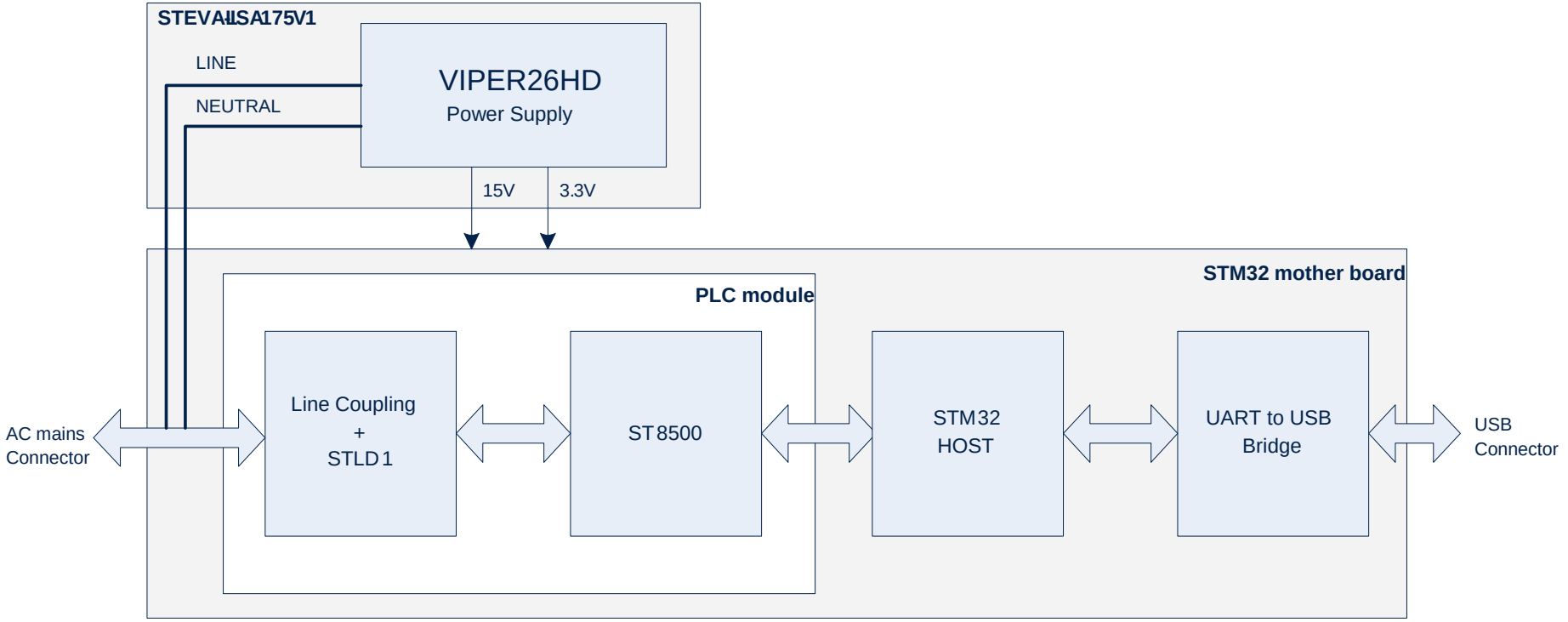


ST8500 Eval Mother board

ST8500 Eval Module

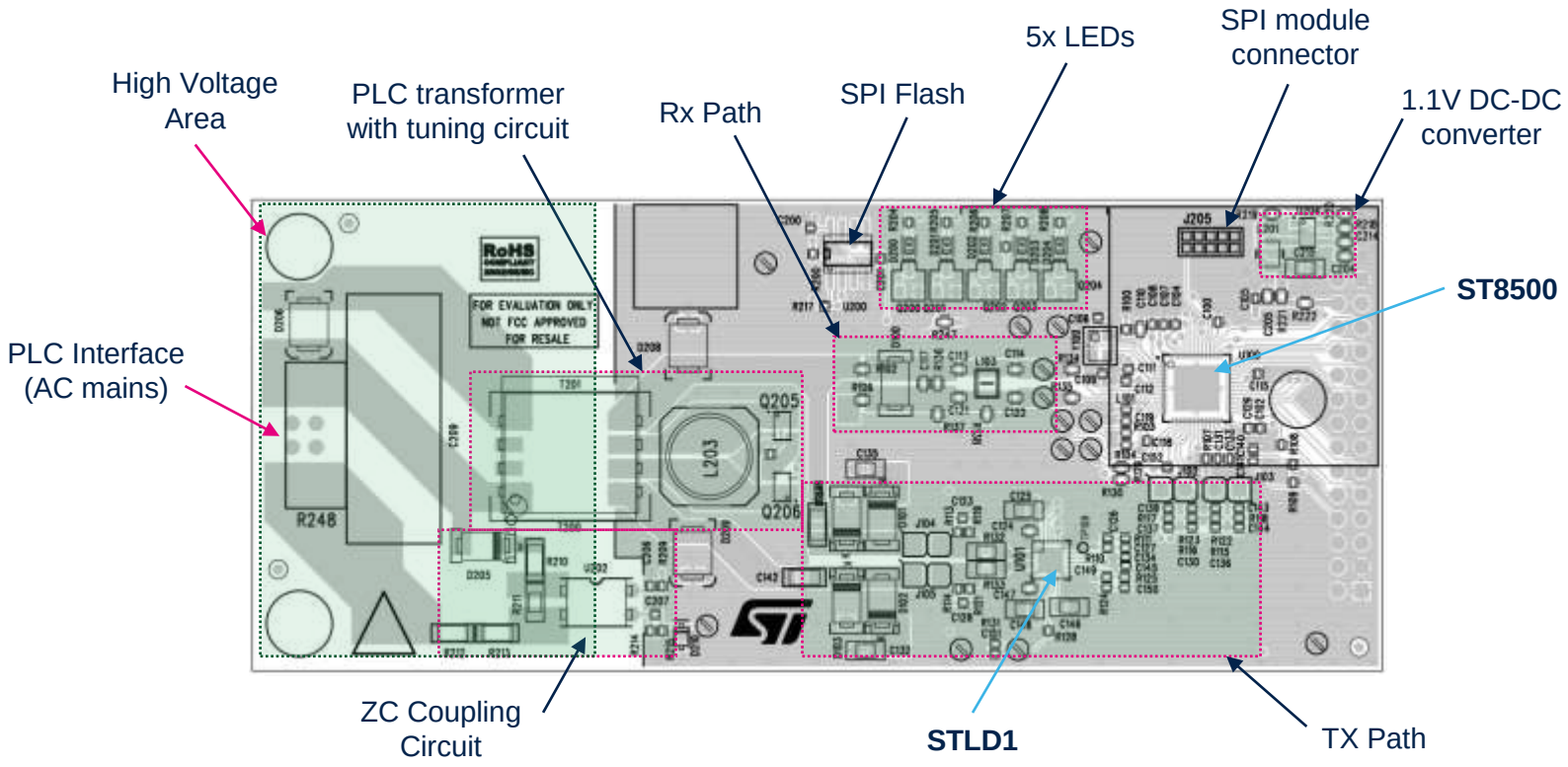


Block diagram

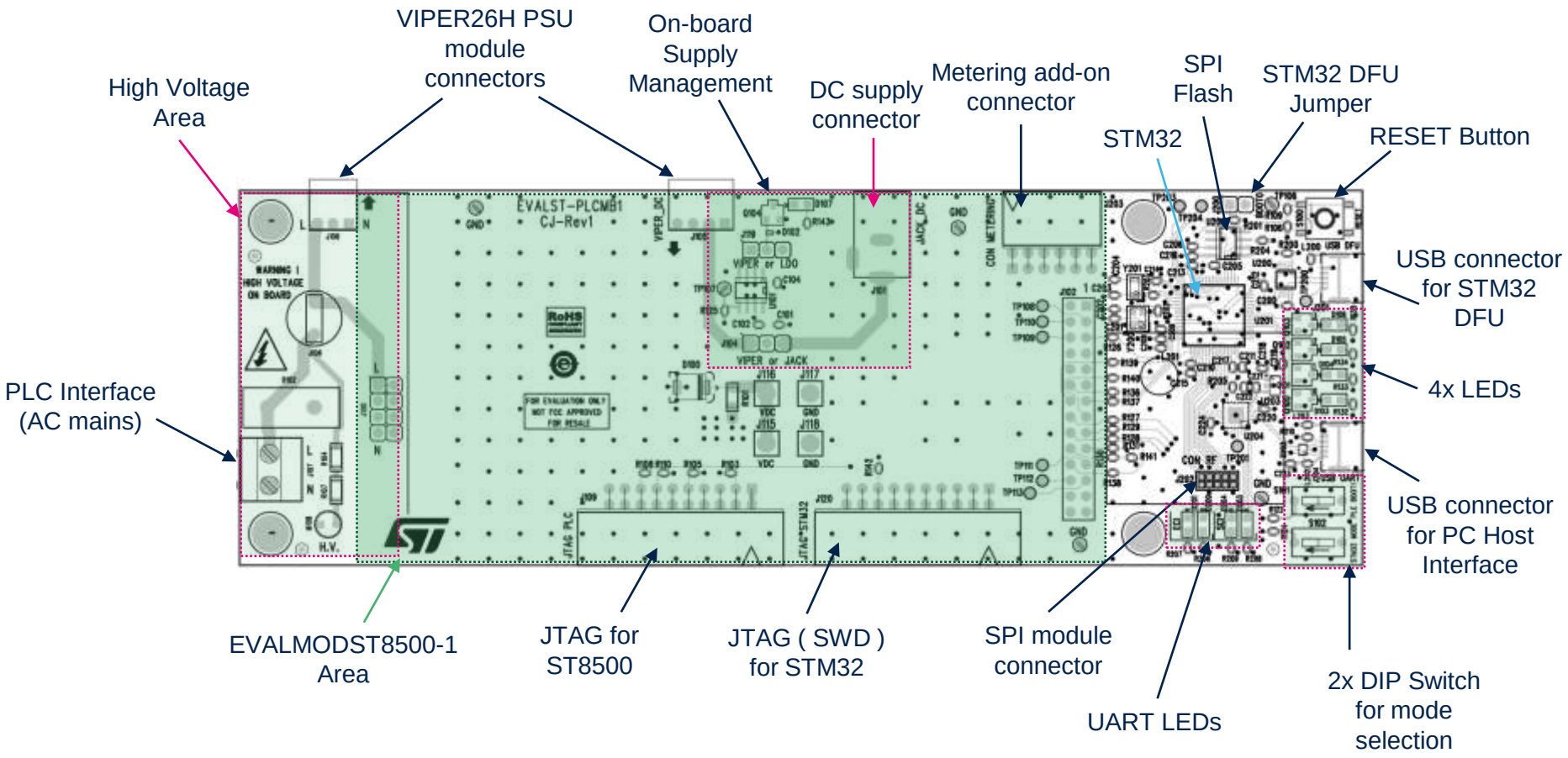


- For development purpose, the EVALKITST8500-1 allows to:
  - Use external DC Supply – no AC mains needed
  - Enable ARM Cortex debug capability for STM32 and ST8500 (for internal use only) through external JTAG probe
  - Enable GPIO for debug purpose (available on connector)

EVALMODST8500-1 description

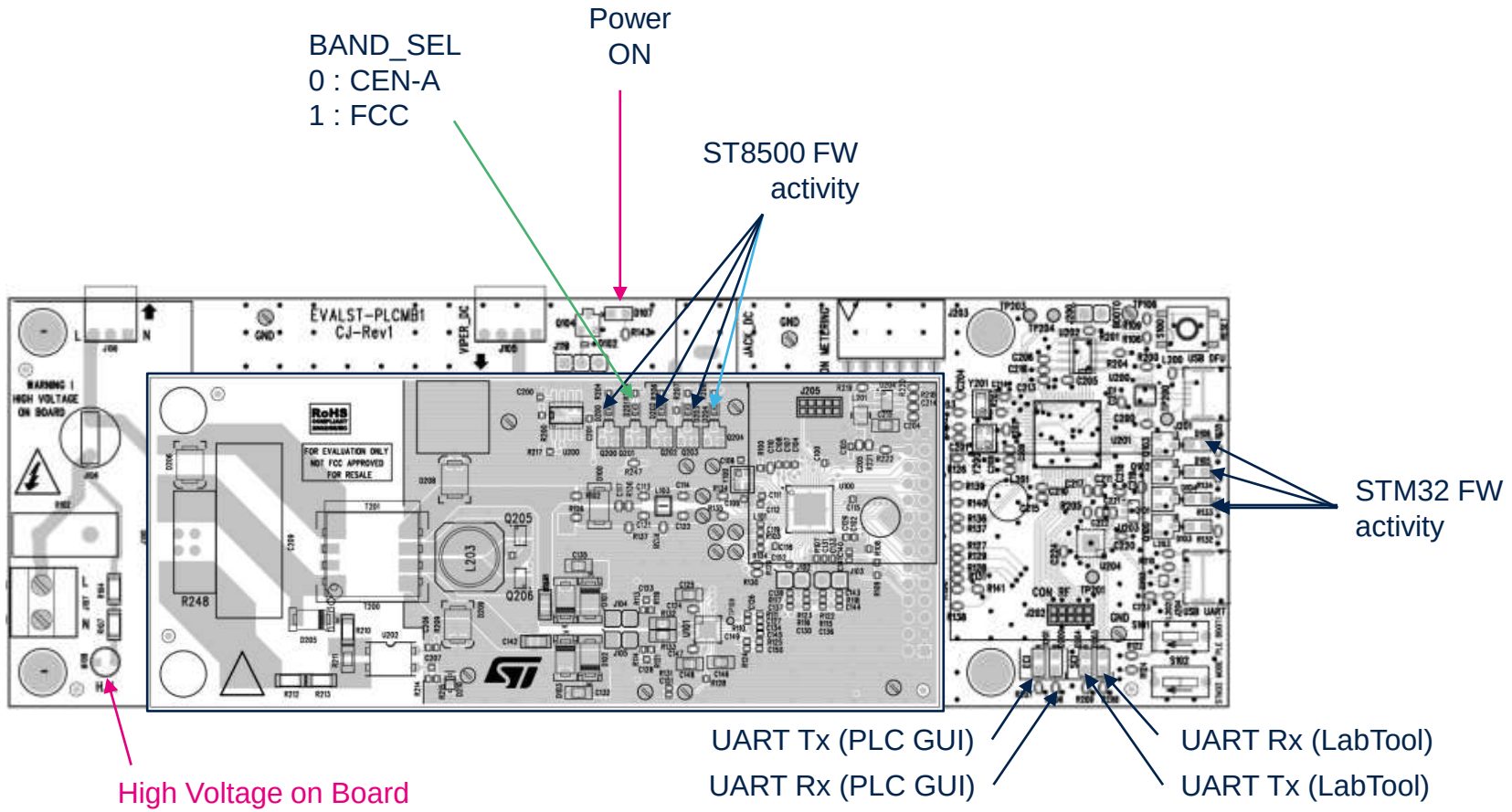


EVALST-PLCMB1 description

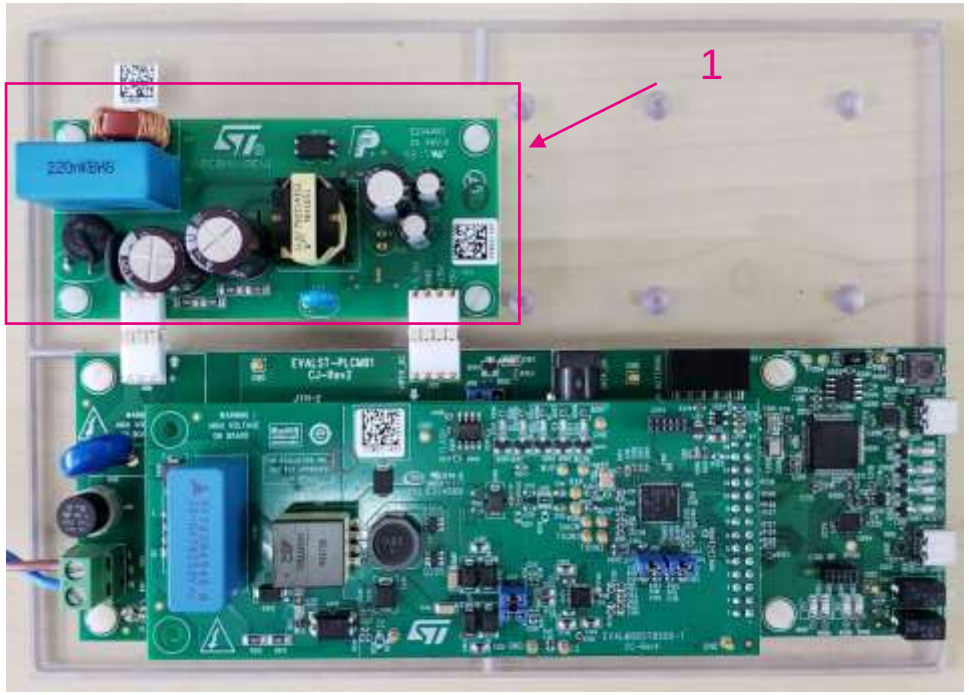


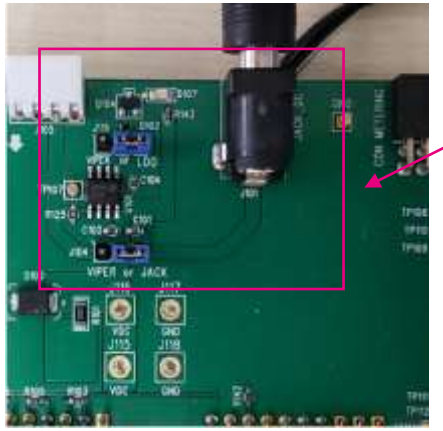
EVALKITST8500-1: LEDs

- After power-up and ST8500 boot, here is the mapping of the LEDs:



EVALKITST8500-1: DC operation

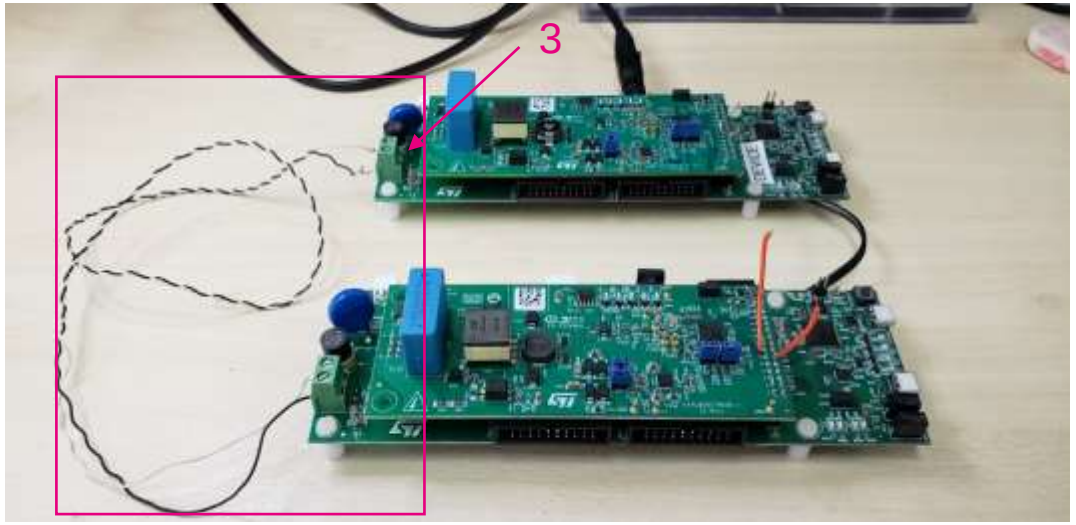




(1) Remove the power supply board

(2) Change J119 to LDO and J104 to JACK position and then connect to a 12V~15V DC power supply

(3) Connect J107 connector to the DC bus

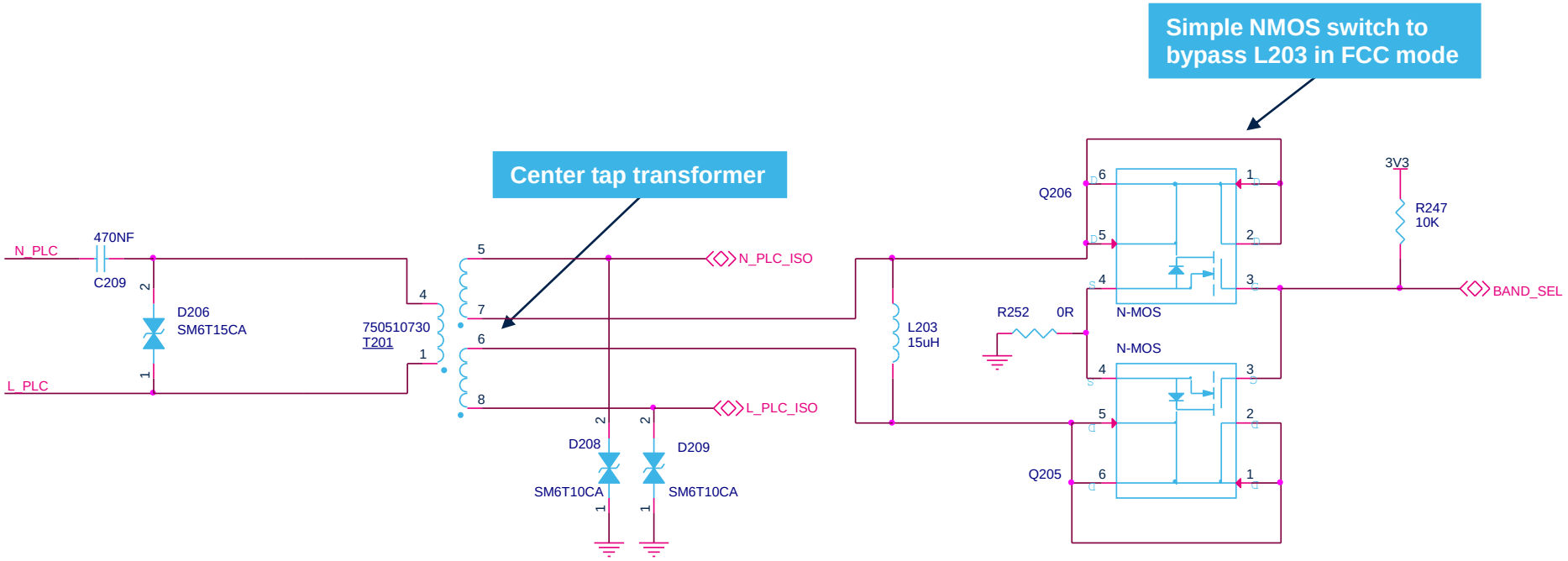


EVALKITST8500-1
HW design and EMC compliance

life.augmented

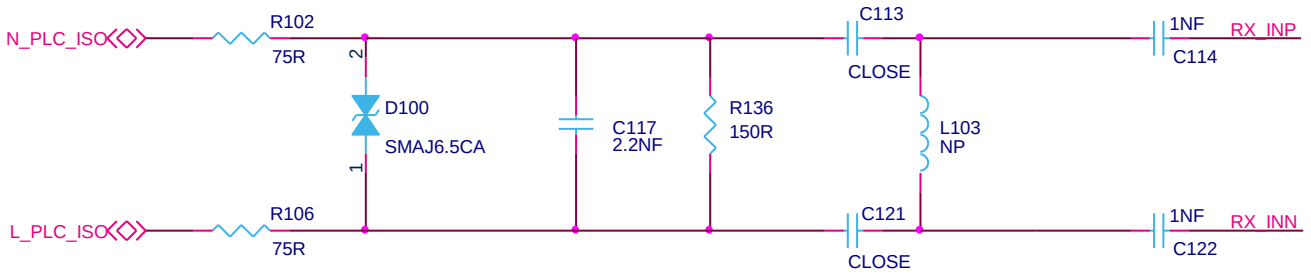
TX section

- ST patented solution for automatic CEN A – FCC tuning



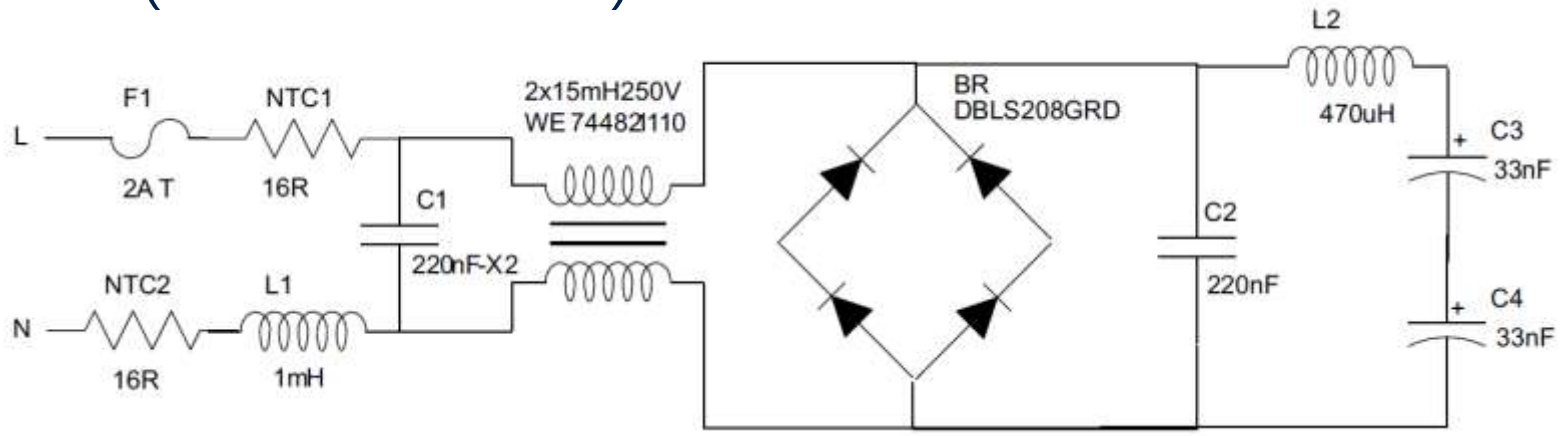
RX section

- Large CEN A to FCC frequency response
- Very low BOM solution
- -6 dB to match TX (up to 30 Vp-p) and RX (max 15 Vp-p) dynamic range



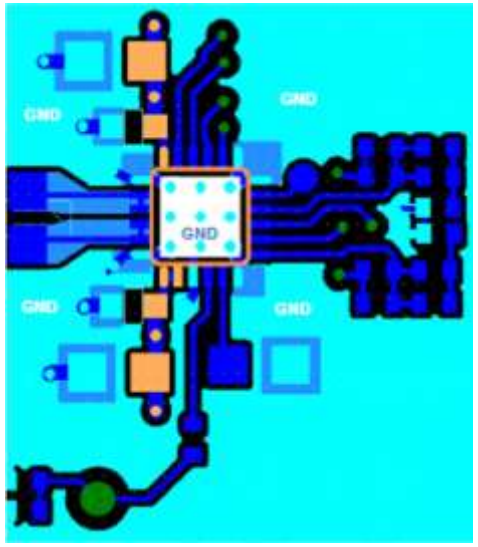
Power supply requirements for PLC performance

- Power budget:
  - VCC target value = 15 V dc
  - 0.7 A dc minimum current required on VCC for STLD1 to drive 2 Ω line impedance
  - 3V3 + 1V1 power budget: < 200 mW
  - Minimum power budget = (15 V * 0.7 A * 50% duty cycle) + 0.2 = 5.5 W
- EMI filter design:
  - L-C differential noise filtering + CM choke as first stage
  - Target: minimize noise injected to the power line + increase input impedance
  - Typical schematics (EVALKITST8500-1):

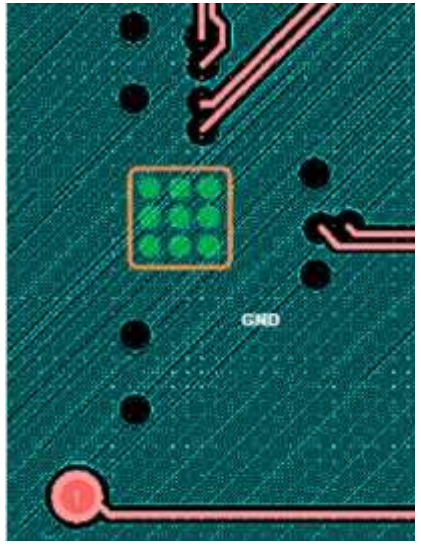


PCB guidelines

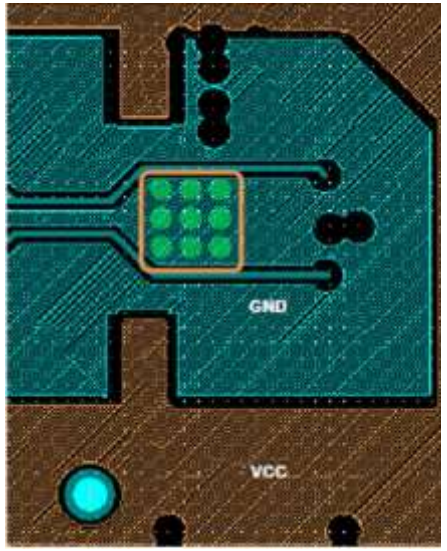
- See AN5120 + EVALKITST8500-1 package on st.com/powerline for full details
- Key points:
  - Good RF shielding by GND planes (below and between tracks) + short tracks to optimize EMC/EMI
  - Design for STLD1 thermal performance:
    - TOP: thermal pad with 3x3 via array
    - INNER: fill with GND the area below the device – NO cutting traces below the STLD1 thermal pad
    - BOTTOM: large GND area extending to the border of the PCB with possibly no cutting traces + via encroaching for best thermal pad soldering



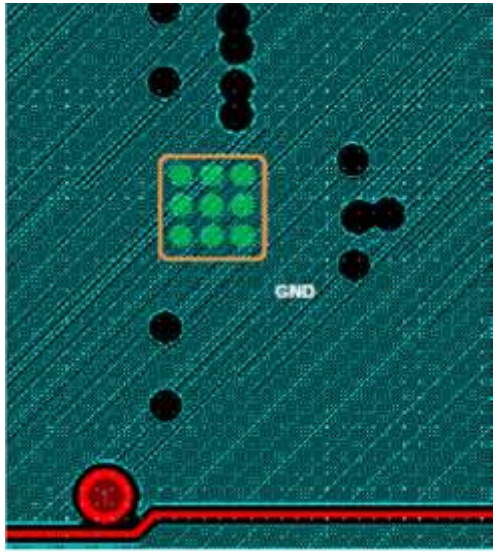
TOP



INNER1 (GND)



INNER2 (POWER)



BOTTOM

EMC compliance

- EN50065 compliance tests PASSED by EVALKITST8500-1

Type	Basic standard	Test	Result
PLC transmission: conducted measurement	EN 50065-1	Bandwidth measurements	PASS(1)
	EN 50065-1	Maximum output levels	PASS(1)
Conducted disturbance measurements	EN 50065-1, EN 55022	Conducted emissions (9 kHz - 30 MHz)	PASS(1), (2)
Radiated disturbance measurements	EN 50065-1, EN 55022	Radiated emissions (30 MHz - 1 GHz)	PASS(2)
Radiated immunity	EN 61000-4-3	RF radiated fields immunity test (80 - 1000 MHz, 10 V/m)	PASS
	EN 61000-4-8	Magnetic 50 Hz field immunity test (100 A/m, 300 A/m)	PASS
Contact/radiated immunity	EN 61000-4-2	Electro-static discharges immunity test (8 kV contact and air mode)	PASS(3)
Conducted immunity	EN 61000-4-6	RF conducted signals immunity test (150 kHz - 80 MHz, 10 V rms)	PASS(3)
	EN 50065-2-3	Narrow-band signals immunity test (95 kHz - 150 kHz; 150 kHz - 30 MHz)	PASS(3)
	EN 61000-4-4	Fast transients immunity test (2 kV, 5 kHz)	PASS(3)
	EN 61000-4-5	Surge immunity test (4 kV, common mode and differential mode)	PASS(3)
	EN 61000-4-11	Power voltage dips and interruptions (30% - 10 ms; 60% - 100 ms; 100% - 5 s)	PASS(3)
Input impedance measurement	EN50065-7	RX impedance	PASS(1), (2)
		TX impedance	PASS(1)

1. Related to the specific PLC protocol implementation.
2. Results impacted by the VIPer26H power supply module.
3. In case of non-metering applications, communicating outside the CENELEC A band, please refer to the immunity requirements listed in the EN50065-2-1 document, which may set lower limits for some tests.


tecnalia

Test Report
No. B41-18-BH-I1

ENAC

Tests according to PE.EES-10-E

TEST SAMPLE	PRIME 1.4 COMMUNICATION BOARD
MODEL	EVALKITST8500-1
MANUFACTURER	STMicroelectronics S.r.l.
APPLICANT	STMicroelectronics S.r.l.
	Via C. Olivetti, 2. Agrate Brianza 20864 (MB) - ITALY
DATES OF RECEPTION	10/01/2018 (sample 1 and 2)
DATES OF TEST	From 10/01/2018 to 10/22/2018
DATE OF ISSUE	11/05/2018

Technical Responsible

Alfosa Hernández

tecnalia

EVALKITST8500-1
G3-PLC PHY performance

life.augmented

EVALKITST8500-1: G3-PLC CEN-A PHY performance summary

TX Power
(differential RMS-AVG)

EN50065 LISN	2 Ω LISN
129* dBµV	122* dBµV

* = value measured on LISN RF port + 6 dB

Power consumption

Supply rail	RX	TX
3V3 + 1V1	140 mW	170 mW
VCC = 15 V	15 mW	600 mW

Sensitivity and data rates

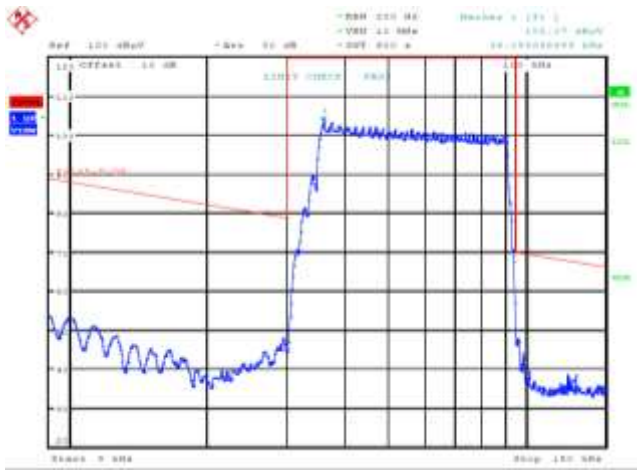
Modulation	Sensitivity (dBµV rms)	PHY Data rate (kbps), IFS < CIFS
CROBO	24	4.8
DROBO	25	5.2
CBPSK	27	17.1
DBPSK	30	18.5
CQPSK	30	27.6
DQPSK	33	30.5
C8PSK	34	35.2
D8PSK	40	38.4

G3 PHY Performance

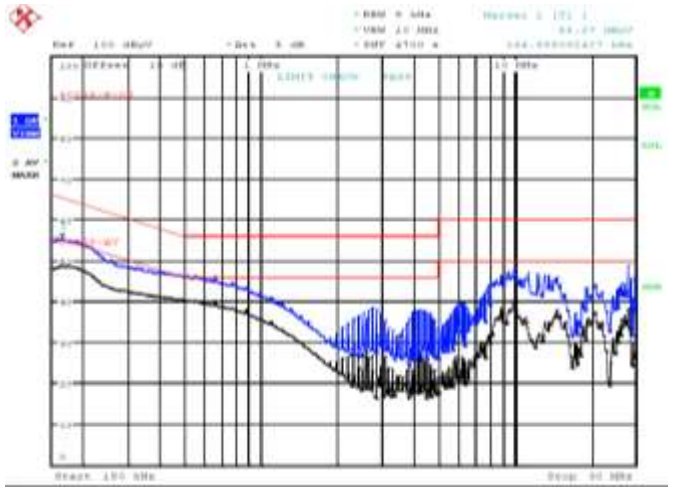
Performance tests PASS in LAN lab

EN50065-1 Conducted Emission tests

PASS



PASS



EVALKITST8500-1: G3-PLC CEN-B PHY performance summary

TX Power
(differential RMS-AVG)

EN50065 LISN	2 Ω LISN
126* dBµV	122* dBµV

* = value measured on LISN RF port + 6 dB

Power consumption

Supply rail	RX	TX
3V3 + 1V1	140 mW	170 mW
VCC = 10 V	10 mW	400 mW

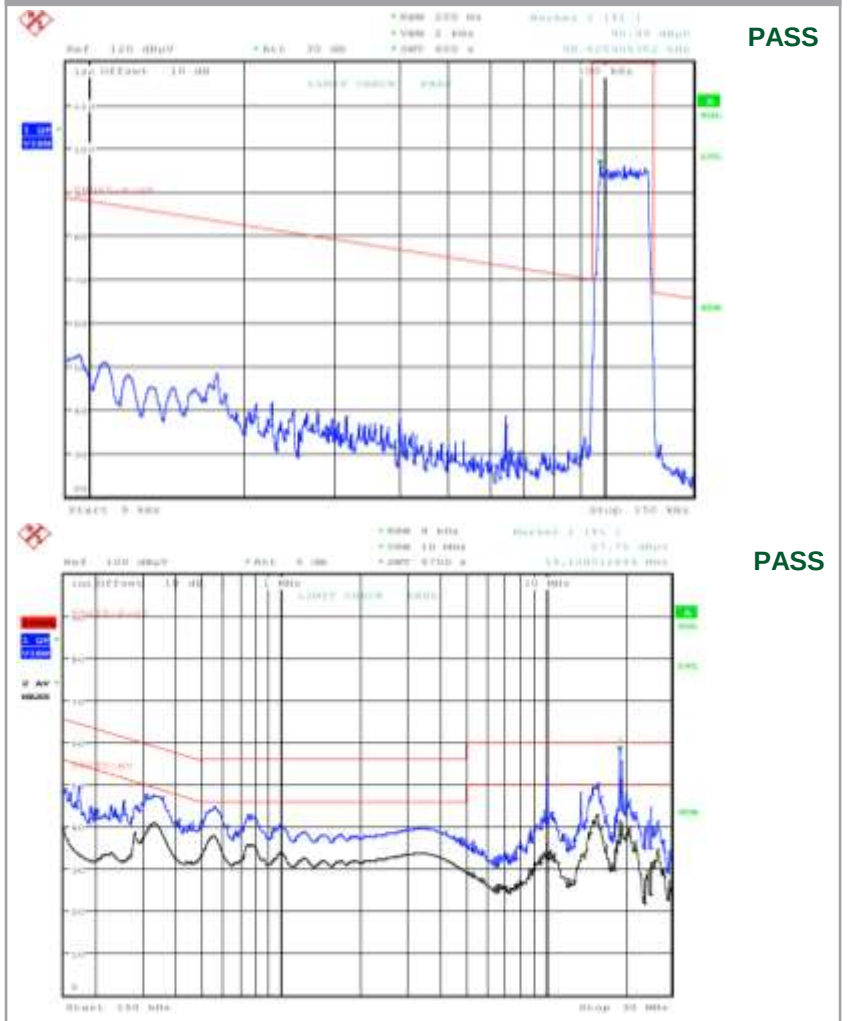
Sensitivity and data rates

Modulation	Sensitivity (dBµV rms)	PHY Data rate (kbps), IFS < CIFS
CROBO	20	1.7
DROBO	21	2
CBPSK	23	7.5
DBPSK	26	8.8
CQPSK	26	13.5
DQPSK	30	15.2
C8PSK	31	18.1
D8PSK	34	19.9

G3 PHY Performance

Performance tests PASS in LAN lab

EN50065-1 Conducted Emission tests



PASS

PASS

EVALKITST8500-1: G3-PLC FCC PHY performance summary

TX Power
(differential RMS-AVG)

EN50065 LISN	2 Ω LISN
127* dBµV	120* dBµV

* = value measured on LISN RF port + 6 dB

Power consumption

Supply rail	RX	TX
3V3 + 1V1	160 mW	190 mW
VCC = 15 V	15 mW	600 mW

Sensitivity and data rates

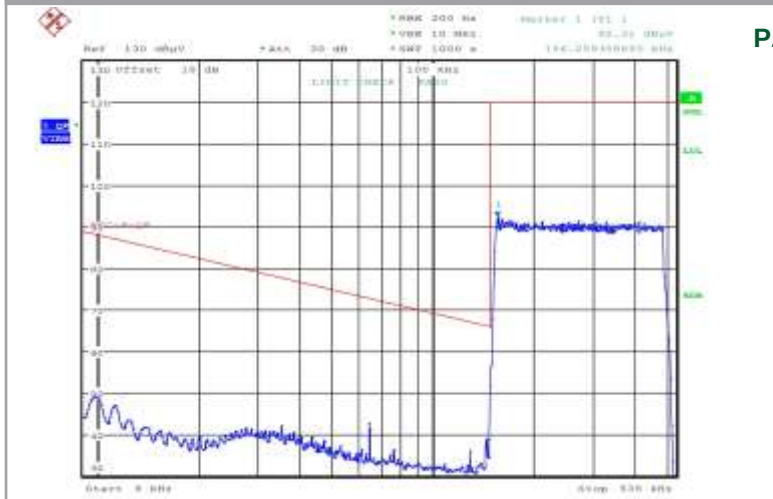
Modulation	Sensitivity (dBµV rms)	PHY Data rate (kbps), IFS < CIFS
CROBO	30	31.3
DROBO	33	33.9
CBPSK	35	103
DBPSK	38	112
CQPSK	38	171
DQPSK	42	180
C8PSK	42	211
D8PSK	45	225

G3 PHY Performance

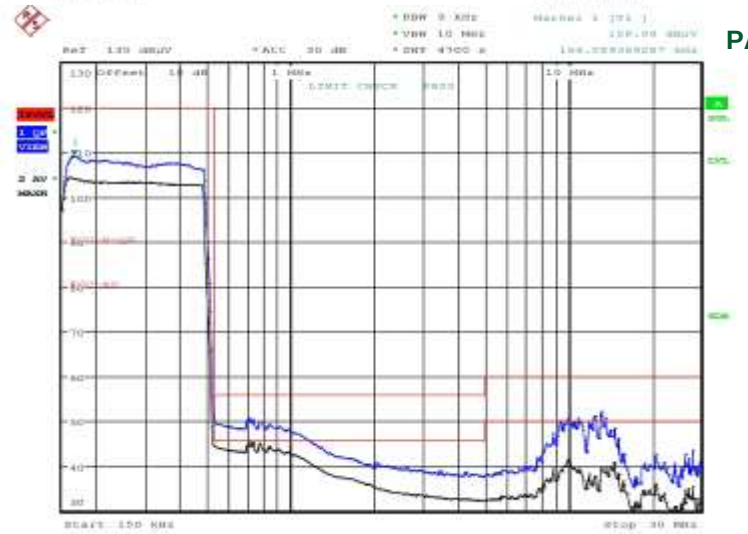
Performance tests PASS in LAN lab

ITU-T G.9901 (06/2017) Conducted Emission tests

PASS



PASS



EVALKITST8500-1: power dissipation of STLD1 line driver

- Maximum power dissipation that the Line Driver can sustain without Over-Temperature Protection intervention
- Measured with G3-PLC at PHY level vs. TX duty cycle and coupling configuration

Line coupling Configuration	R_load	TX duty cycle	Max Signal level @ R_load	Average Line Driver dissipation	Zth_JA estimated
Single Ended	2 Ω	50%	1 V rms	1.8 W	26 °C/W
		99.5%	1 V rms	3.6 W	
Differential		50%	1.5 V rms	4.5 W	
		99.5%	0.5 V rms	3.7 W	

EVLKST8500GH868 / 915 overview

life.augmented

EVLKST8500GH868 / 915
Connectivity development kit for multiple applications

- Hybrid PLC&RF connectivity development kit based on ST market-proven and widely used connectivity chipsets ST8500, STLD1 and S2-LP
- For various PLC (35-500 kHz) and RF (868-915 MHz) frequency bands
- Modular design with PLC, RF and MCU modules for easy scalability thanks to the STM32 Open Development Ecosystem

STM32 Open Development Environment

Order code	Description
EVLKST8500GH868	Development kit
EVLKST8500GH915	Development kit
STSW-ST8500GH	Software package

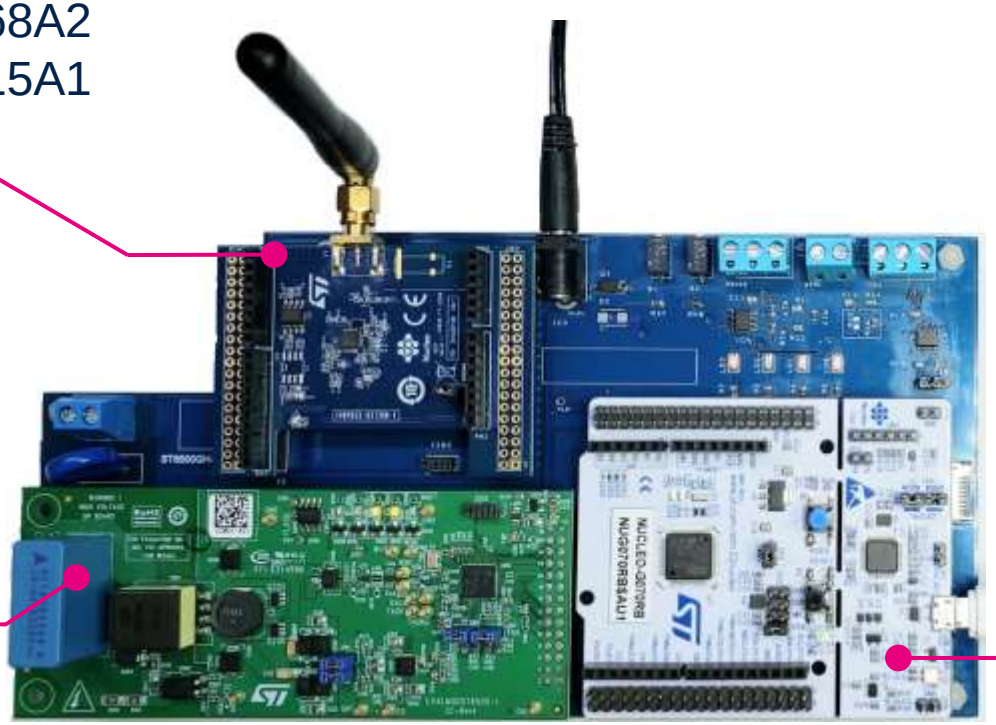
www.st.com/powerline

life.augmented

EVLKST8500GH868 / 915 development board

Features and Scalability

- ❑ X-NUCLEO-S2868A2
- ❑ X-NUCLEO-S2915A1



- ❑ ST8500 Module
- ❑ NUCLEO-G070RB

Features:

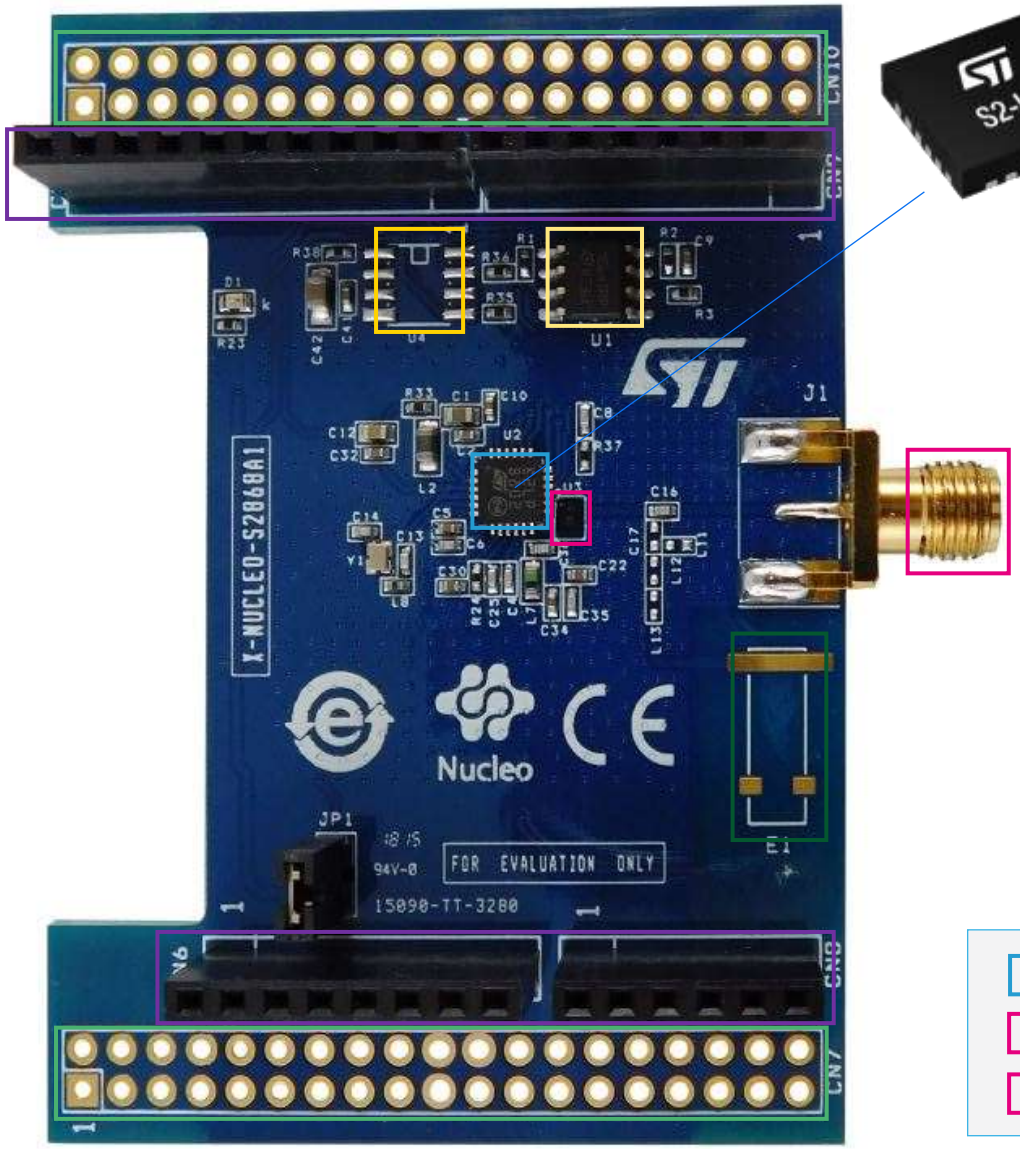
- ❑ RS485 interface
- ❑ CAN* interface
- ❑ SD Card connector for data logging
- ❑ SPI Flash for firmware storage
- ❑ ST8500 Boot Mode selection through S2
- ❑ STM32 Mode selection through S1

life.augmented

* check STM32 CAN availability

Compatibility with most of 64 pins NUCLEO boards

S2-LP: X-NUCLEO-S2868A2/915A1



X-NUCLEO HARDWARE:

- X-NUCLEO-S2868A2 (868 MHz)
- X-NUCLEO-S2915A1/STEVAL-FKI915V1 (915 MHz w/ PA)

STM32 Open Development Environment

S2-LPQTR
BALF-SPI2-01D3
SMA antenna
M95640
STSAFE-A100 (opt)
SMD antenna (opt)
ST Morpho connector (opt)
Arduino UNO R3 connector

life.augmented

NUCLEO-G070RB

STM32 NUCLEO Development Boards

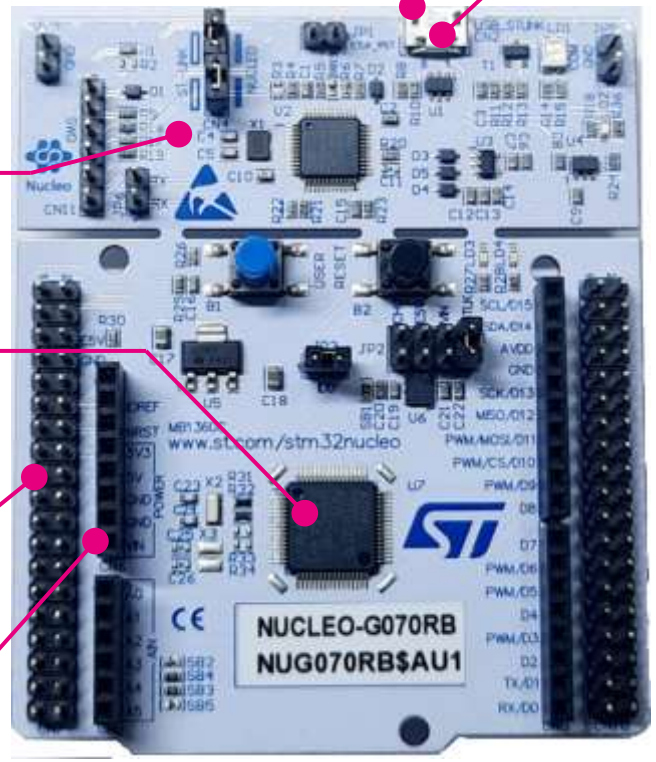
Board power supply
Through USB or
External source

Integrated debbuging
and programming
ST-LINK probe

STM32G070RB

Morpho
Extension header

Arduino™
Extension header



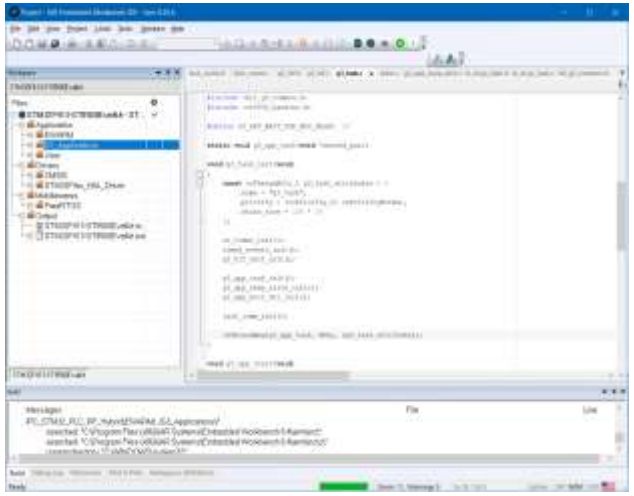
Virtual COM port used by
EVALKST8500GH868/915

- ARM Cortex-M0+ @ 64MHz
- 128KB FLASH, 36KB RAM
- 7-channel DMA controller
- 4x USART, 2x SPI, 2x I2C
- 11 Timers
- 12-bit ADC up to 16 ext. Channels
- Reset and power management

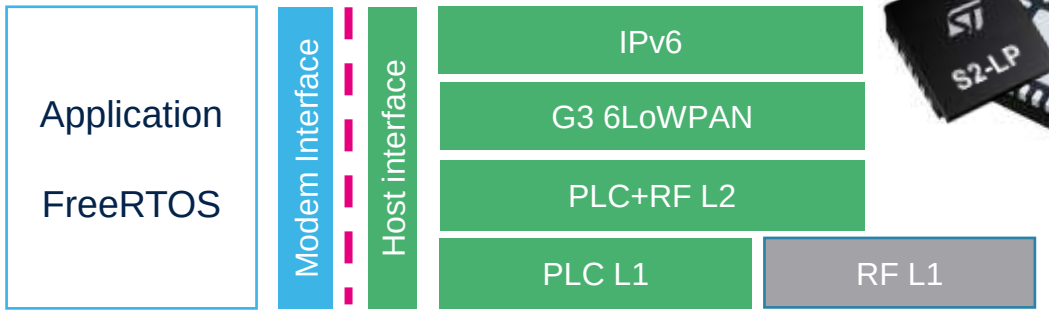
life.augmented

STM32 package for G3-PLC Hybrid PLC&RF application development

- **STSW-ST8500GH**: Complete software package for evaluation and application development
  - ST8500 G3-PLC Hybrid PLC&RF library
  - STM32 source code framework based on CubeMX, ready for customer application firmware development and integration



G3-PLC keep-alive example



life.augmented

ST8500 Hybrid Platform

Order Codes

- A complete and scalable platform:

Order code	Description	Package
ST8500TR	Programmable Modem + AFE	VFQFPN 56 7x7x1 mm
STLD1TR	Line Driver	QFN-24L 4x4x1 mm
S2-LPQTR	Sub-GHz RF transceiver	QFN-24L 4x4x1 mm

- Further information and full design support available at:

www.st.com/powerline

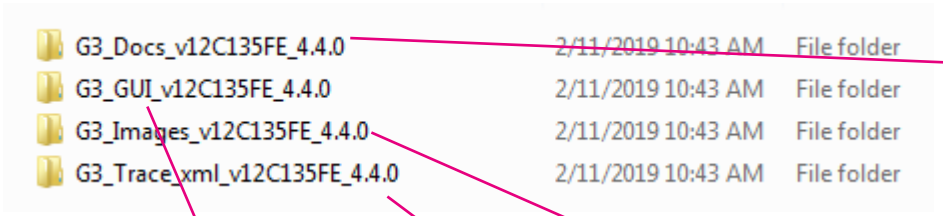
www.st.com/spirit

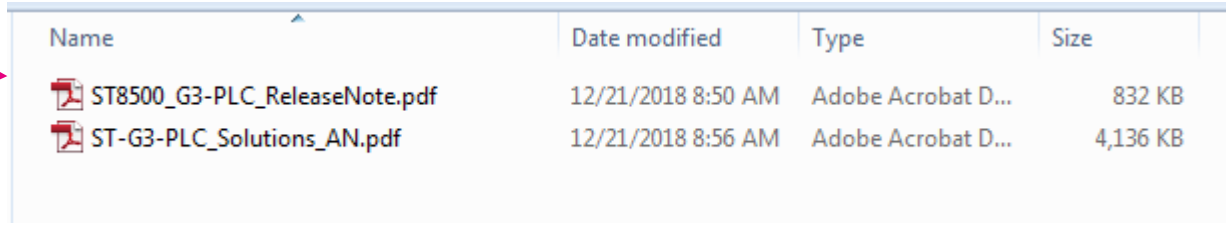
life.augmented

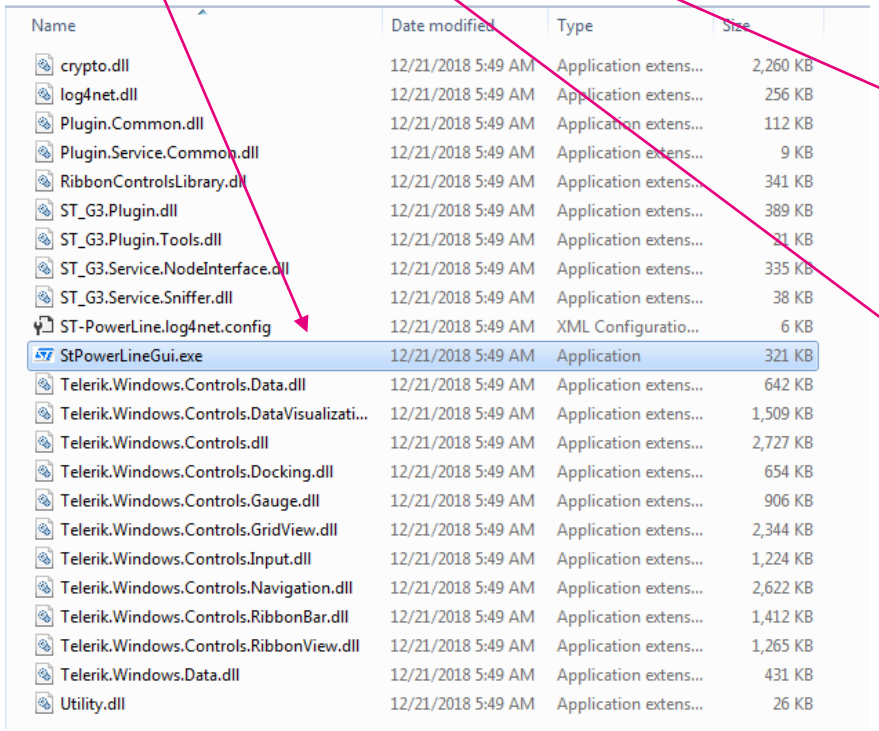
ST8500 evaluation - quick start

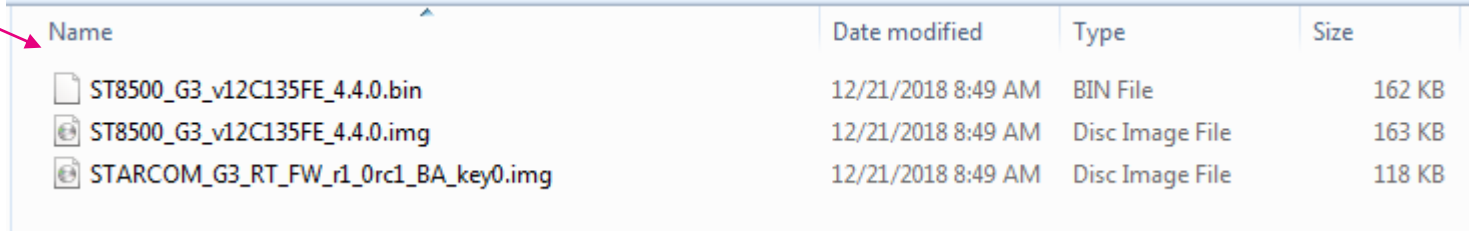
life.augmented

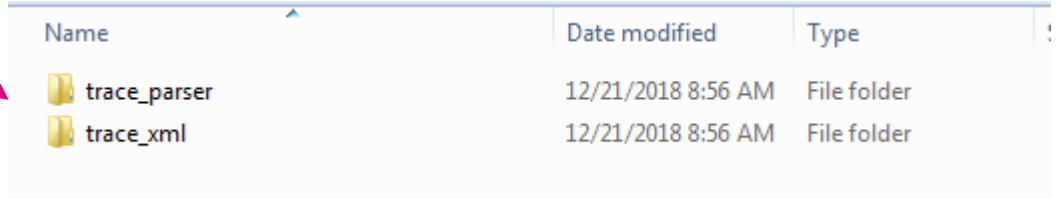
ST8500 G3-PLC evaluation package











life.augmented

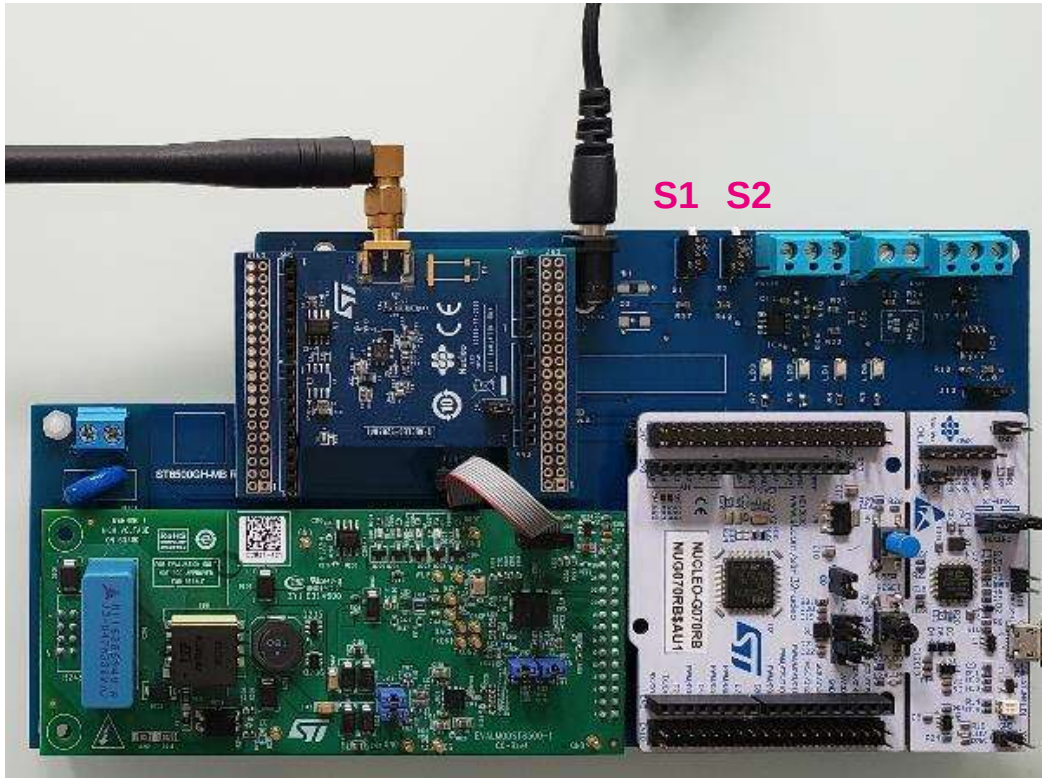
Platform mode configuration

STM32 Boot mode	EVALKITST8500-1	EVLKST8500GH868 / 915
Normal mode (MCU host)	S102 up	S1 up
Pass-through mode (PC host)	**S102 down**	**S1 down**

ST8500 Boot mode	EVALKITST8500-1	EVLKST8500GH868 / 915
Boot from UART host interface	**S101 up**	S2 up
Boot from ST8500 module SPI FLASH	S101 down	**S2 down**

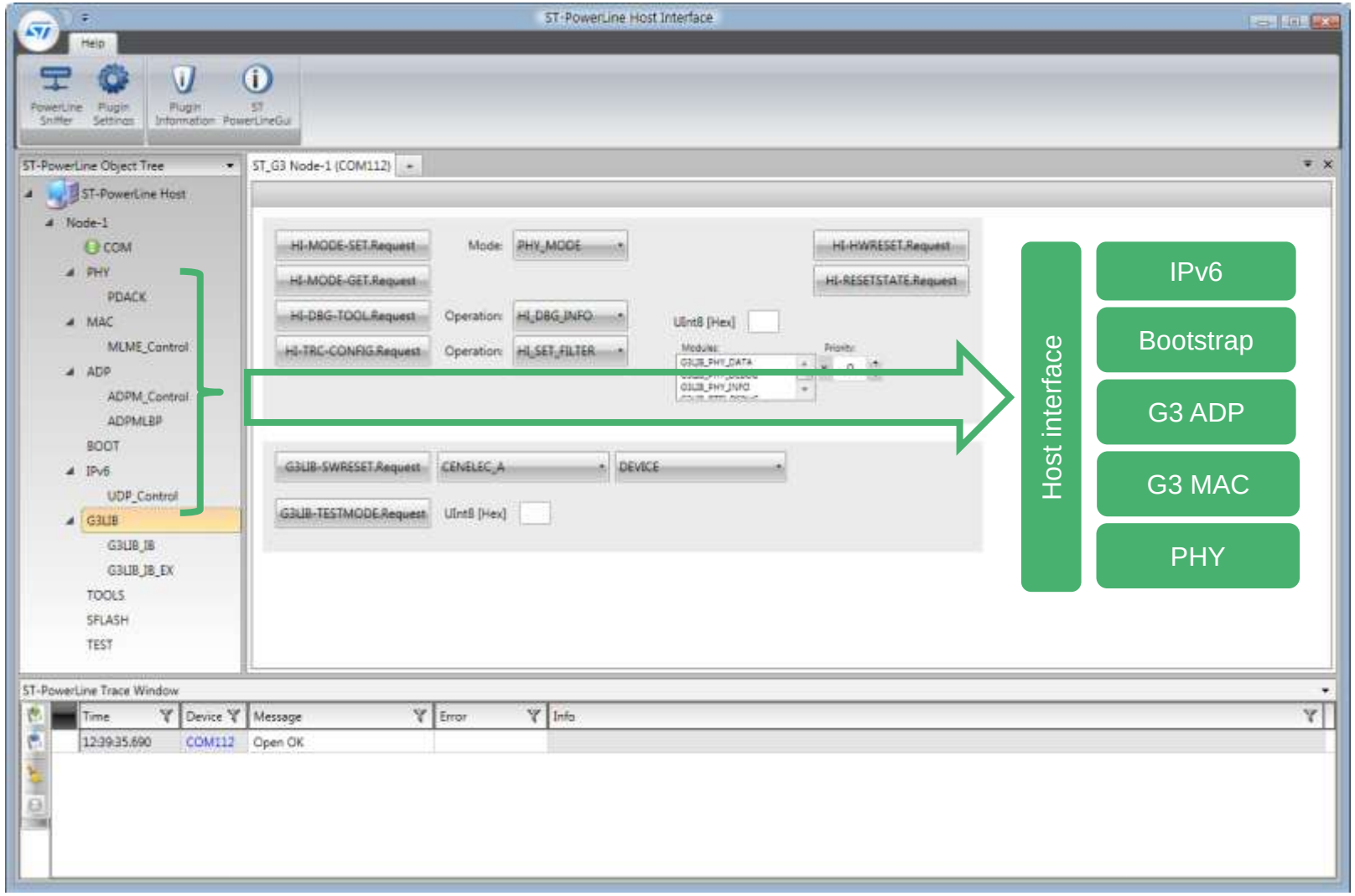
EVALKITST8500-1

EVLKST8500GH868 / 915



life.augmented

G3-PLC GUI: Navigate the node tree



- Explore Node tree:
  - Configuration of the G3 library
  - Read/Write attributes of G3 protocol
- Send/Receive data:
  - PHY layer
  - MAC layer
  - ADP layer
  - IPv6 layer
- Update SPI FLASH
- Power Line Sniffer feature
- Trace window

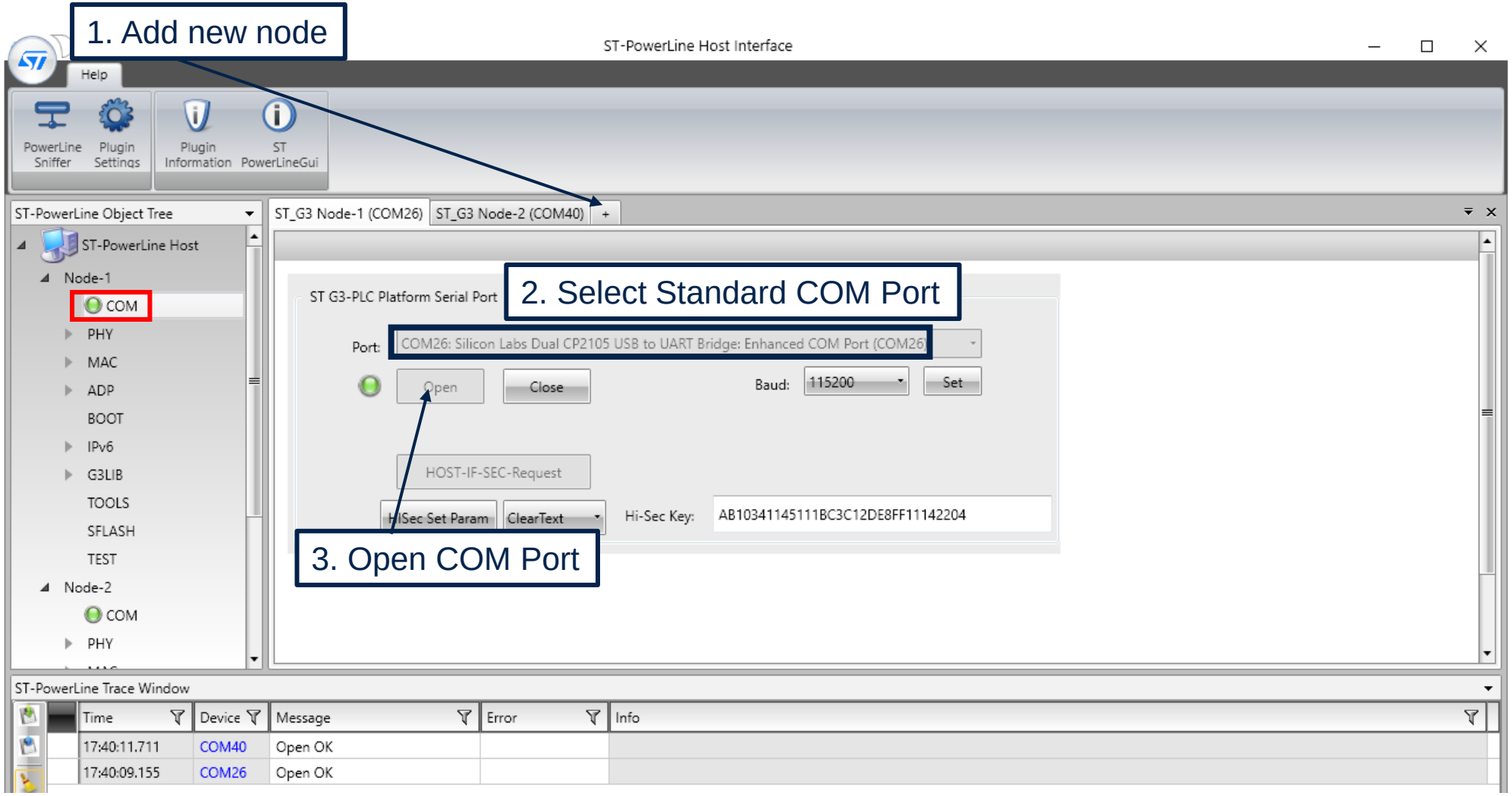
life.augmented

Physical layer

Communication setup steps

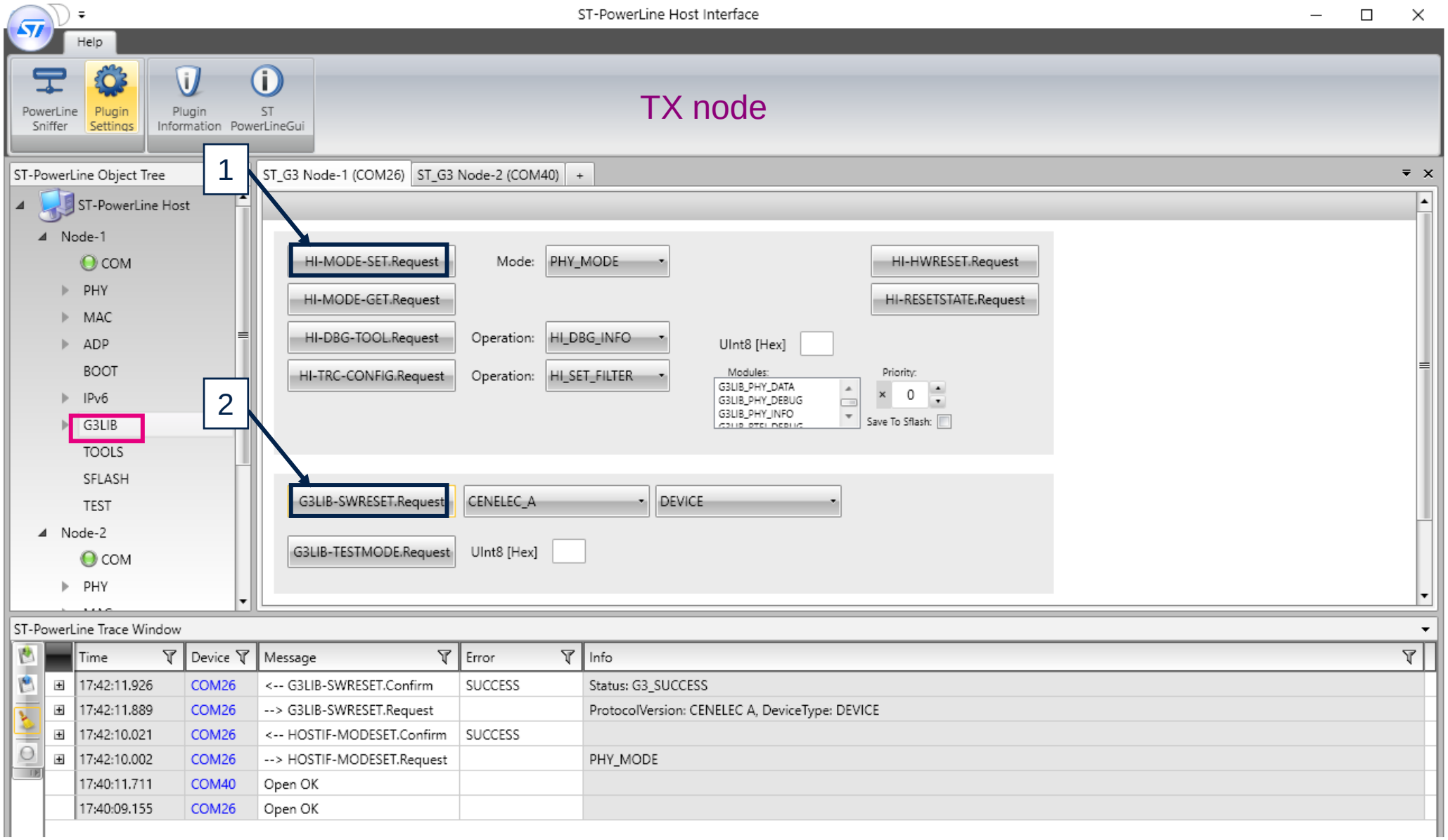
1. Open G3 GUI
2. Add two new nodes
3. Open Standard COM port for both nodes
4. Configure TX node
5. Configure RX node
6. Start reception
7. Start transmission
8. View statistics

G3 GUI – UART connection

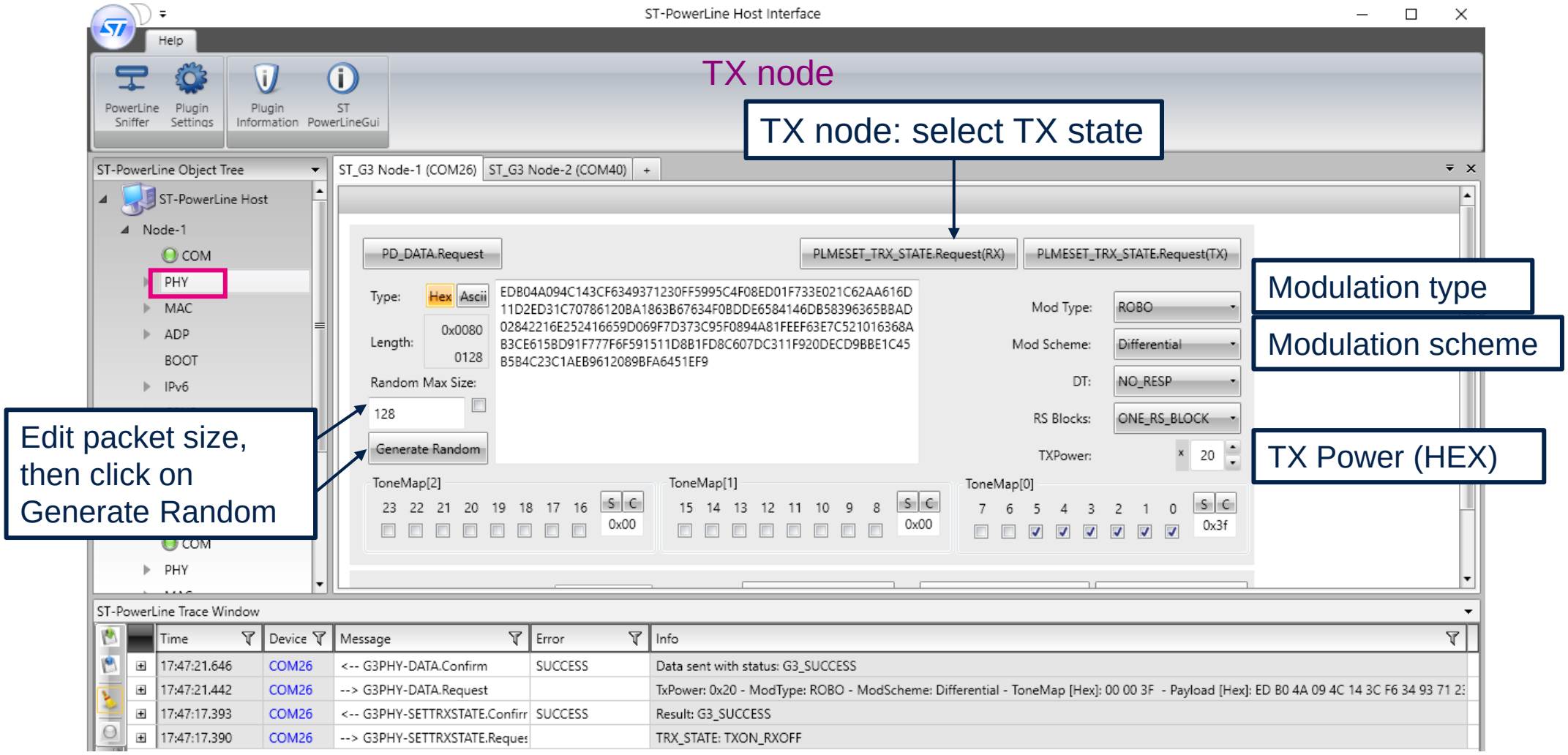


Note: you need to create 2 nodes for communication test

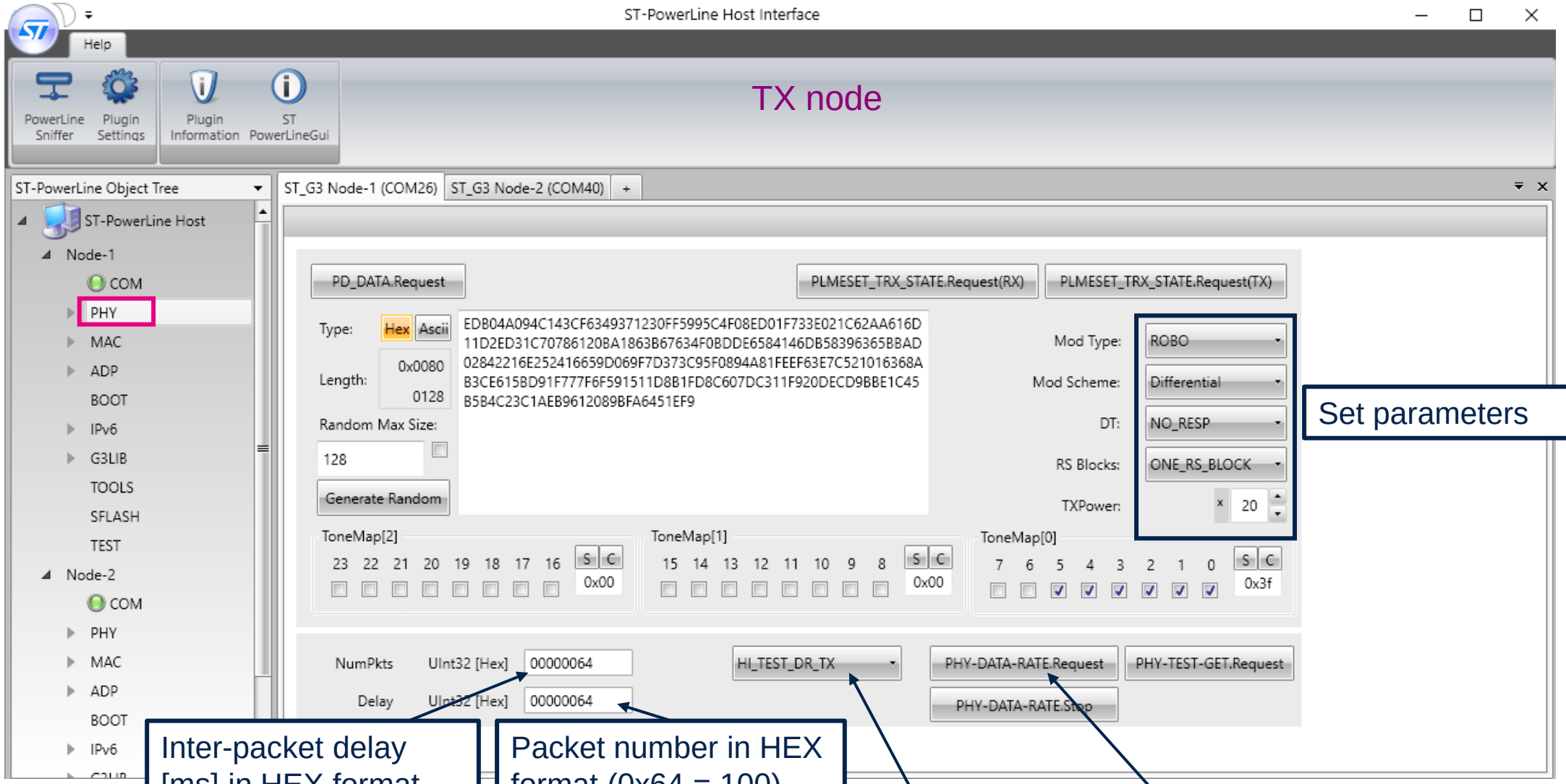
G3 GUI – node initialization



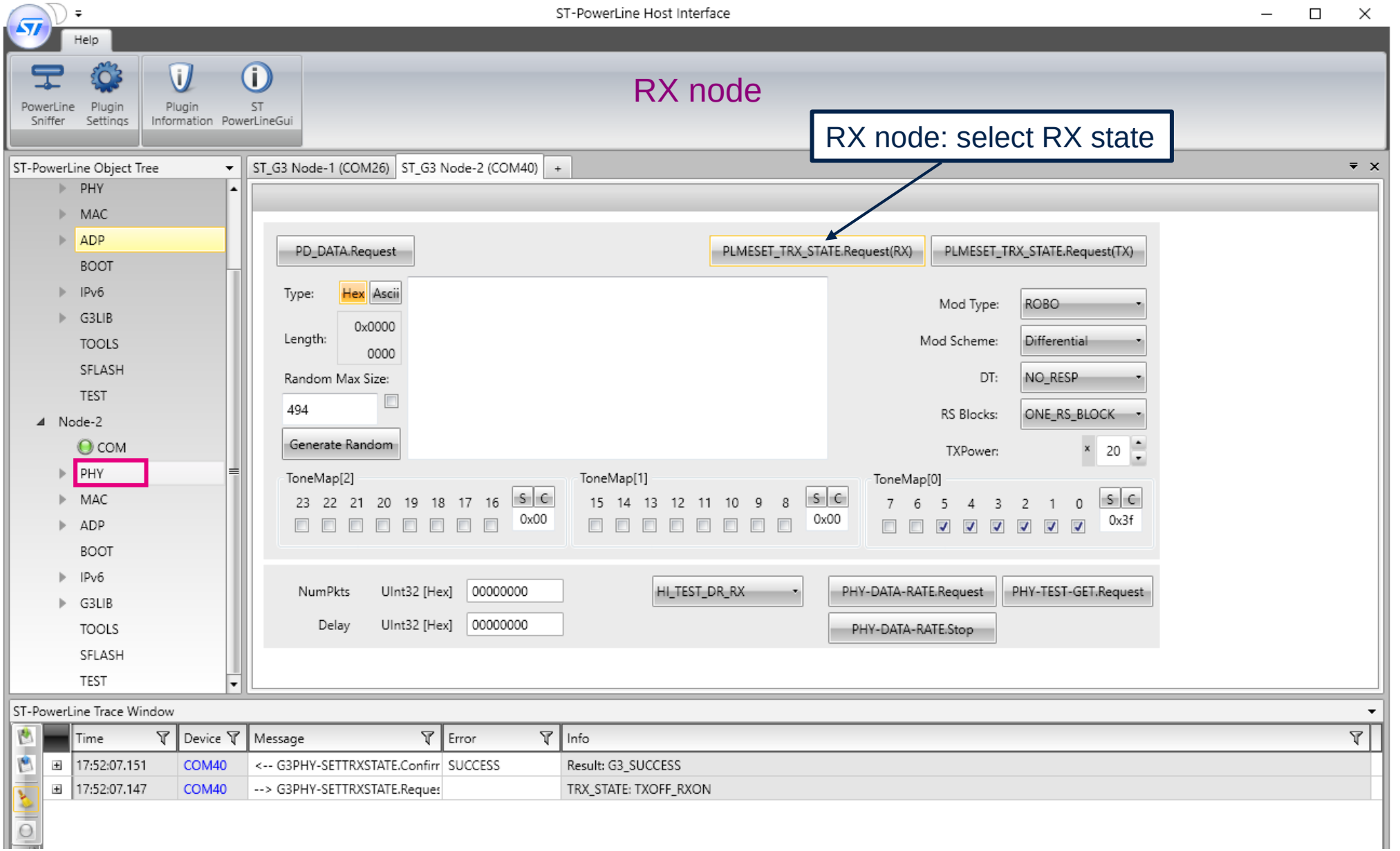
G3 GUI – TX settings



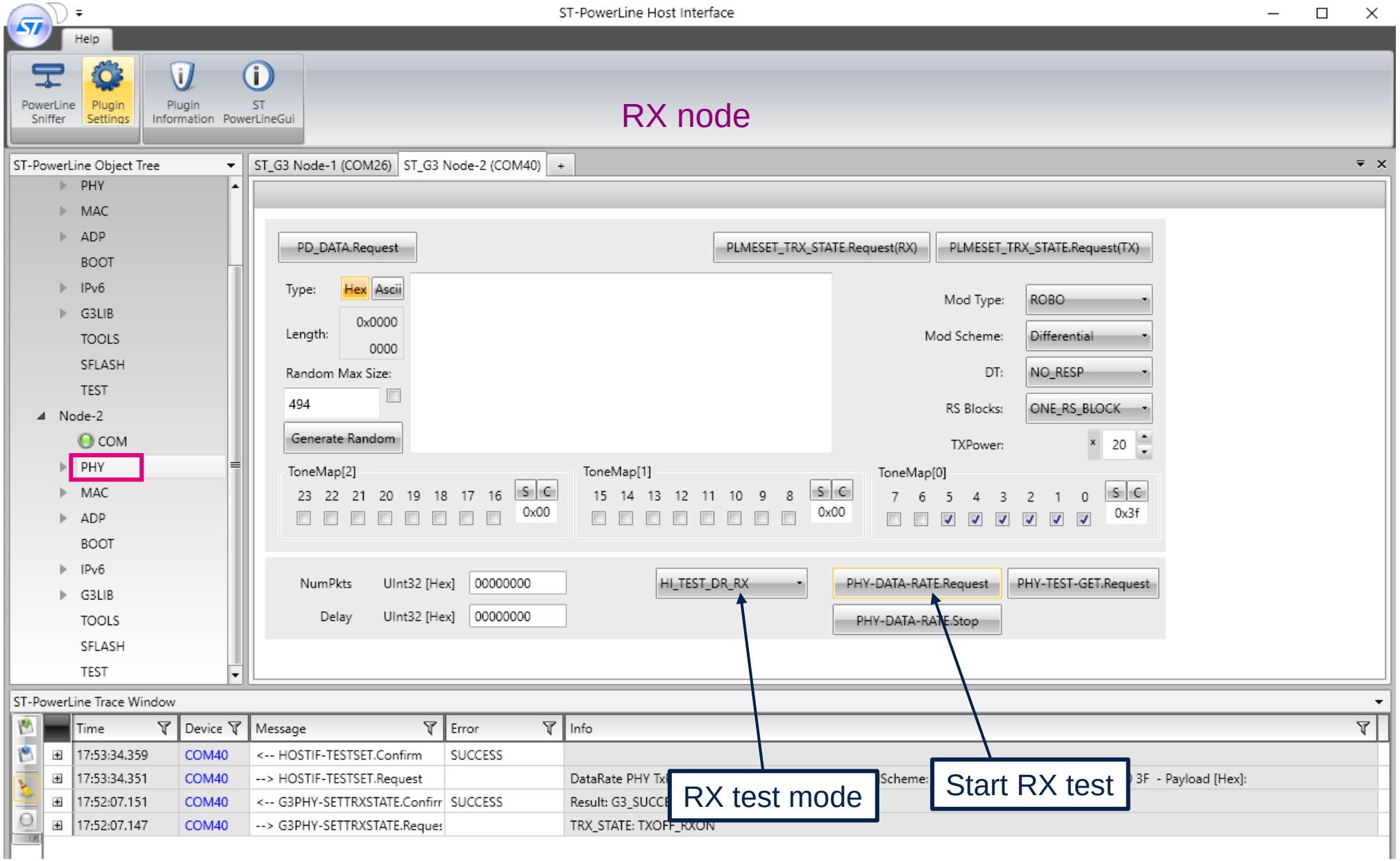
G3 GUI: TX output power measurements



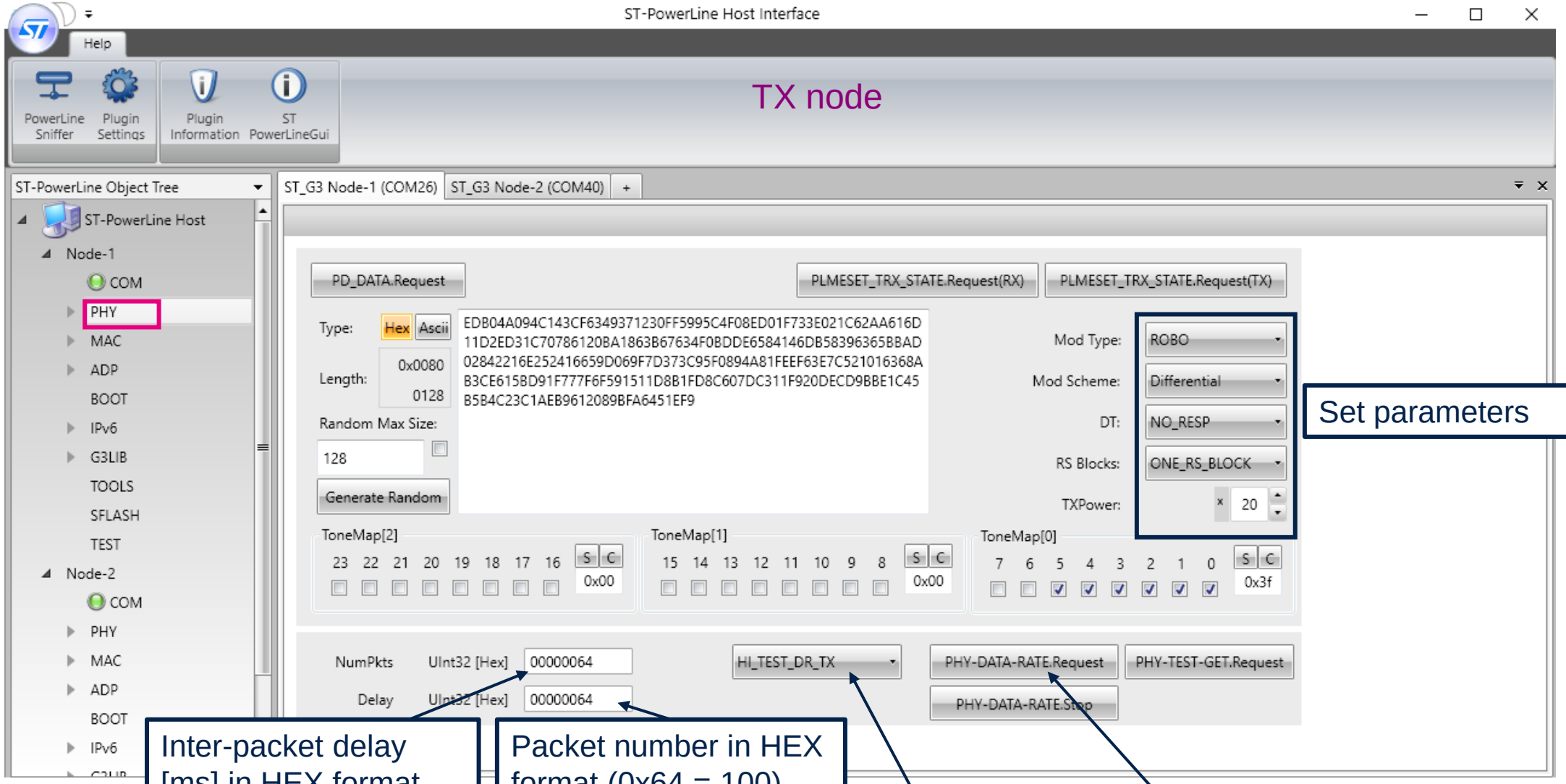
G3 GUI – RX setting



G3 GUI – RX start

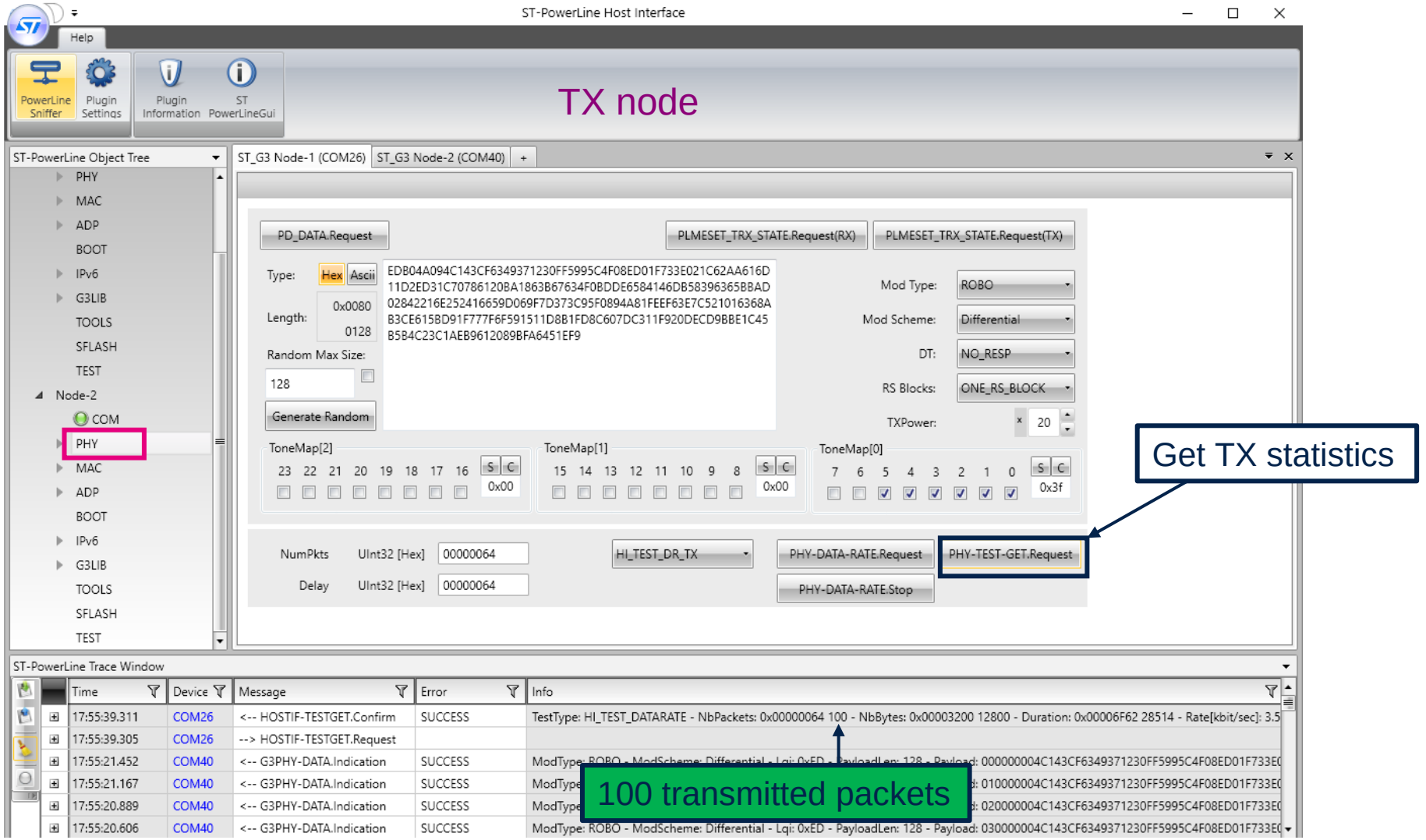


G3 GUI: TX start



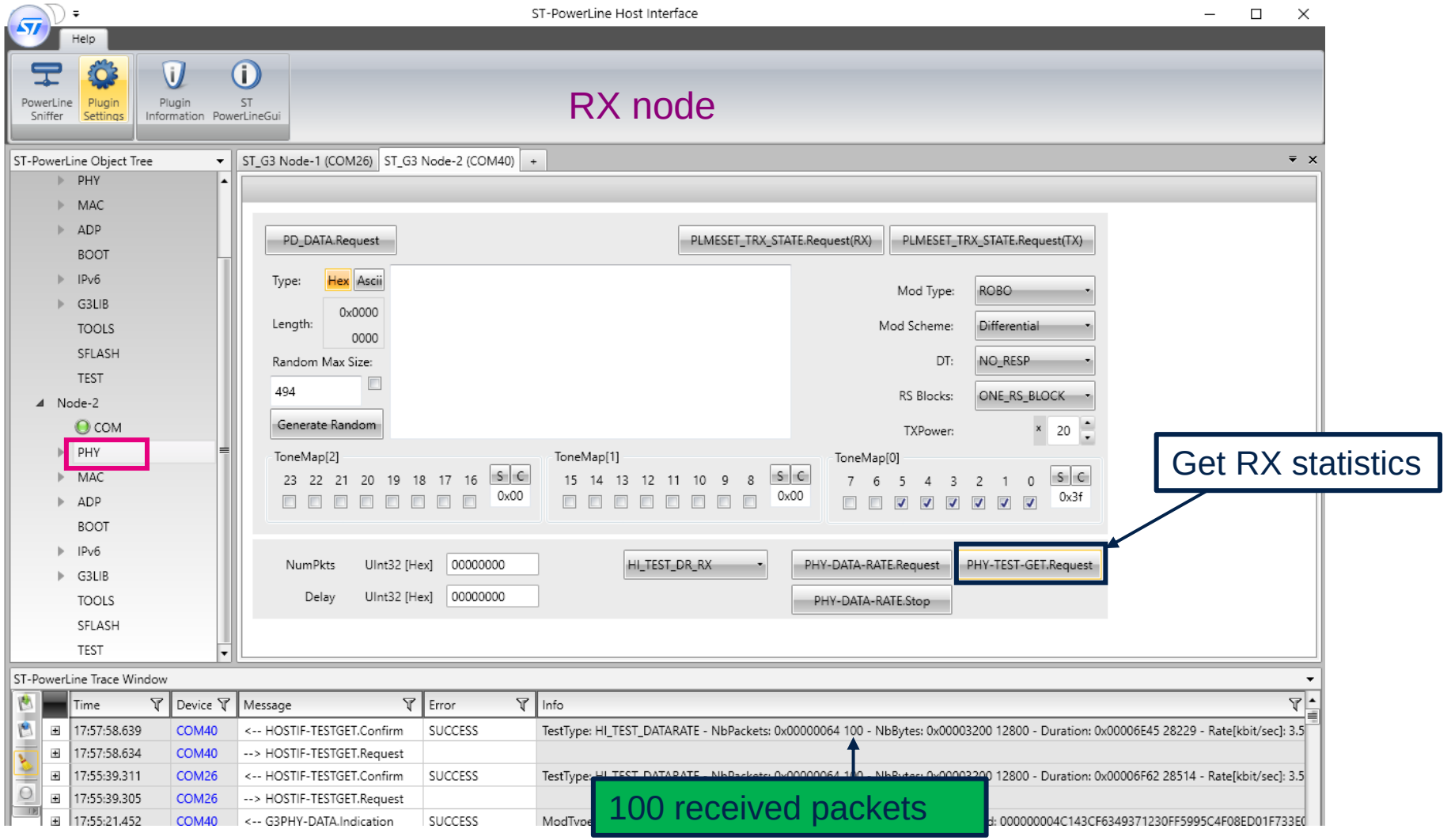
G3 GUI – TX statistics

Once the transmission has finished, you can see the statistics related to TX packets



G3 GUI – RX statistics

Once the transmission has finished, you can see the statistics related to RX packets

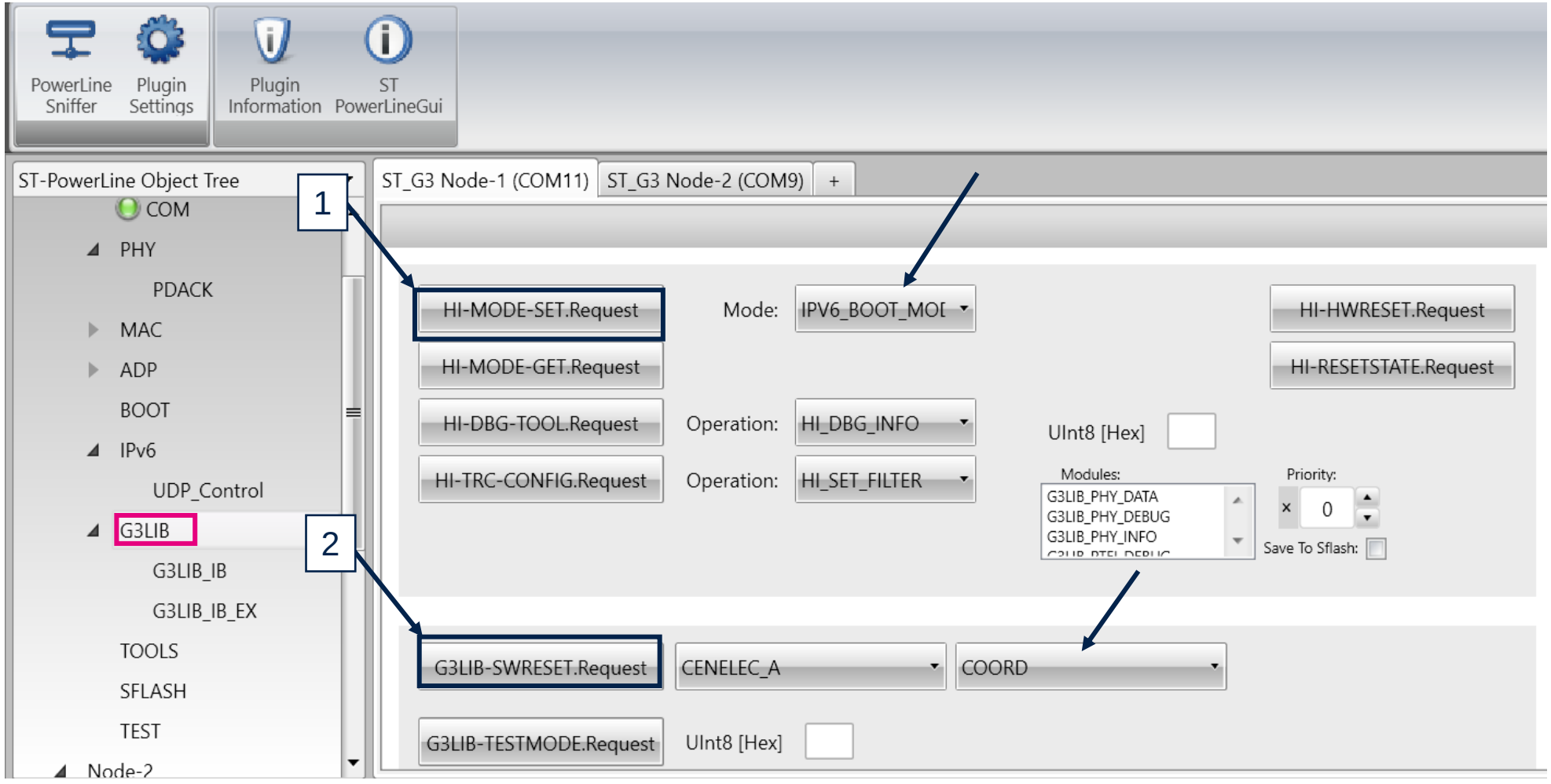


IPv6 layer

Communication setup steps

1. Open G3 GUI
2. Add two new nodes
3. Open Standard COM port for both nodes
4. Set one node as COORD (COM11 in this example) and the other as DEVICE (COM9 in this example), in IPv6 boot mode. Note that it’s necessary to configure the Coordinator first
5. Get MAC short address for both COORD and DEVICE
6. Configure UDP unicast connection for both COORD and DEVICE
7. Start communication from COORD to DEVICE
8. Start communication from DEVICE to COORD

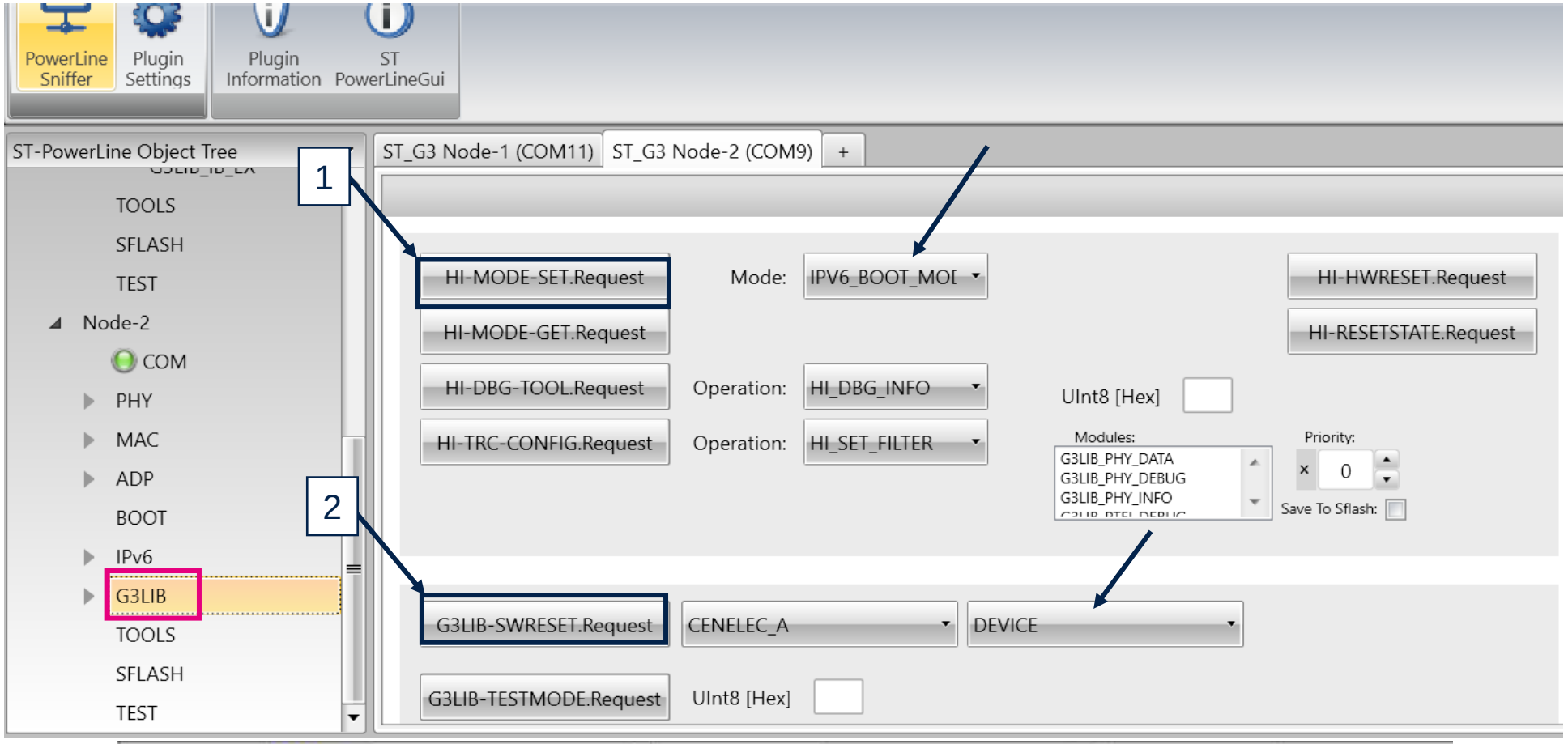
IPv6 boot mode configuration: Coordinator



13:05:13.431	COM11	<-- G3BOOT-SRV-START.Confirm	SUCCESS	Status: G3_SUCCESS
13:04:53.374	COM11	<-- G3LIB-SWRESET.Confirm	SUCCESS	Status: G3_SUCCESS
13:04:51.958	COM11	--> G3LIB-SWRESET.Request		ProtocolVersion: CENELEC A, DeviceType: COORD
13:04:40.381	COM11	<-- HOSTIF-MODESET.Confirm	SUCCESS	
13:04:40.349	COM11	--> HOSTIF-MODESET.Request		IPV6_BOOT_MODE

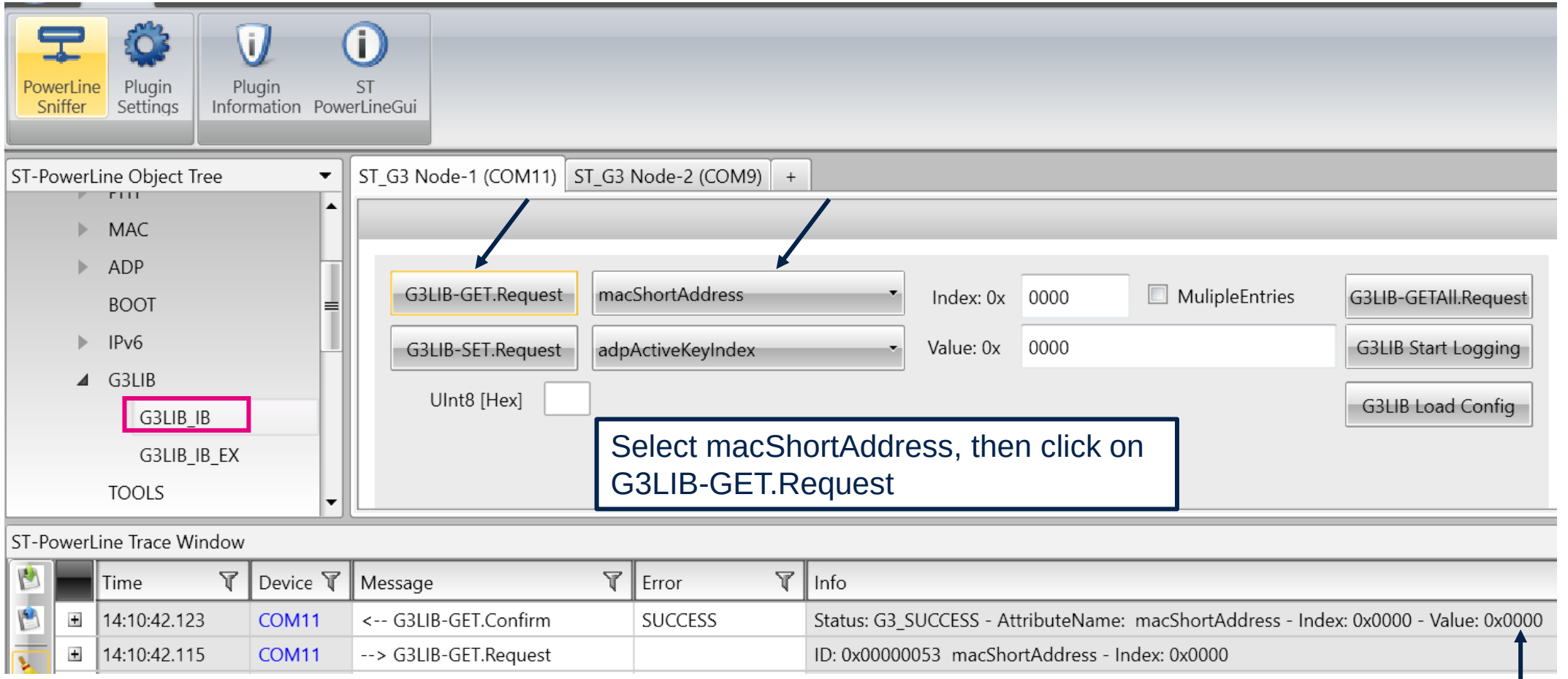
life.augmented

IPv6 boot mode configuration: Device



13:07:44.847	COM9	<-- G3BOOT-DEV-START.Confirm	SUCCESS	Status: G3_SUCCESS - NetworkAddress: 0x0002 - PANId: 0x781D
13:07:44.743	COM11	<-- G3BOOT-SRV-JOIN.Indicatio	SUCCESS	ExtendedAddress: 0x0080E1FFFE4BA618 - ShortAddress: 0x0002
13:07:43.391	COM11	<-- G3BOOT-SRV-GETPSK.Indica	SUCCESS	ExtendedAddress: 0x0080E1FFFE4BA618 - IdP: 0x0080E1FFFE4BA618
13:07:39.977	COM9	<-- G3BOOT-DEV-PANSORT.Indi	SUCCESS	PANCount: 1
13:07:19.919	COM9	<-- G3LIB-SWRESET.Confirm	SUCCESS	Status: G3_SUCCESS
13:07:19.891	COM9	--> G3LIB-SWRESET.Request		ProtocolVersion: CENELEC A, DeviceType: DEVICE
13:07:14.690	COM9	<-- HOSTIF-MODESET.Confirm	SUCCESS	
13:07:14.676	COM9	--> HOSTIF-MODESET.Request		IPV6_BOOT_MODE

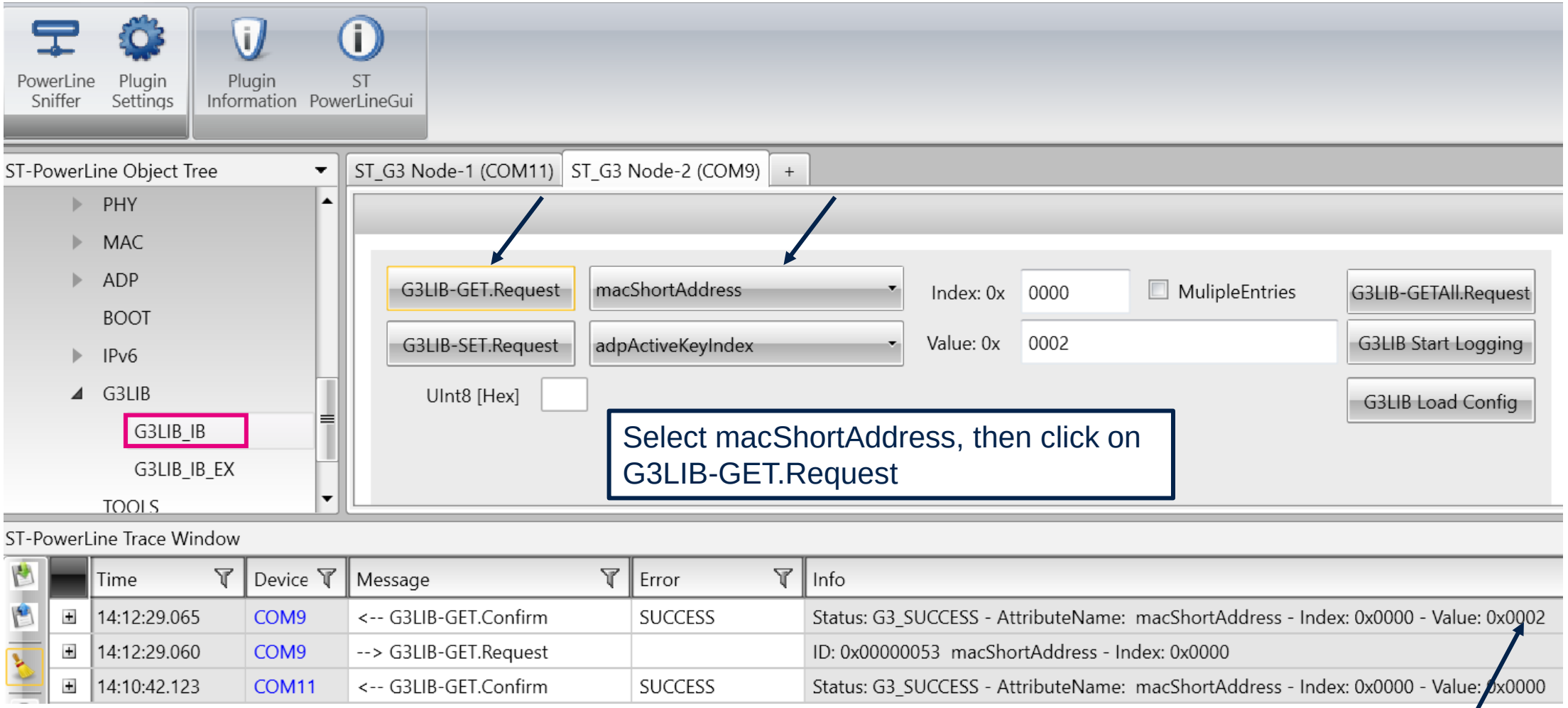
MAC short address: Coordinator



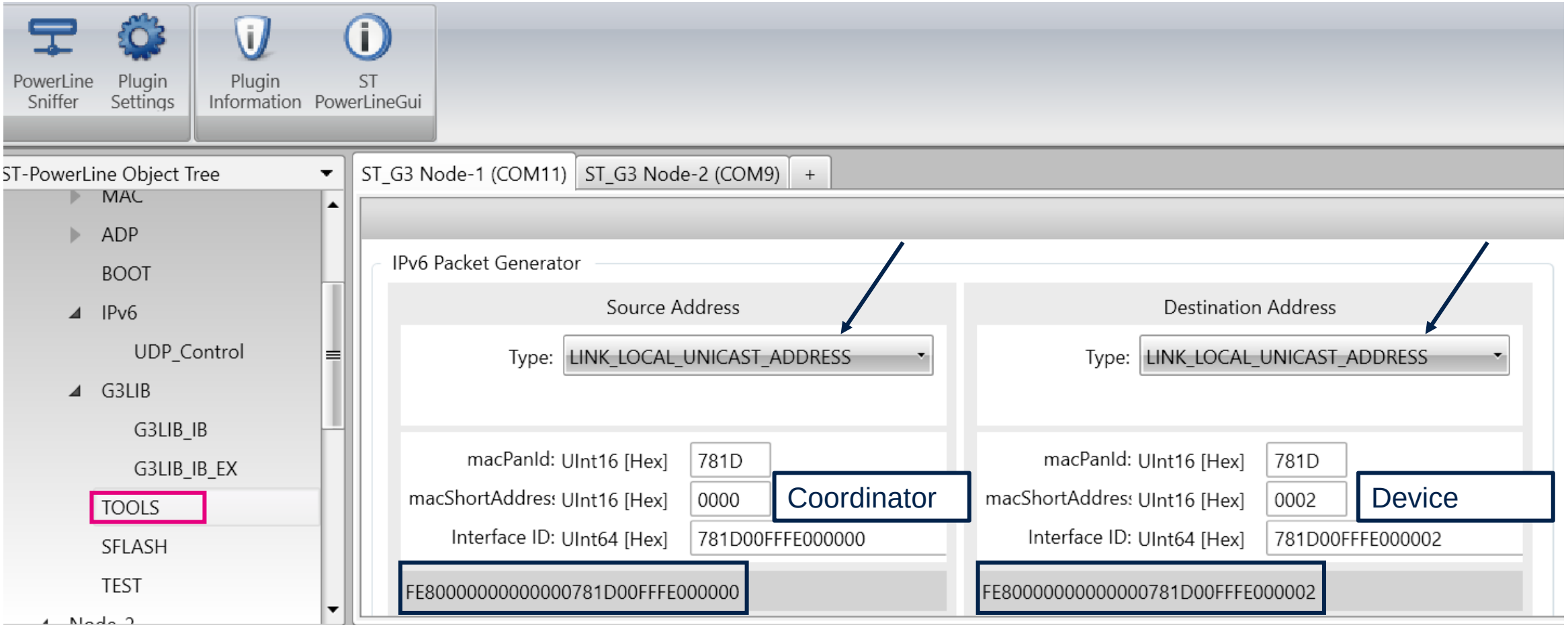
Coordinator MAC short address

life.augmented

MAC short address: Device



Unicast connection settings: Coordinator

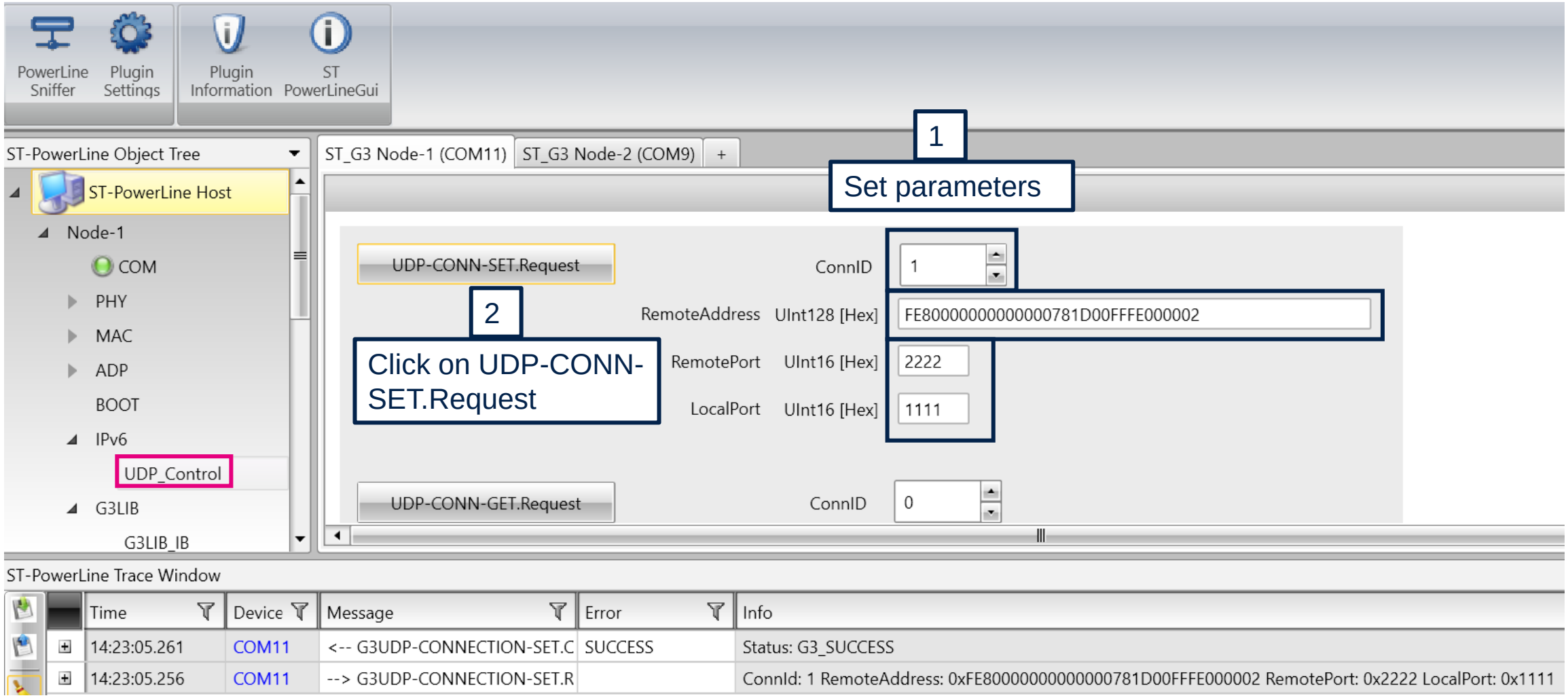


Remote Address for Device, to be copied into the related UDP_Control menu (Node-2)

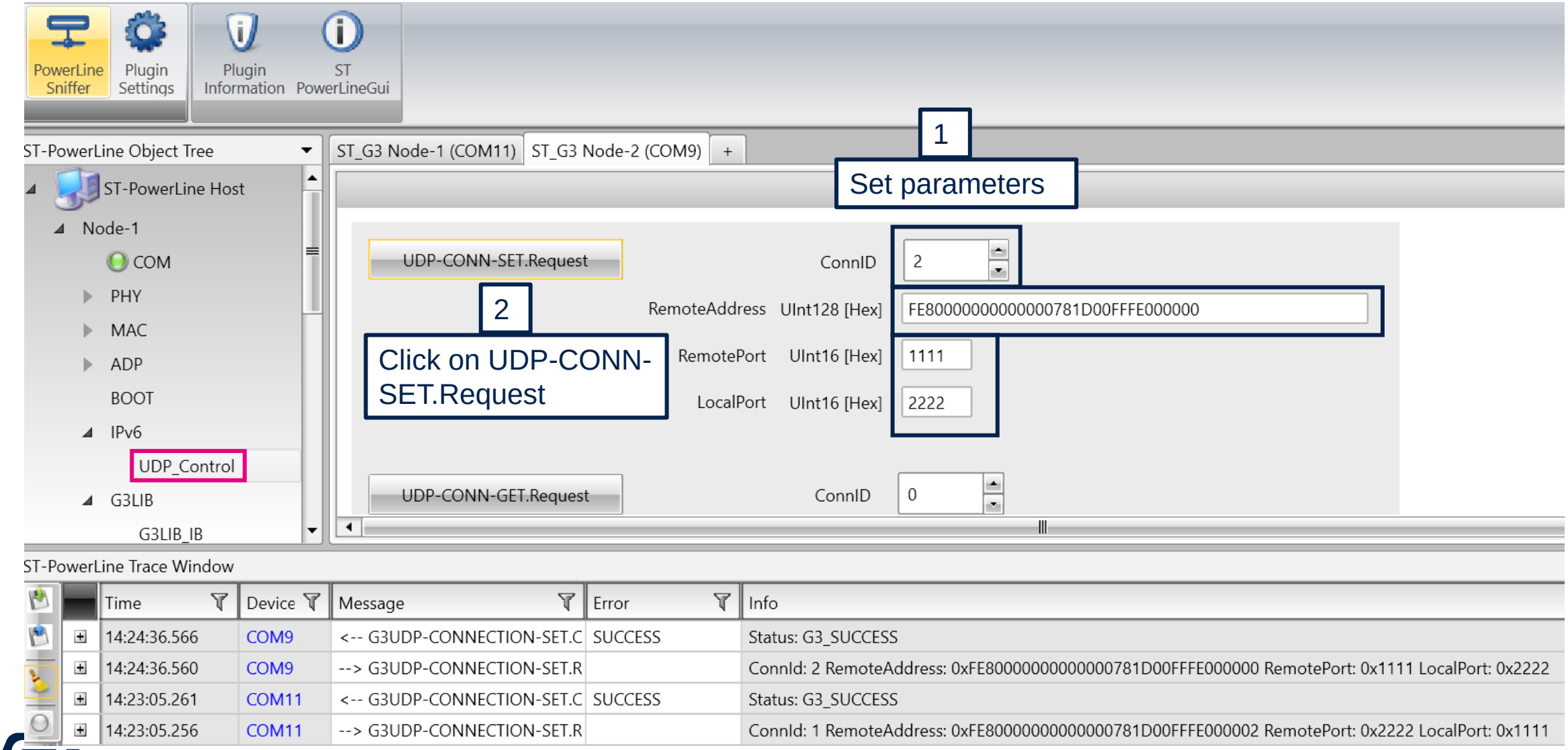
Remote Address for Coordinator, to be copied into the related UDP_Control menu (Node-1)

life.augmented

UDP settings: Coordinator

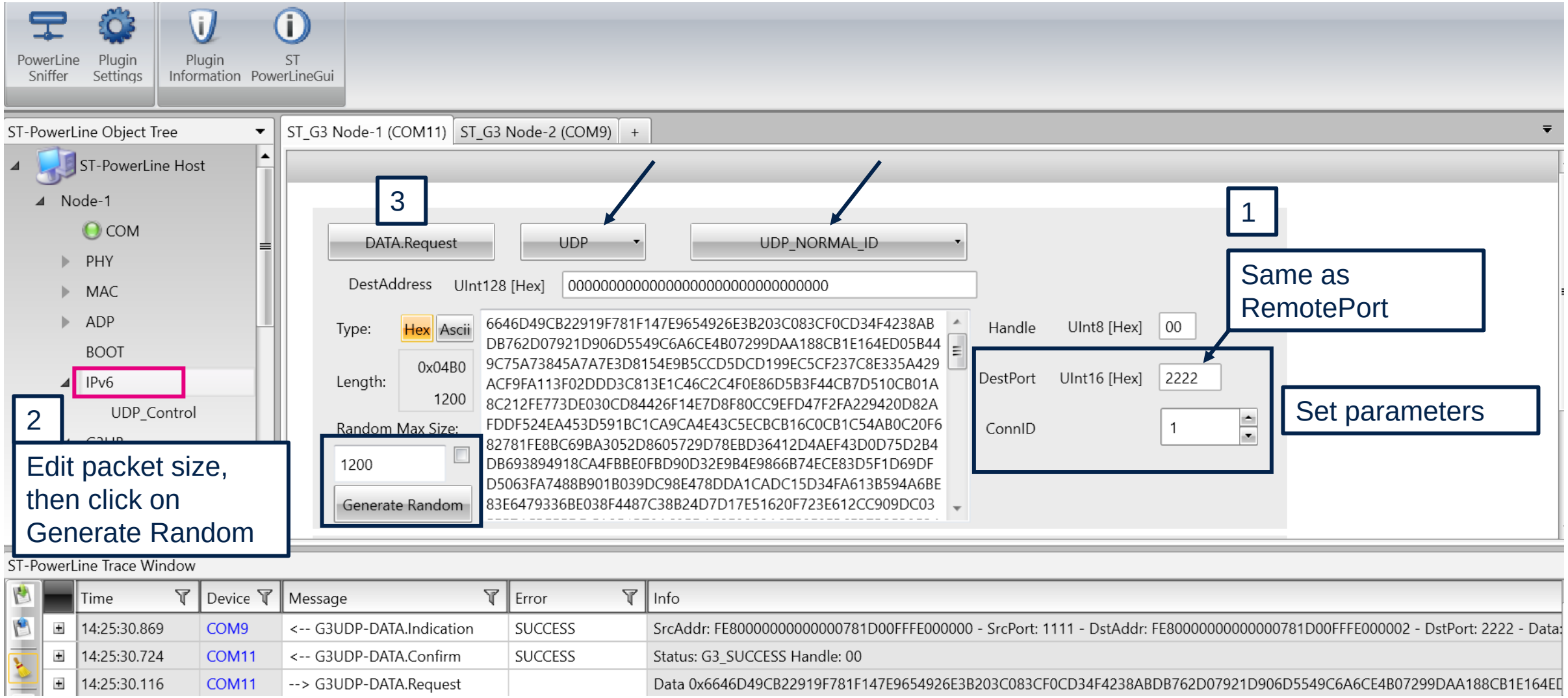


UDP settings: Device



life.augmented

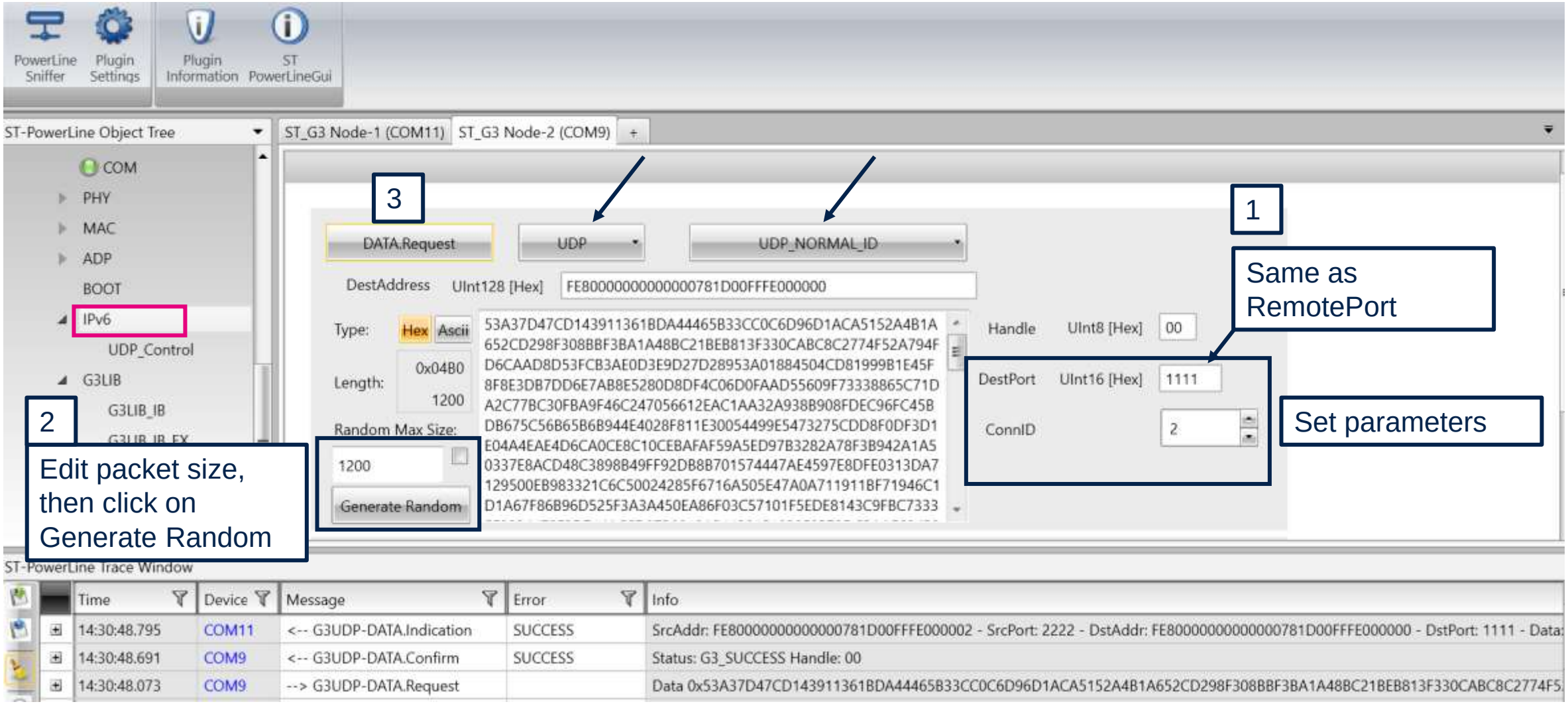
Coordinator vs Device



G3UDP Data Confirm to Coordinator (COM11) and G3 UDP Data Indication on Device (COM9)

life.augmented

Device vs Coordinator



G3UDP Data Confirm to Device (COM9) and G3 UDP Data Indication on Coordinator (COM11)

life.augmented

Thank you

life.augmented