Angle Sensors

GMR-Based Angular Sensors

TLE5012B Register Setting

TLE5012B

Application Note

V1.1, 2011-07-01

ATV SC

Edition 2011-07-01

Published by
Infineon Technologies AG
81726 Munich, Germany

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
V1.1, 2011-07-01	

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1 Introduction

This document is the second part of the electrical specification. Generally the latest data sheet of TLE5012B is valid.

The main interface of the TLE5012B is SSC and the following section describes their configuration bits.

2 SSC- Register Description

In the following section different bit types are used. The meaning of the abbreviation can be found in **Table 1**.

Table 1 Bit Types

Abbreviation	Function	Description
R	Read	Read-only registers
W	Write	Read and write registers
U	Update	Update buffer for this bit is present. If an update is issued and the Update-Register Access bit (UPD in Command Word) is set, the immediate values are stored in this update buffer simultaneously. This enables a snapshot of all necessary system parameters at the same time.

2.1 Registers Chapter

This section defines the registers of the TLE5012B. It also defines the read/write access rights of the specific registers. **Table 2** identifies the values with symbols. Access to the registers is accomplished via the SSC Interface.

Table 2 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Registers Chapter, TLE5012B Registers Description			
STAT	Status Register	00_H	**8**
ACSTAT	Activation Status Register	01_H	**10**
AVAL	Angle Value Register	02_H	**12**
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Table 2 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
ADC_X	X-raw value	10_H	24
ADC_Y	Y-raw value	11_H	24
IIF_CNT	IIF Counter value	20_H	25

The register is addressed wordwise.

2.1.1 TLE5012B Registers Description

Status Register

STAT	Offset	Reset Value
Status Register	**00_H**	**8001_H**

15	14	13	12	11	10	9	8
RD_ST	**S_NR**		**NO_GMR_A**	**NO_GMR_XY**	**S_ROM**	**S_ADCT**	Res
r	w		ru	ru	r	ru	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
S_MAGOL	**S_XYOL**	**S_OV**	**S_DSPU**	**S_FUSE**	**S_VR**	**S_WD**	**S_RST**
ru	ru	ru	ru	ru	ru	ru	ru

Field	Bits	Type	Description
RD_ST	15	r	**Read Status** 0_B status values not changed since last readout 1_B status values changed Reset: 1_B
S_NR	14:13	w	**Slave Number** It is used to identify up to four sensors in a bus configuration. The levels on pin SCK and pin IFC can be used to change the default slave number for SPC interface. Pin SCK represents S_NR[13] and pin IFC the S_NR[14]. Reset: 00_B

Field	Bits	Type	Description
NO_GMR_A	12	ru	**No valid GMR Angle Value** Cyclic check of DSPU output. 0_B valid GMR angle value on the interface 1_B no valid GMR angle value on the interface (e.g test vectors) Reset: 0_B
NO_GMR_XY	11	ru	**No valid GMR XY Values** Cyclic check of ADC input. 0_B valid GMR_XY values on the ADC input 1_B no valid GMR_XY values on the ADC input (e.g. test vectors) Reset: 0_B
S_ROM	10	r	**Status ROM**[1)] Check of ROM-CRC at startup. After fail DSPU does not start. SPI access possible. 0_B CRC ok 1_B CRC fail or running Reset: 0_B
S_ADCT	9	ru	**Status ADC-Test**[1)] Check of signal path with test vectors. All test vectors at startup tested. Activation in operation via AS_ADCT possible. 0_B Test vectors ok 1_B Test vectors out of limit Reset: 0_B
S_MAGOL	7	ru	**Status Magnitude Out of Limit**[1)] Cyclic check of available magnetic field strength. Deactivation via AS_VEC_MAG. 0_B GMR-magnitude ok 1_B GMR-magnitude out of limit Reset: 0_B
S_XYOL	6	ru	**Status X,Y Data Out of Limit**[1)] Cyclic check of X and Y raw values. Deactivation via AS_VEC_XY 0_B X,Y data ok 1_B X,Y data out of limit (>23230 digits) Reset: 0_B
S_OV	5	ru	**Status Overflow**[1)] Cyclic check of DSPU overflow. Deactivation via AS_OV. 0_B No DSPU overflow occurred 1_B DSPU overflow occurred Reset: 0_B
S_DSPU	4	ru	**Status Digital Signal Processing Unit** Check of DSPU, CORDIC and CAPCOM at startup. Activation in operation via AS_DSPU possible. 0_B DSPU self test ok 1_B DSPU self test not ok, or self test is running Reset: 0_B

Field	Bits	Type	Description
S_FUSE	3	ru	**Status Fuse CRC**[1)] Cyclic CRC check of laser cut fuses. Deactivation via AS_FUSE and disabled by activated auto calibration. *Note: Changing of fused parameters results in new CRC, which is unlike to stored CRC --> Fuse CRC fail* 0_B Fuse CRC ok 1_B Fuse CRC fail Reset: 0_B
S_VR	2	ru	**Status Voltage Regulator**[1)] Permanent check of internal and external supply voltages. Deactivation via AS_VR 0_B Voltages ok 1_B V_{DD} over voltage; V_{DD} intervillage; V_{DD}-off; GND-off; or V_{OVG}; V_{OVA}; V_{OVD} too high Reset: 0_B
S_WD	1	ru	**Status Watchdog** Permanent check of watchdog. After watchdog-counter overflow, the DSPU stops. Deactivation via AS_WD 0_B after chip reset 1_B watchdog counter expired (DSPU stop), AS_RST must be activated. Outputs deactivated, Pull Up/Down active. Reset: 0_B
S_RST	0	ru	**Status Reset** Permanent check of any reset. Deactivation via AS_RST. 0_B no reset since last readout 1_B indication of power-up, short power-break, firmware or active reset Reset: 1_B

1) reset to “0” after readout

Activation Status Register

ACSTAT	**Offset**	**Reset Value**
Activation Status Register	**01_H**	**$5AFE_H$**

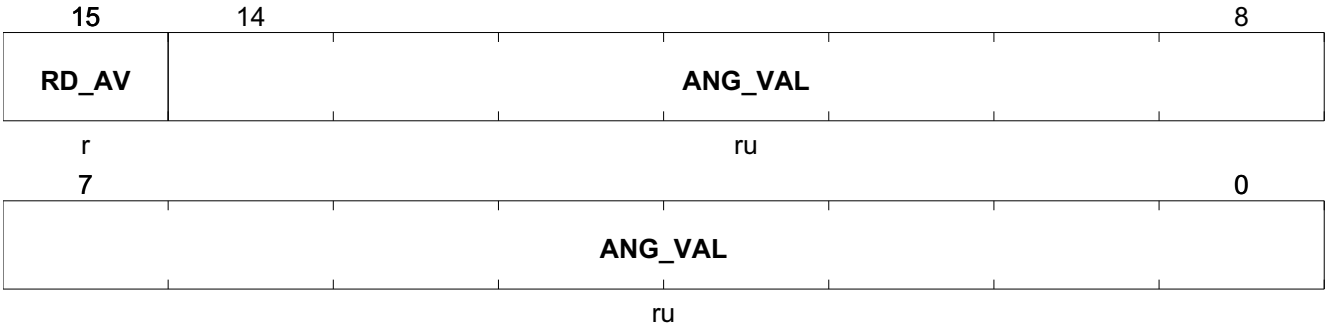
15					11	10	9	8
Res						**AS_FRST**	**AS_ADCT**	Res
						w	w	

7	6	5	4	3	2	1	0
AS_VEC_MAG	**AS_VEC_XY**	**AS_OV**	**AS_DSPU**	**AS_FUSE**	**AS_VR**	**AS_WD**	**AS_RST**
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
Res	15:11	w	**Reserved** Reset: 01011_B
AS_FRST	10	w	**Activation of Firmware Reset** All configuration registers remain their contents. 0_B after execution 1_B activation of firmware reset (S_RST is set) Reset: 0_B
AS_ADCT	9	w	**Enable ADC Test vector Check** 0_B after execution 1_B activation of ADC Test vector Check Reset: 1_B
AS_VEC_MAG	7	w	**Activation of Magnitude Check** 0_B monitoring of magnitude disabled 1_B monitoring of magnitude enabled Reset: 1_B
AS_VEC_XY	6	w	**Activation of X,Yout of limit -Check** 0_B monitoring of X,Y out of limit disabled 1_B monitoring of X,Y out of limit enabled Reset: 1_B
AS_OV	5	w	**Enable of DSPU Overflow Check** 0_B monitoring of DSPU Overflow disabled 1_B monitoring of DSPU Overflow enabled Reset: 1_B
AS_DSPU	4	w	**Activation DSPU BIST** 0_B after execution 1_B activation of DSPU BIST or BIST running Reset: 1_B
AS_FUSE	3	w	**Activation Fuse CRC** 0_B monitoring of Fuse CRC disabled 1_B monitoring of Fuse CRC enabled Reset: 1_B
AS_VR	2	w	**Enable Voltage Regulator Check** 0_B check of regulator voltages disabled 1_B check of regulator voltages enabled Reset: 1_B
AS_WD	1	w	**Enable DSPU Watchdog-HW-Reset** 0_B DSPU Watchdog monitoring disabled 1_B DSPU Watchdog monitoring enabled Reset: 1_B
AS_RST	0	w	**Activation of Hardware Reset** Activation occurs after CSQ switches from ’0’ to ’1’ after SSC transfer. 0_B after execution 1_B activation of HW Reset (S_RST is set) Reset: 0_B

Angle Value Register

AVAL	Offset	Reset Value
Angle Value Register	**02_H**	**8000_H**



Field	Bits	Type	Description
RD_AV	15	r	**Read Status, Angle Value** 0_B no new angle value since last readout 1_B new angle value (ANG_VAL) present Reset: 1_B
ANG_VAL	14:0	ru	**Calculated Angle Value (signed 15bit)** (ANG_RANGE = 0x080) $Angle[°] = \frac{360°}{2^{15}} ANG\_VAL[digits]$ (1) 4000_H -180° 0000_H 0° $3FFF_H$ +179.99° Reset: 0_H

Angle Speed Register

ASPD	Offset	Reset Value
Angle Speed Register	03_H	8000_H

15	14	8
RD_AS	ANG_SPD	
r	ru	

7	0
ANG_SPD	
ru	

Field	Bits	Type	Description
RD_AS	15	r	**Read Status, Angle Speed** 0_B no new angle speed value since last readout 1_B new angle speed value (ANG_SPD) present Reset: 1_B
ANG_SPD	14:0	ru	**Calculated Angle Speed** Without prediction difference between three consecutive angle values. With prediction, difference between predicted value and next-to-last measured angle value. $Speed\ [°/s] = \frac{\frac{AngleRange\ [°]}{2^{15}} ANG\_SPD\ [digits]}{2t_{upd}\ [s]}$ (2) Reset: 0_H

Angle Revolution Register

AREV	Offset	Reset Value
Angle Revolution Register	04_H	8000_H

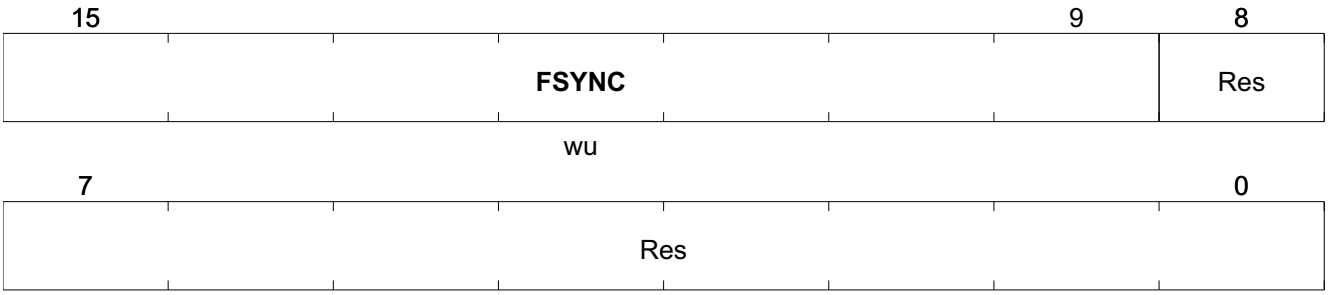
15	14	9	8
RD_REV	FCNT		REVOL
r	wu		ru

7	0
REVOL	
ru	

Field	Bits	Type	Description
RD_REV	15	r	**Read Status, Revolution** 0_B no new values since last readout 1_B new value (REVOL) present Reset: 1_B
FCNT	14:9	wu	**Frame Counter (unsigned 6 bit value)** Increments every new angle value Reset: 0_H
REVOL	8:0	ru	**Number of Revolutions (signed 9 bit value)** If prediction is enabled, revolution counter is one schedule delayed related to ANG_VAL. Reset: 0_H

Frame Synchronization Register

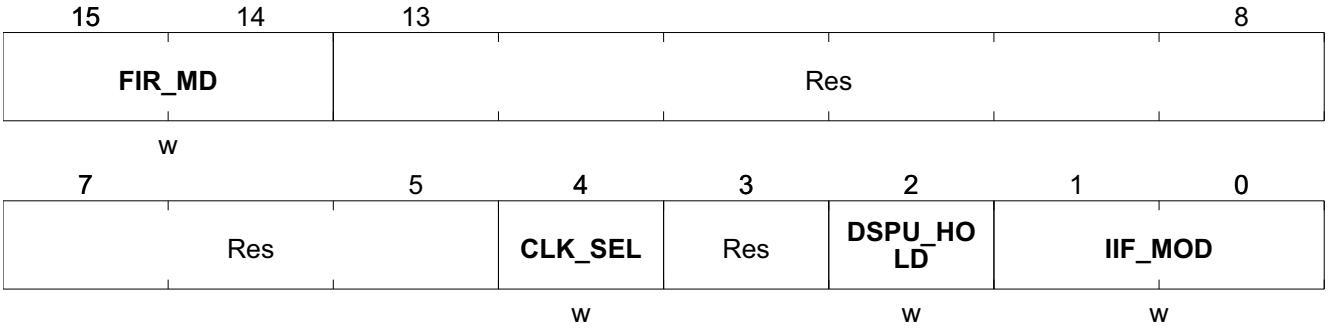
FSYNC	Offset	Reset Value
Frame Synchronization Register	**05_H**	**0000_H**



Field	Bits	Type	Description
FSYNC	15:9	wu	**Frame Synchronization Counter Value** Sub counter within one frame. Reset: 0_H

Interface Mode1 Register

MOD_1	Offset	Reset Value
Interface Mode1 Register	06_H	4001_H



Field	Bits	Type	Description
FIR_MD	15:14	w	**Filter Decimation Setting (Update Rate Setting)** 00_B 21.3µs (only for raw X/Y-values) 01_B 42.7µs 10_B 85.3µs 11_B 170.6µs Reset: 01_B
CLK_SEL	4	w	**Clock Source Select** in absence of external clock or PLL out of lock automatically switch to internal oscillator. 0_B internal oscillator 1_B external 4MHz clock (IFC pin switched to input) Reset: 0_B
DSPU_HOLD	2	w	**Hold DSPU Operation** If DSPU is on hold no WD-reset is performed by DSPU. Deactivate watchdog with AS_WD before setting DSPU on hold. 0_B DSPU in normal schedule operation 1_B DSPU is on hold Reset: 0_B
IIF_MOD	1:0	w	**Incremental Interface Mode** 00_B IIF disabled 01_B A/B operation with Index on CLK/HS3 10_B Step/Direction operation with Index on CLK/HS3 11_B not allowed Reset: 01_B

SIL Register

SIL	Offset	Reset Value
SIL Register	07_H	0000_H

15	14	13	11	10	9	8
FILT_PAR	**FILT_INV**	Res		**FUSE_REL**	Res	
w	w			w		

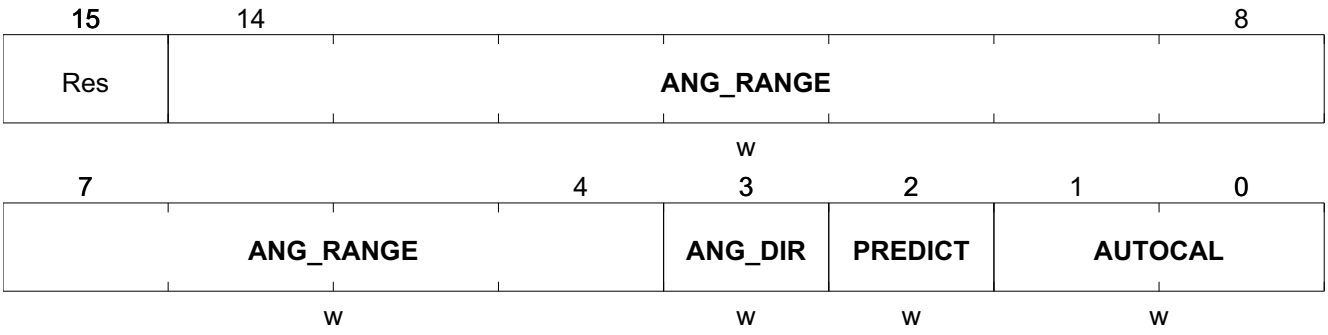
7	6	5	3	2	0
Res	**ADCTV_EN**	**ADCTV_Y**		**ADCTV_X**	
	w	w		w	

Field	Bits	Type	Description
FILT_PAR	15	w	**Filter Parallel** 0_B filter parallel disabled 1_B filter parallel enabled (source: X-value) Reset: 0_B
FILT_INV	14	w	**Filter Inverted** 0_B filter inverted disabled 1_B filter inverted enabled Reset: 0_B
FUSE_REL	10	w	**Fuse Reload** 0_B fuse reload disabled 1_B fuse parameters reloaded to DSPU at next cycle start Reset: 0_B
ADCTV_EN	6	w	**ADC-Test vectors** 0_B ADC-Test vectors disabled 1_B ADC-Test vectors enabled Reset: 0_B
ADCTV_Y	5:3	w	**Test vector Y** 000_B 0V 001_B +70% 010_B +100% 011_B +Overflow 101_B -70% 110_B -100% 111_B -Overflow Reset: 0_H

Field	Bits	Type	Description
ADCTV_X	2:0	w	**Test vector X** 000_B 0V 001_B +70% 010_B +100% 011_B +OV 101_B -70% 110_B -100% 111_B -OV Reset: 0_H

Interface Mode2 Register

MOD_2	Offset	Reset Value
Interface Mode2 Register	**08_H**	**0801_H**

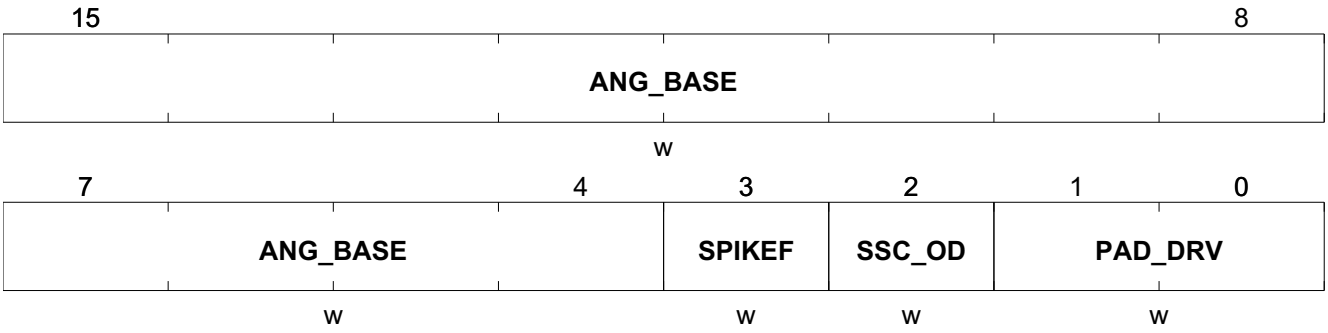


Field	Bits	Type	Description
ANG_RANGE	14:4	w	**Angle Range** Angle Range [°] = 360° * (2^7 / ANG_RANGE[digits]) 200_H represents 90° 080_H represents 360° Reset: 080_H
ANG_DIR	3	w	**Angle Direction** 0_B counterclockwise rotation of magnet 1_B clockwise rotation of magnet Reset: 0_B
PREDICT	2	w	**Prediction** 0_B prediction disabled 1_B prediction enabled Reset: 0_B

Field	Bits	Type	Description
AUTOCAL	1:0	w	**Auto calibration Mode** Explanation to auto calibration modes are described in data sheet of TLE5012B. 00_B no auto calibration 01_B auto calibration mode 1 10_B auto calibration mode 2 11_B auto calibration mode 3 Reset: 01_B

Interface Mode3 Register

MOD_3	Offset	Reset Value
Interface Mode3 Register	**09_H**	**0000_H**

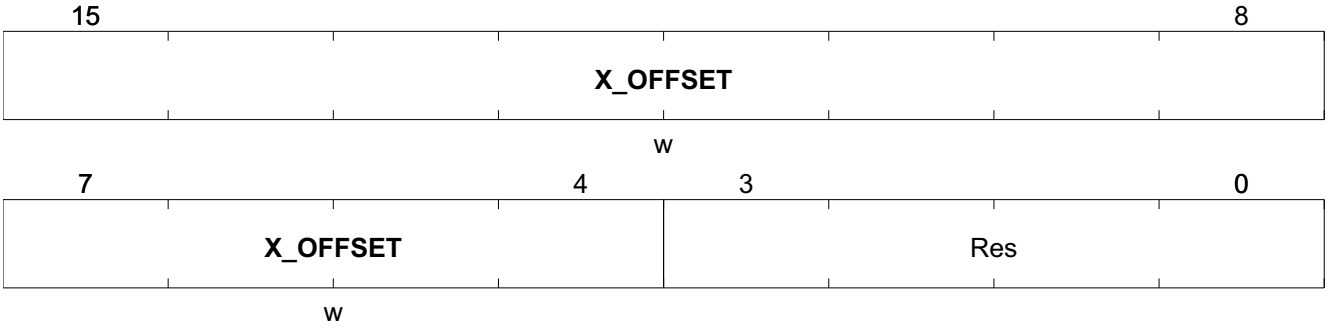


Field	Bits	Type	Description
ANG_BASE	15:4	w	**Angle Base** 800_H -180° 000_H 0° 001_H 0.0879° $7FF_H$ +179.912° Reset: 000_H
SPIKEF	3	w	**Analog Spike Filters of Input Pads** 0_B spike filter disabled 1_B spike filter enabled Reset: 0_B
SSC_OD	2	w	**SSC-Interface** 0_B Push-Pull 1_B Open Drain Reset: 0_B

Field	Bits	Type	Description
PAD_DRV	1:0	w	**Configuration of Pad-Driver** 00_B IFA/IFB/IFC: strong driver, DATA: strong driver, fast edge 01_B IFA/IFB/IFC: strong driver, DATA: strong driver, slow edge 10_B IFA/IFB/IFC: weak driver, DATA: medium driver, fast edge 11_B IFA/IFB/IFC: weak driver, DATA: weak driver, slow edge Reset: 00_B

Offset X Register

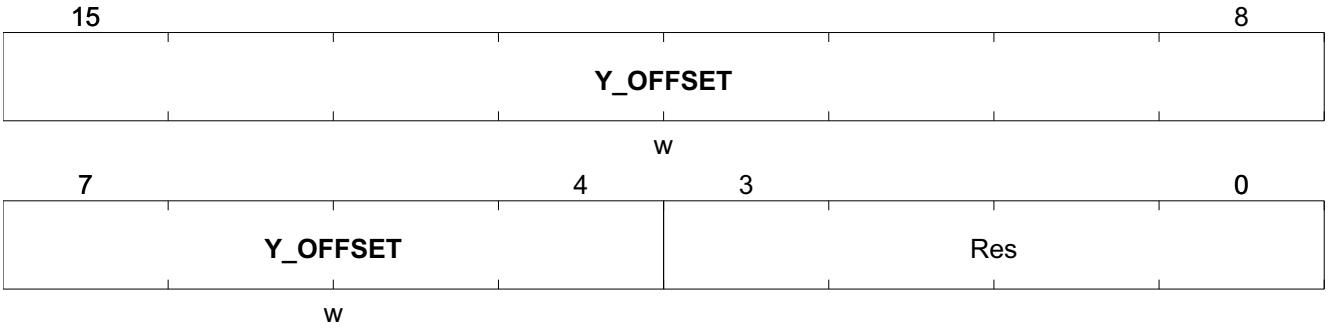
OFFX	Offset	Reset Value
Offset X	**$0A_H$**	**0000_H**



Field	Bits	Type	Description
X_OFFSET	15:4	w	**Offset Correction of X-value in digits** Reset: 0_H

Offset Y Register

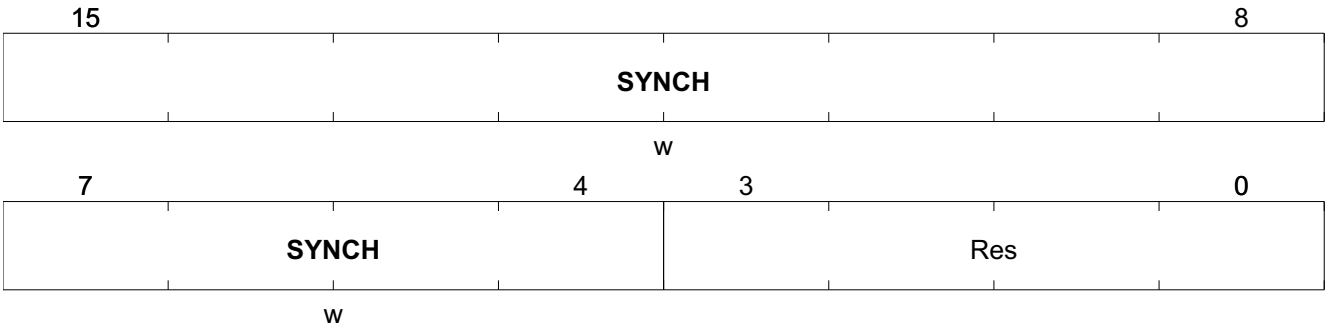
OFFY	Offset	Reset Value
Offset Y	$0B_H$	0000_H



Field	Bits	Type	Description
Y_OFFSET	15:4	w	**Offset Correction of Y-value in digits** Reset: 0_H

Synchronicity Register

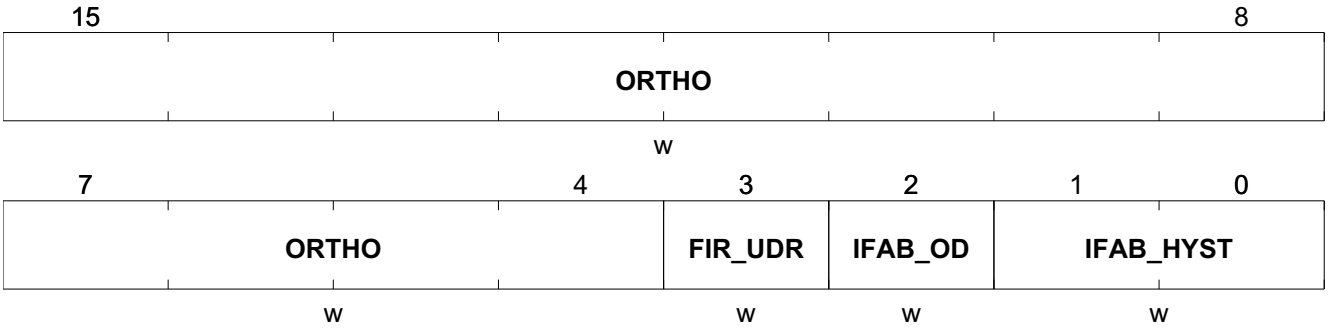
SYNCH	Offset	Reset Value
Synchronicity	$0C_H$	0000_H



Field	Bits	Type	Description
SYNCH	15:4	w	**Amplitude Synchronicity** $+2047_D$ 112.494% 0_D 100% -2048_D 87.500% Reset: 0_H

IFAB Register

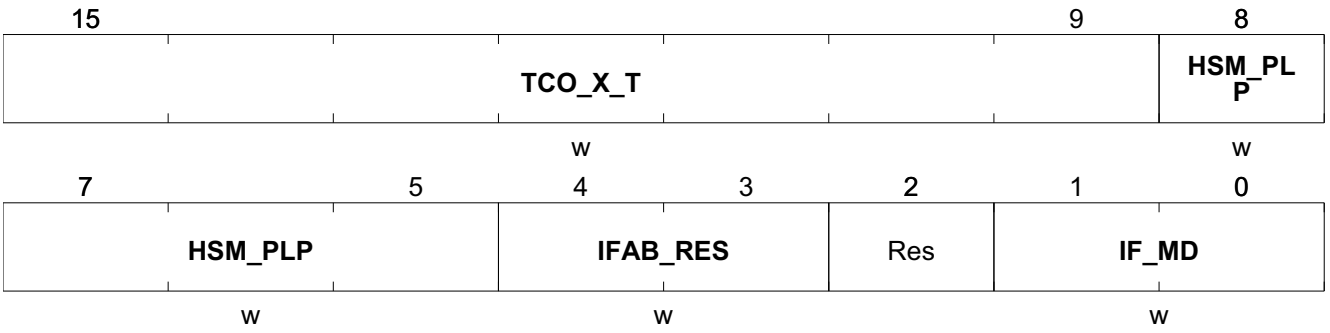
IFAB	Offset	Reset Value
IFAB Register	$0D_H$	$000B_H$



Field	Bits	Type	Description
ORTHO	15:4	w	**Orthogonality Correction of X and Y Components** $+2047_D$ 11.2445° 0_D 0° -2048_D -11.2500° Reset: 0_H
FIR_UDR	3	w	**FIR Update Rate** Initial FIR setting. Changes of FIR setting can be done after power-on via SPI within FIR_MD. 0_B FIR_MD = '10' (85.3µs) 1_B FIR_MD = '01' (42.7µs) Reset: 1_B
IFAB_OD	2	w	**IFA & IFB Open Drain** 0_B Push-Pull 1_B Open Drain Reset: 0_B
IFAB_HYST	1:0	w	**HSM & IIF Hysteresis** 00_B 0° 01_B 0.09° 10_B 0.27° 11_B 0.625° Reset: 11_B

Interface Mode4 Register

MOD_4	Offset	Reset Value
Interface Mode4 Register	$0E_H$	0080_H

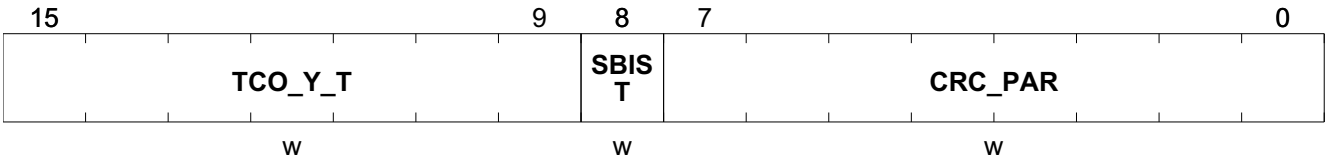


Field	Bits	Type	Description
TCO_X_T	15:9	w	**Offset Temperature Coefficient for X-Component** Reset: 0_H
HSM_PLP	8:5	w	**Hall Switch Mode; Pole-Pair Configuration** 0000_B 1 pole pairs 0001_B 2 pole pairs 0010_B 3 pole pairs 0011_B 4 pole pairs 0100_B 5 pole pairs 0101_B 6 pole pairs 0110_B 7 pole pairs 0111_B 8 pole pairs 1000_B 9 pole pairs 1001_B 10 pole pairs 1010_B 11 pole pairs 1011_B 12 pole pairs 1100_B 13 pole pairs 1101_B 14 pole pairs 1110_B 15 pole pairs 1111_B 16 pole pairs Reset: 0100_B
IFAB_RES	4:3	w	**IFAB Resolution** 00_B 12bit = 0.088° (244Hz) 01_B 11bit = 0.176° (488Hz) 10_B 10bit = 0.352° (977Hz) 11_B 9bit = 0.703° (1953Hz) Reset: 00_B

Field	Bits	Type	Description
IF_MD	1:0	w	**Interface Mode** Selected by external circuit of CLK pin at Power On Time. CLK pin connected to V_{DD} --> Incremental Interface is selected; CLK pin connected to GND --> IF_MD stored Interface is used. Switching to another interface during operation needs to stop the DSPU (DSPU_HOLD). 00_B SSC mode; IIF 01_B SSC mode; PWM 10_B SSC mode; HSM 11_B SSC mode; SPC Reset: 00_B

Temperature Coefficient Register

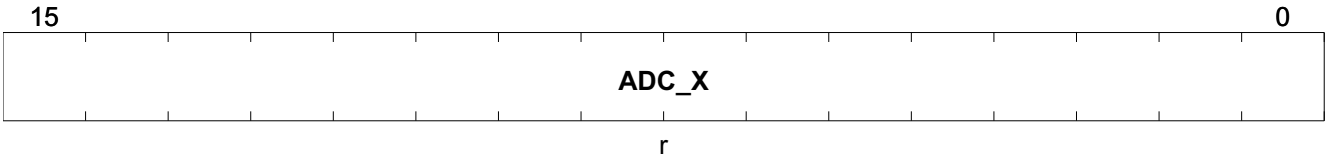
TCO_Y	Offset	Reset Value
Temperature Coefficient Register	**$0F_H$**	**0100_H**



Field	Bits	Type	Description
TCO_Y_T	15:9	w	**Offset Temperature Coefficient for Y-Component** Reset: 0_H
SBIST	8	w	**Startup-BIST** 0_B Startup-BIST disabled 1_B Startup-BIST enabled Reset: 1_B
CRC_PAR	7:0	w	**CRC of Parameters** CRC of parameters from address 08_H to $0F_H$. By changing any settings within these registers also this CRC has to be updated. Reset: 0_H

X-raw Value Register

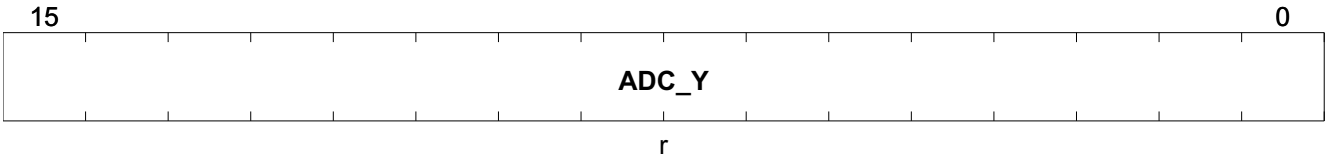
ADC_X	Offset	Reset Value
X-raw value	10_H	0000_H



Field	Bits	Type	Description
ADC_X	15:0	r	**ADC value of X-GMR** Read out of this register will update ADC_Y Reset: 0_H

Y-raw Value Register

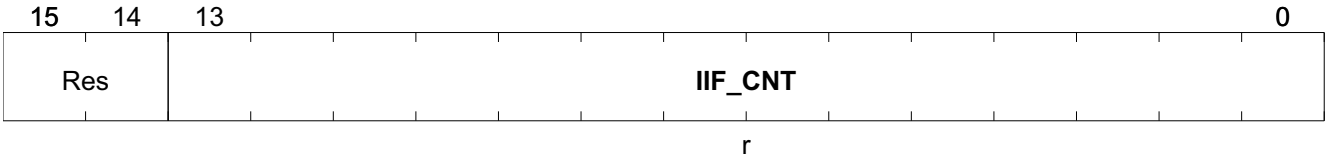
ADC_Y	Offset	Reset Value
Y-raw value	11_H	0000_H



Field	Bits	Type	Description
ADC_Y	15:0	r	**ADC value of Y-GMR** Updated when ADC_X or ADC_Y is read. Reset: 0_H

Increment Counter Register

IIF_CNT	Offset	Reset Value
IIF Counter value	20_H	0000_H



Field	Bits	Type	Description
IIF_CNT	13:0	r	**Counter value of increments** This value can be used for synchronization purposes between sensor and counter value on micro controller side. Reset: 0_H

2.2 Communication Examples

This chapter gives some short SPI communication examples. The sensor has to be selected first via CSQ and also SCK must be available for the communication.

Table 3 SSC Command to read the angle value

SSC Word No.	Description	Master transmitting	TLE5012 transmitting	Note
1	Command	1_0000_0_000010_0001		R/W_Lock_UPD_ADD_ND
2	Read Data		1_xxxxxxxxxxxxxxx	Read angle value
3	Safety Word		1_1_1_1_xxxx_xxxxxxxx	Read safety word

Table 4 SSC Command to read angle speed and angle revolution

SSC Word No.	Description	Master transmitting	TLE5012 transmitting	Note
1	Command	1_0000_0_000011_0010		R/W_Lock_UPD_ADD_ND
2	Read Data		1_xxxxxxxxxxxxxxx	Read angle speed
3	Read Data		1_xxxxxx_xxxxxxxxx	Read angle revolution
4	Safety Word		1_1_1_1_xxxx_xxxxxxxx	Read safety word

Table 5 SSC Command to change Interface Mode2 register

SSC Word No.	Description	Master transmitting	TLE5012 transmitting	Note
1	Command	0_1010_0_001000_0001		R/W_Lock_UPD_ADD_ND
2	Write Data	0_00010000000_1_0_01		ANG_Range: 080_H; ANG_DIR: 1_B; PREDICT: 0_B; AUTOCAL: 01_B
3	Safety Word		1_1_1_1_xxxx_xxxxxxxx	Read safety word

3 SSC- Register Description for SPC Interface

The Short PWM Code (SPC) is a synchronized data transmission based on the SENT protocol (Single Edge Nibble Tranmission). More details to that can be found in the latest data sheet of TLE5012B. SPC uses some registers in a different way. Not mentioned registers and bits remain the same as described in **Section 2**.

3.1 Registers Chapter for SPC Interface

This section defines the registers of the TLE5012B. It also defines the read/write access rights of the specific registers. **Table 6** identifies the values with symbols. Access to the registers is accomplished in parallel to the SPC Interface via the SSC Interface.

Table 6 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Registers Chapter for SPC Interface, TLE5012B SPC Registers Description			
IFAB	IFAB Register	$0D_H$	**27**
MOD_4	Interface Mode4 Register	$0E_H$	**28**

The register is addressed wordwise.

3.1.1 TLE5012B SPC Registers Description

IFAB Register

IFAB	Offset	Reset Value
IFAB Register	**$0D_H$**	**0000_H**

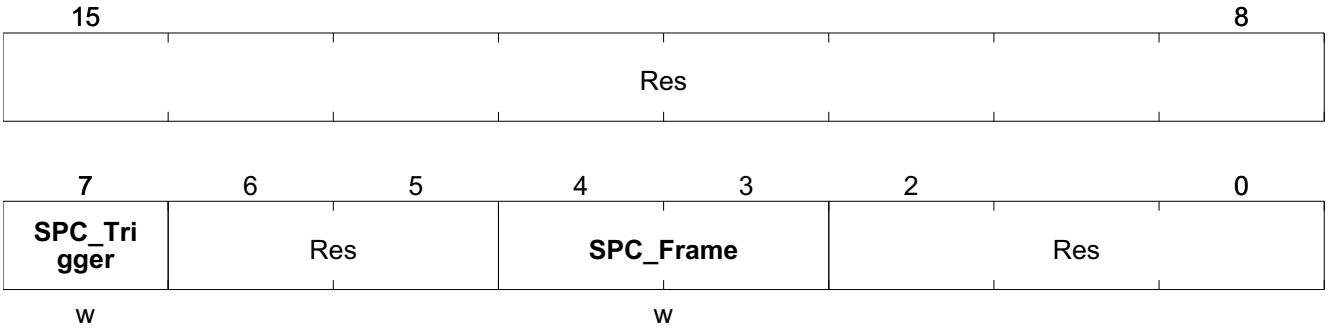
15	14	13	12	11	10	9	8
Res							

7	6	5	4	3	2	1	0
Res						**Predivider**	
						w	

Field	Bits	Type	Description
Predivider	1:0	w	**SPC Predivider** The length of one unit time (UT) can be changed. 00_B 3µs 01_B 2.5µs 10_B 2.0µs 11_B 1.5µs Reset: 00_B

Interface Mode4 Register

MOD_4	Offset	Reset Value
Interface Mode4 Register	**$0E_H$**	**0000_H**



Field	Bits	Type	Description
SPC_Trigger	7	w	**SPC Total Trigger Time** The maximum length of the master pulse can be reduced. 0_B 90UT 1_B t_{mlow} + 12UT Reset: 0_B
SPC_Frame	4:3	w	**SPC Frame Configuration** 00_B 12bit angle 01_B 16bit angle 10_B 12bit angle; 8bit temperature 11_B 16bit angle; 8bit temperature Reset: 00_B

4 Fuse Values

The difference between the product types can be seen in **Figure 1**

	Interface Mode2 Register																			
	ang_range											ang_dir	predict	autocal		spikef	ssc_od	pad_drv		
TLE5012B - E1000 (IIF)	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	
TLE5012B - E3005 (HSM)	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	
TLE5012B - E5000 (PWM)	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	
TLE5012B - E9000 (SPC)	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	
	msb									*lsb*				*msb*	*lsb*			*msb*	*lsb*	

	Temp. Coeff. Reg.	IFAB Register				Interface Mode4 Register							
	sbist	fir_udr	ifab_od	ifab_hyst		hsm_plp				ifab_res		if_mod	
TLE5012B - E1000 (IIF)	1	1	0	1	1	0	1	0	0	0	0	0	0
TLE5012B - E3005 (HSM)	1	1	0	1	1	0	1	0	0	0	0	1	0
TLE5012B - E5000 (PWM)	1	0	0	0	0	0	0	0	0	0	0	0	1
TLE5012B - E9000 (SPC)	1	0	1	0	0	x	0	x	x	0	0	1	1
				msb	*lsb*	*msb*		*lsb*		*msb*	*lsb*	*msb*	*lsb*

Figure 1 Default fuse settings

w w w . i n f i n e o n . c o m

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