Multilayer SiN_x Passivated Al_2O_3 Gate Dielectric Featuring a Robust Interface for Ultralong-Lifetime AlGaN/GaN HEMT

***Abstract*—This paper presents a multilayer SiN_x passivation-based robust and high-reliability interface for effective suppression of current collapse and reduction of leakage current in AlGaN/GaN heterostructure. A plasma-enhanced atomic layer deposited (PEALD) Al_2O_3 gate dielectric is pre-passivated using low-pressure chemical vapor deposition (LPCVD)-grown bilayer (Si-rich and Si-poor) SiN_x and post-passivated using plasma-enhanced chemical vapor deposition (PECVD)-grown thick SiN_x. The high thermal stability and well-ordered crystalline structure of the generated interface that effectively suppress surface-trap-induced current collapse and leakage current are exploited to develop high-performance AlGaN/GaN-Si high electron mobility transistors (HEMTs). High-resolution transmission electron microscopy/energy-dispersive X-ray spectroscopy (TEM/EDX) mapping analyses indicate a very sharp interface with a narrow oxygen contaminated region. In addition, the performance characterization of the fabricated HEMT reveals a high drain saturation current, peak extrinsic transconductance (up to 199.5 mS/mm), and dynamic R_{ON}/static R_{ON} of 1.067 even at a high drain voltage (700 V). Moreover, an excellent mean time-to-failure (MTTF) of 2.204×10^8 h at an activation energy of 2.621 eV (T_C = 150 °C) is obtained, which indicates that the developed HEMT exhibits an ultralong operation lifetime for high-power applications.**

***Index Terms*— Accelerated three-temperature test, AlGaN/GaN HEMT, multilayer SiN_x passivation, TEM/EDX mapping, ultralong-lifetime.**

I. Introduction

SUPERIOR material properties such as high breakdown voltage, high bandgap (~3.4 eV), high electron saturation velocity (~2×10^7 cm s^{-1}), high thermal conductivity, and high two-dimensional electron gas (2DEG) density (~1×10^{13} cm^{-2}) at the interface, have established AlGaN/GaN heterostructure as a frontrunner in the development of high-performance high-electron-mobility transistors (HEMTs) [1-4]. Such devices are expected to meet the ever-growing demands of high power, high efficiency, and high-speed switching applications [5-7]. However, current collapse and leakage current, which are critical device failure mechanisms, impede the device reliability and degrade its power efficiency; thereby shortening the lifetime expectancy. Leakage current, which reduces the breakdown voltage and the power-added efficiency while increasing the noise figure, generally appears because of the conductive nature of gallium nitride (GaN) as well as surface processing and passivation issues. Quantum mechanical tunneling can create gate-to-drain leakage currents via electron hopping from trap to trap [8]. Dispersion of drain current (I_D) and increase in the dynamic on-resistance (R_{ON}), which are indicative of current collapse, are caused due to the trapping of electrons by surface traps [9-11] and bulk traps [12-14] existing at various locations including the metal/AlGaN interface, the ungated AlGaN surface near the date edge, and buffer GaN layer during device operation in the AlGaN/GaN heterostructure.

A promising approach to minimize the off-state leakage current, and therefore, yield good channel pinch-off characteristics and high breakdown voltage involves enhancing the total electrical isolation between the devices using semi-insulating GaN buffer layers such as SiO_2, Si_3N_4, HfO_2, Al_2O_3, or other oxides [15, 16]. Substantial progress in atomic layer deposition (ALD) in conjunction with the attractive features of Al_2O_3 such as its large bandgap (9 eV), high dielectric constant (~ 10), high breakdown field (10^7 V/cm), thermal stability, and chemical stability against AlGaN have attracted research interest towards implementing gate dielectrics using Al_2O_3 [17, 18]. However, when using Al_2O_3, special attention should be paid to the subsequent process temperature. Based on transmission electron microscopy (TEM) investigations, C. Mizue *et al.* [19] observed that the as-deposited ALD-Al_2O_3 layer exhibited an amorphous-phase structure and that the Al_2O_3/GaN interface was uniformly flat. However, annealing of the film at 800 ℃, which is a typical temperature for the formation of ohmic electrodes, generated a large number of microcrystallized regions in the Al_2O_3 layer, causing a marked increase in the leakage current of the Al_2O_3/GaN structure. S. Toyoda *et al.* [20] also reported that annealing procedures at 800 ℃ resulted in the phase transformation of Al_2O_3 films from amorphous to crystalline. To address this issue, a surface protection layer is considered indispensable to avoid the chemical bond disorder on the AlGaN surface during the

annealing process. Many efforts made to suppress current collapse in AlGaN/GaN HEMTs are directly related to the modification of surface/interface states in AlGaN/GaN heterostructures. These modifications include surface passivation [21], the application of a thin AlN barrier layer in the AlGaN/GaN interface [22], application of a field plate [23], surface treatments with chemicals or plasma [24], and post-gate-annealing [25]. Among these various techniques to engineer electrically active surface states for improved device performance, the most popular approach involves surface passivation using dielectrics such as Si_3N_4 and oxides. The passivation process increases the density of surface states and buries traps, which become inaccessible to electrons from the gate [26]. In addition, the passivation layer reduces the edge electric field near the gate at the drain side, leading to minimized electron injection from the gate to the AlGaN surface, thereby reducing electron trapping at the AlGaN surface [9]. To suppress the surface-state-induced current collapse, a thick SiN_x layer (~120 nm) is grown by plasma-enhanced chemical vapor deposition (PECVD) typically at temperatures below 350 ℃ to passivate the (Al)GaN surface along with in-*situ* or ex-*situ* pre-treatments [5], [10]. However, because of the large thermal mismatch with GaN, the thick PECVD-SiN_x passivation layer may crack after rapid thermal annealing (RTA) (>800 ℃) in a passivation-prior-to-ohmic process, which could be a preventive solution for the suppression of surface states in AlGaN/GaN heterostructure. The deposition of a thin SiN_x layer by PECVD or grown *in-situ* by metal-organic chemical vapor deposition (MOCVD) on fresh AlGaN/GaN supporting wafers could form an alternative method to suppress the formation of surface states; however, the effectiveness of this approach may be limited by the film thickness. Low-pressure chemical vapor deposition (LPCVD)-grown SiN_x passivation has recently generated considerable interest in terms of high-temperature and plasma-free deposition process, which can lead to high film quality and less damage to the AlGaN barrier [27-29]. However, the effectiveness of such passivation layer [30], [31] to suppress current collapse has only been confirmed at low drain bias (< 100 V) [32]. Furthermore, LPCVD-grown single-layer SiN_x passivation suffers from gate current noise spectra and a large current slump [33, 34].

Illustrated here is an approach to generate a robust $SiN_x/Al_2O_3/SiN_x$/AlGaN interface using LPCVD-grown bilayer stoichiometric SiN_x-based pre-passivation and PECVD-grown SiN_x-based post-passivation of a plasma-enhanced atomic layer deposition (PEALD)-grown Al_2O_3 gate dielectric. Transmission electron microscopy/energy-dispersive x-ray spectroscopy (TEM/EDX) mapping technology is used for comprehensive study of interface trap and the underlying mechanism of current collapse suppression. In addition, static characterization, DC pulse tests, and accelerated three-temperature operating life tests are used to demonstrate the validity of the proposed method to develop ultralong-lifetime AlGaN/GaN HEMTs.

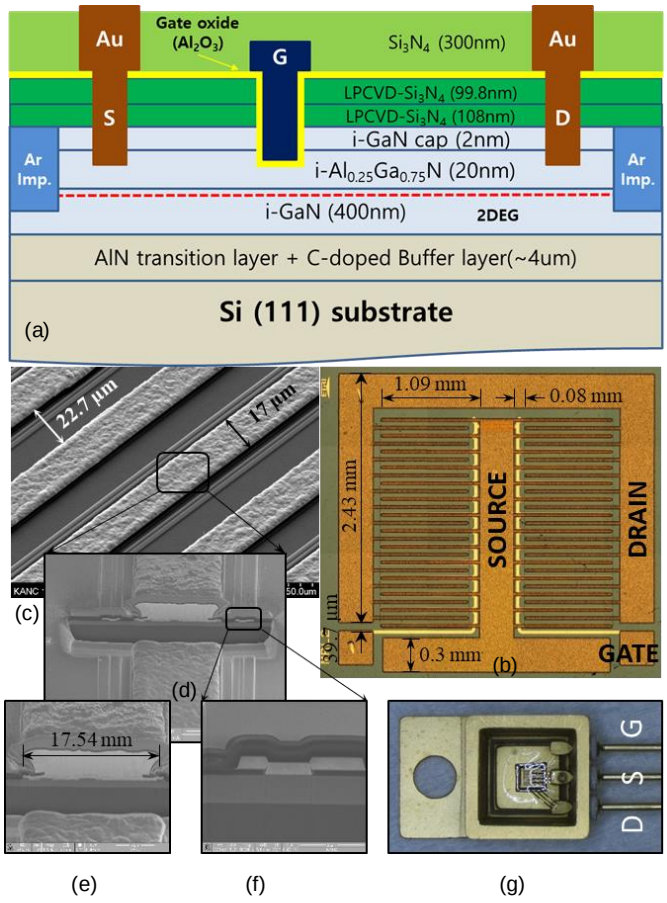


Fig. 1. (a) Schematic cross-sectional layout of proposed HEMT, (b) optical microscopy image of a fabricated sample, (c) Scanning electron microscopy (SEM) image of a portion of the fabricated sample, (d) Focused ion beam (FIB) image showing drain and gate electrode, (e) Magnified image of the drain, (f) magnified image of the gate, and (g) picture of a packaged HEMT.

This paper is organized as follows: Section II begins by outlining the method to fabricate the proposed HEMT based on LPCVD-grown stoichiometric SiN_x pre-passivation, PEALD-grown Al_2O_3 gate deposition, and PECVD-grown SiN_x post-passivation. In addition, an experimental setup for accelerated-three-temperature operating life test is illustrated. For the developed HEMTs, the performance characterization using surface morphology, transfer characteristics and interface trap analyses and operation lifetime examination using time to failure (TTF) and mean time to failure (MTTF) are presented and discussed in Section III. Our conclusions are drawn in Section IV.

II. Methods and Materials

A. HEMT Structure and Fabrication

The proposed high-reliability AlGaN/GaN HEMT, whose schematic cross-section is shown in Fig. 1(a), was fabricated on a 4-inch GaN-on-Si (111) epi-wafer. The epi-structure consists of an undoped GaN cap layer (2 nm) and undoped $Al_{0.25}Ga_{0.75}N$ barrier layer (20 nm) on an undoped GaN layer (400 nm) with a 2DEG channel. Since the carbon-doped buffer layer features

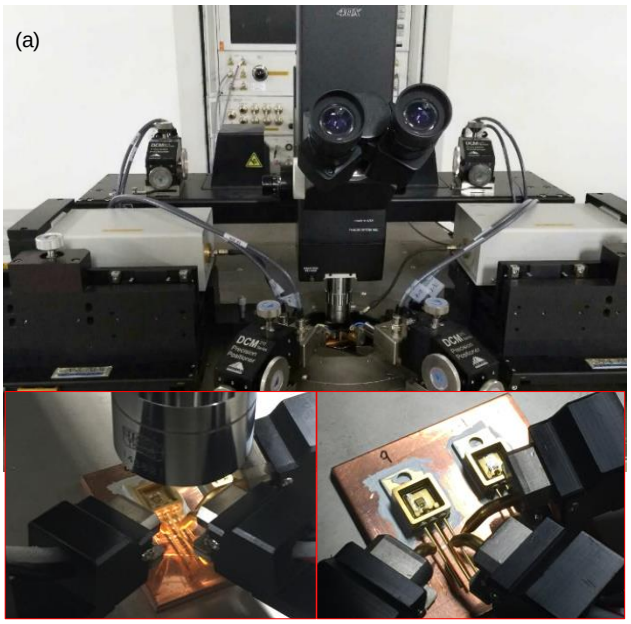


Fig. 2. (a) DC characterization and accelerated three-temperature operating life test setup for packaged AlGaN/GaN HEMT samples, (b) and (c) magnified images illustrating probe station connected with packaged HEMT electrodes for supplying controlled voltages.

a high bandgap and therefore the capacity to compensate for the native defects, we adopted this buffer layer (~4 μm) to increase the breakdown voltage and reduce the substrate leakage current of the device [35]. Ar-ion implantation and a multilayer of Ti/Al/Ni/Au metal deposited by using an e-beam evaporator was used for planar structure device isolation and source/drain ohmic contacts, respectively. A 99.8 nm [measured using transmission electron microscopy (TEM)] thick layer of Si-rich LPCVD-grown SiN_x [dichlorosilane (SiH_2Cl_2) flow of 200 sccm, gas flow ratio (SiH_2Cl_2:ammonia (NH_3)) of 6:1, and deposition rate of 2.5 nm/min) was first deposited at 780 ℃. It was followed by the deposition of LPCVD-grown 108 nm thick Si-poor (stoichiometric silicon) SiN_x (SiH_2Cl_2 flow of 70 sccm and SiH_2Cl_2:NH_3 flow of 1:3, and deposition rate of 5.5 nm/min).

A 30-nm-thick Al_2O_3 gate dielectric layer was deposited via PEALD process. The Al_2O_3 films were loaded into a PEALD LL SENTECH Instruments GmbH reactor. The ALD system was equipped with a remote capacitively coupled plasma source excited by a 13.56-MHz RF generate via a matchbox, and the power supply rating was 200 W. Depositions were carried out at 205 ℃ using trimethylaluminum (TMA) as aluminum precursor and O_2 plasma as the oxygen source with an oxygen flow of 150 sccm. TMA was delivered from the bubbler to the reactor with N_2 carrier gas at a flow rate of 40 sccm. The pulse times of the metal precursor and oxygen pulse were 0.06 and 1 s, respectively. After each precursor pulse, the deposition chamber was purged with 40 sccm of N_2 for 2 s to remove unreacted precursors.

Following Al_2O_3 deposition, gate contacts were formed using Ni/Au metal. After the formation of a 300-nm-thick dielectric passivation layer, Au plating was used for interconnecting the source and drain multi-fingers of the high-power device. All devices had a total gate periphery of 20 × 1000 μm. The gate length, gate–source, and gate–drain spacing values were 1.5, 3.0, and 15 μm, respectively. For post-passivation, a 300 nm thick SiN_x was deposited using PECVD at a chamber pressure and temperature of 111.4 Pa and 150 ℃, respectively, radio-frequency (RF) of 13.56 MHz and RF power of 60 W [36**]**. The previously reported works have demonstrated that the use of post-passivation SiN_x reduces the trapping effects; thereby improving HEMT DC characteristics and peak intrinsic transconductance with threshold voltage [37, 38]. All test samples were packaged as shown in Fig. 1(g) and placed on the temperature controlled heating blocks during the test. Fig. 1(b) depicts the optical microscopy image of a fabricated HEMT showing the source (S), gate (G), and drain (D) electrodes. A scanning electron microscopy (SEM) image of a portion of the fabricated HEMT is shown in Fig. 1(c). The focused ion beam (FIB) cross-section images of the drain and gate electrode are shown in Fig. 1(d) and the magnified cross-section image of the drain electrode is shown in Fig. 1(e). Fig. 1(f) shows the magnified cross-section image of the gate electrode.

B. Accelerated Three-Temperature Operating Life Test

An accelerated three-temperature operating life test was carried out to evaluate the MTTF of AlGaN/GaN HEMTs. Three devices under each test condition were accelerated under the bias and elevated temperature conditions. The conditions included controlled drain biases for maintaining a constant drain current (I_D) of 2 A and three temperatures of 260 ℃, 280 ℃, and 300 ℃. Device parameters such as drain current (I_D), drain voltage (V_D), and gate current (I_D) were monitored using a Tektronix 370A curve tracer with real-time data acquisition

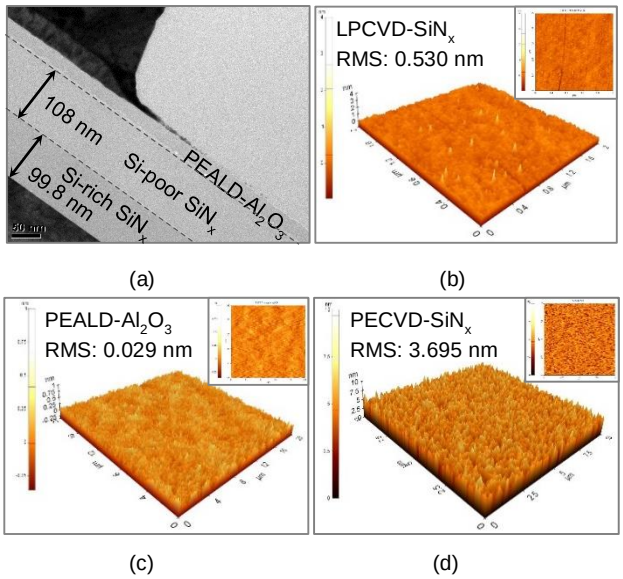
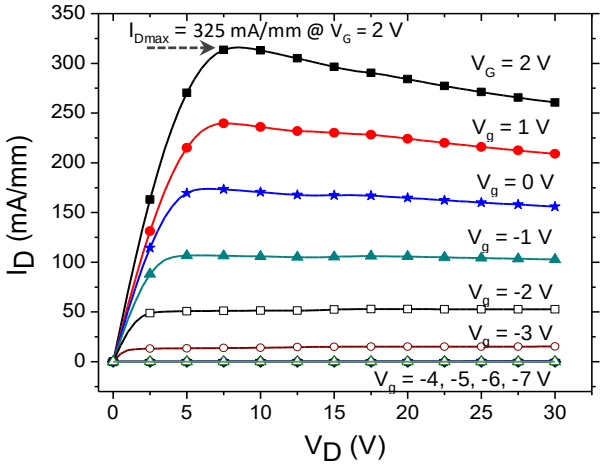


Fig. 3. Morphological analysis using atomic force microscopy (AFM) in 2 × 2 μm^2. (a) TEM image showing LPCVD-bilayer and PEALD-Al_2O_3, (b) 3D surface profile of LPCVD-grown SiN_x passivation layer and corresponding 2D image of the same area, (c) 3D surface profile of PEALD-grown AL_2O_3 gate dielectric and corresponding 2D image of the same area, and (d) 3D surface profile of PECVD-grown SiN_x passivation layer and corresponding 2D image of the same area.



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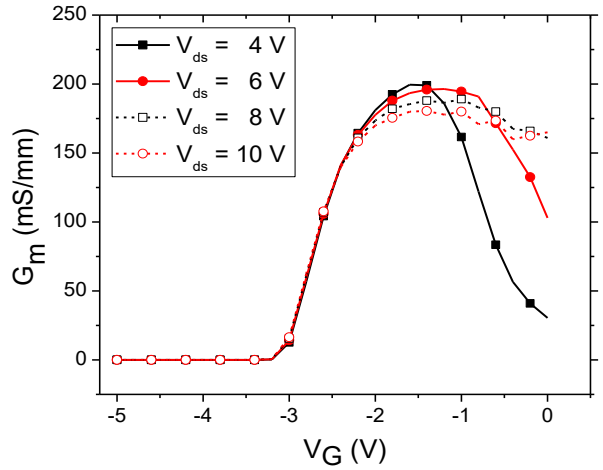
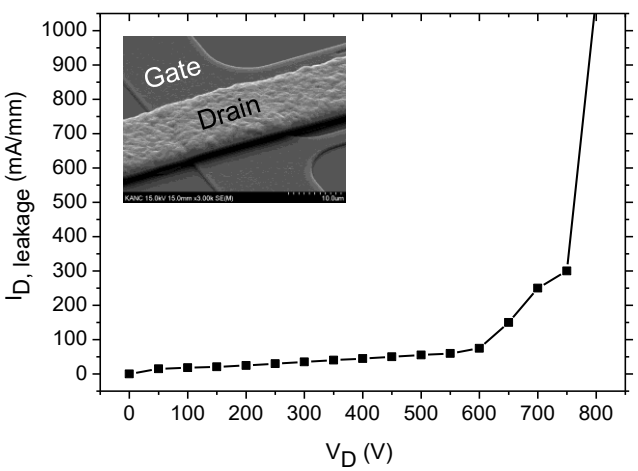


(b)

Fig. 4. (a) I_D-V_D characteristics of a representative AlGaN/GaN HEMT at various gate bias voltages (V_G) and (b) dependence of HEMT transconductance on gate voltage (V_G).



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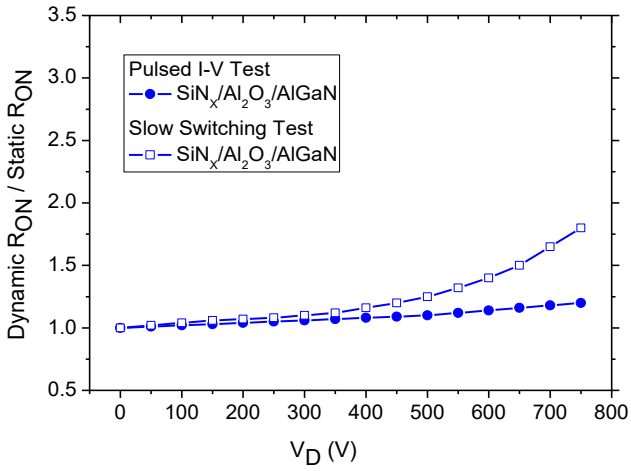

(b)

Fig. 5. (a) Plot of the leakage current ($I_{D,\ leakage}$) against the variation in V_D, indicating the high breakdown voltage (763.2 V) and (b) plot of dynamic R_{ON}/static R_{ON} based on pulsed I–V and slow switching tests.

software and a computer control system. Fig. 2 illustrates the test setup for DC characterization of the HEMT samples and accelerated three-temperature operating life tests to estimate the MTTF.

III. Results and Discussions

A. Surface Characterization of Pre- and Post- Passivation Layers (SiN_x) and Al_2O_3 Gate Dielectric

Fig. 3(a) illustrates TEM cross-section image indicating LPCVD-grown pre-passivation SiN_x bilayer and PEALD-grown Al_2O_3 gate dielectric. Fig. 3(b), (c), and (d) illustrate the surface morphology of LPCVD-grown SiN_x pre-passivation layer, PEALD-grown Al_2O_3 gate dielectric, and PECVD-grown post-passivation SiN_x layer, respectively, characterized using atomic force microscopy (AFM). For quintuplicate analysis of surface morphology, AFM images of the surfaces of samples from the center, top, bottom, left, and right edge were taken. The images show that the high quality films with crack-free, continuous and smooth surfaces were obtained. The mean value and relative standard deviation (RSD) of root mean square (RMS) surface roughness obtained within a $2 \times 2\ \mu m^2$ area after SiN_x pre-passivation was found to be (0.187 ±5.01%) nm. After deposition of the Al_2O_3 layer, the RMS surface roughness was (0.08 ±2.37%) nm. This result indicates that the PEALD Al_2O_3 has good step coverage and thickness uniformity. The RMS surface roughness of PECVD-SiN_x post-passivation was found to be (0.673 ±9.99%) nm.

B. HEMT DC Characterization

The static drain current-voltage (I_D-V_D) characteristics of the fabricated HEMT samples, which were measured for all the devices at room temperature (25 °C) and in the dark, are shown in Fig. 4(a). The results indicated a positive correlation between the saturated drain current (I_{Dsat}) with the gate voltage (V_G) for a swing of -7 to 2 V. The studied AlGaN/GaN HEMT fabricated with a gate-to-source distance, gate-to-drain distance and gate length of $L_{GS}/L_{GD}/L_G$ = 2 µm/15 µm/1.5 µm deliver excellent DC characteristics with a maximum drain current density (I_{Dmax}) of 325 mA/mm at a gate voltage (V_G) of 2 V (Fig. 4 (b)), suggesting the high quality of the material. The threshold voltage, which is defined as the gate bias at a drain current of 1 µA/mm, was -4.6 V. In addition, self-heating-induced degradation in I_{Dsat} is evident at the higher drain voltages when V_G exceeds null voltage. Fig. 4(b) shows the G_m-V_G characteristics of the fabricated AlGaN/GaN HEMT. The peak

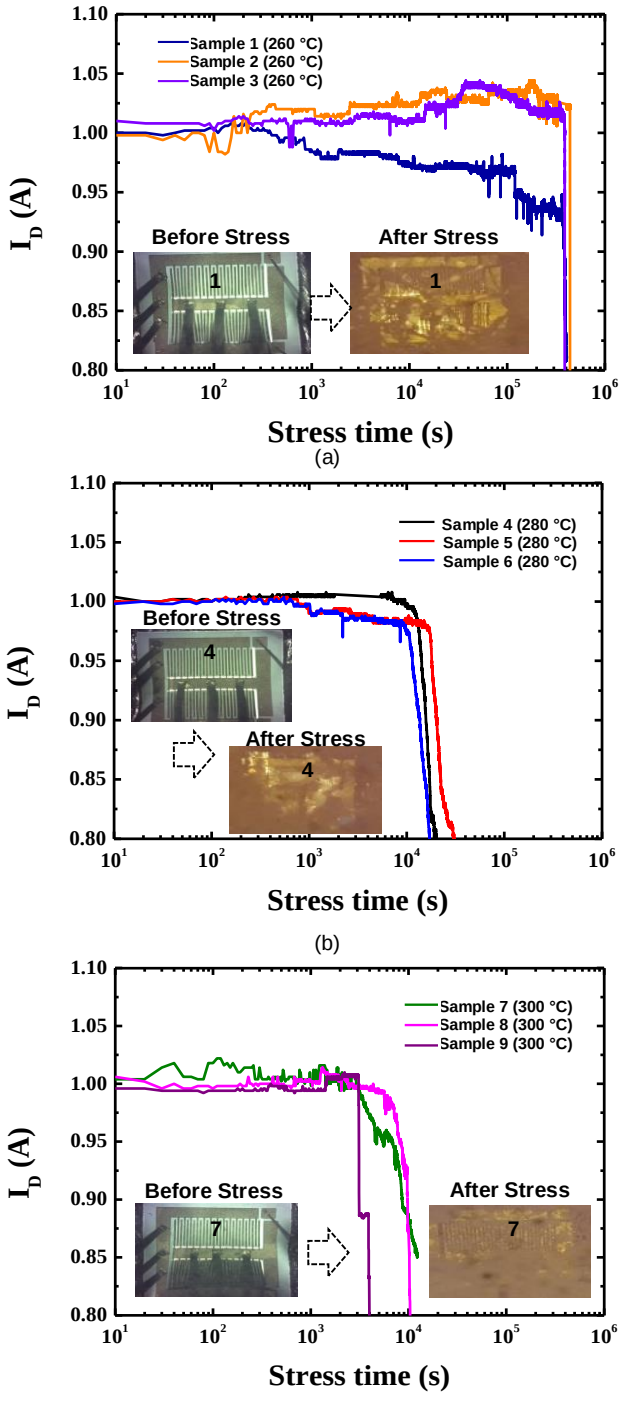

Fig. 6. Degradation in drain current (I_D) under accelerated temperature lifetime test and calculation of time to failure (TTF) based on 15% degradation in I_D. (a) Degradation in I_D for HEMT samples 1, 2, and 3 at channel temperature (T_C) of 260 °C and images of the samples before and after stress test, (b) Degradation in I_D for HEMT samples 4, 5, and 6 at T_C of 250 °C and the images of the samples before and after stress test, and (c) Degradation in I_D for HEMT samples 7, 8, and 9 at T_C of 300 °C and the pictures of the samples before and after stress test.

G_m value at V_{DS} of 4 V was 199.5 mS/mm in the study.

Fig. 5(a), which plots the leakage current (I_D) against variation in V_D, indicates the presence of a very low drain leakage current up to a very high value of V_D. In addition, the

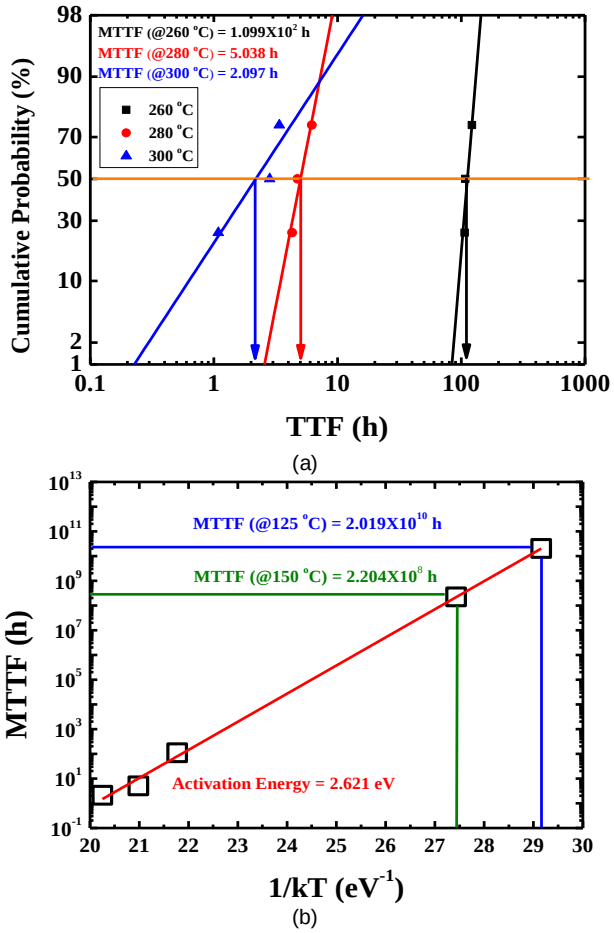

Fig. 7. Lifetime expectancy estimation of HEMTs based on accelerated three-temperature test. (a) Cumulative probability of times to failure (TTFs) for HEMTs operating at temperatures of 260, 280, and 300 °C and (b) Arrhenius plot showing mean TTFs at two different temperatures of 125 and 150 °C with extracted activation energy of 2.621 eV.

HEMT exhibited a very high breakdown voltage of 763.2 V, thereby indicating the robustness and high-temperature stability of the bilayer passivated SiN_x layer. The on-resistance ratio (dynamic R_{ON}/static R_{ON}), which is indicative of the current collapse in HEMTs, is plotted in Fig. 5(b) as a function of V_D. The value of $R_{ON, static}$ and $R_{ON, dynamic}$ were 0.23 Ω and 0.27 Ω, respectively; thus leading to a very low ratio ($R_{ON, dynamic}$/ $R_{ON, static}$) of1.067 as per the pulsed I–V test of the $SiN_x/Al_2O_3/SiN_x$-SiN_x/AlGaN interface. In addition, the slow switching test indicated a small rise in the on-resistance, thus indicating the effective suppression of current collapse in the fabricated HEMTs.

C. TTF and MTTF Characterization

An examination of degradation in I_D, which is caused by either degradation of the active channel of the device or ecrease in the donor density in the channel is useful for accelerated temperature life test-based lifetime estimation of devices. In general, an approximate I_D degradation of 10-20% is used to define failure of a HEMT. Fig. 6 illustrates the I_D degradation in 9 HEMT samples before and after accelerated-temperature tests. Fig. 6 also shows the variation in I_D induced by stress at $V_{GS} = -5$ V, $V_{DS} = 600$ V for the 9 identically fabricated HEMT

samples with stress time. The results indicate that I_D for each sample exhibits an abrupt drop after approximately 10^4 s. The TTFs, which were calculated based on a 15% drop of I_D and are listed in Table I, indicated the strong dependence of the HEMT TTF on the operating channel temperature (T_C). In addition, the failure time curve exhibits a small variability, with a minimum of 106.9 h to a maximum of 122.2 h for a single temperature.

The curves of the lognormal plot of the cumulative density function of the lifetime distribution are shown in Fig. 7(a); these plots afford an insight into understanding the process lifetime and reliability. The results correspond to high-temperature testing of sample sets across three lots. The high-temperature lifetime can be directly estimated from the plot at 50% failure (1.099×10^2 h at 260 ℃), (5.038 h at 280 ℃) and (2.097 h at 300 ℃). Similarly, the long operation lifetime at 25% failure

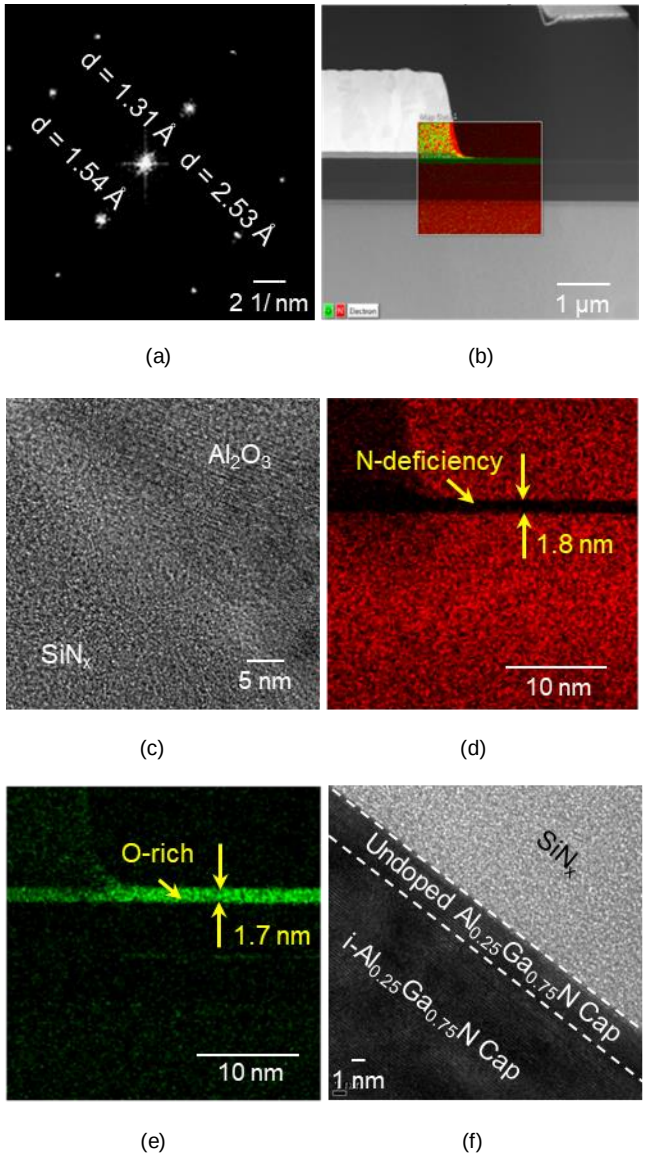

Fig. 8. (a) X-ray diffraction pattern of LPCVD-SiN_x. Element distribution of SiN_x/AlGaN interface analyzed by TEM-EDX mapping, (b) cross-sectional view, (c) magnified view of cross-section of LPCVD-SiN_x/PEALD-Al_2O_3 interface, (d) Nitrogen, (e) Oxygen, and (f) high-resolution micrograph of LPCVD-SiN_x/AlGaN interface marked in the red square of (b).

TABLE I
TTF (15% DEGRADATION POINT) OF THE DEVELOPED HEMTS

Sample	Temperature (℃)	TTF (h)
1	260	1.069×10^2
2	260	1.222×10^2
3	260	1.079×10^2
4	280	4.748
5	280	6.189
6	280	4.299
7	300	1.088
8	300	2.831
9	300	1.088

(1.069×10^2 h at 260 ℃, 4.299 h at 280 ℃, 1.088 h at 300 ℃) and 75% failure (1.222×10^2 h at 260 ℃, 6.189 h at 280 ℃, 3.38 h at 300 ℃) were found. Fig. 7(b) shows the estimate of the MTTF based on the results of the three-temperature GaN HEMT life test. From the median lifetime for each channel temperature as indicated by Arrhenius fit, an activation energy of 2.621 eV was extracted which corresponds to an extrapolated MTTF at a channel temperature of 125 ℃ and 150 ℃ to 2.019×10^{10} h and 2.204×10^8 h, respectively.

D. Interface Trap Characterization

The interplanar spacings of the LPCVD-SiN_x passivation layer, which were determined through the selected area diffraction (SAD) image by X-ray diffraction equipment incorporated in the TEM measurement system, are illustrated in Fig. 8(a); we note from the figure that these spacing are very small. This result suggests that the proposed bilayer LPCVD-SiN_x passivation technique yields a compact structure, and therefore, effectively prevents the passivation/(Al)GaN interface from being oxidized by H_2O or oxygen. To further investigate the possible sources of the interface traps, TEM-EDX mapping of the passivation/AlGaN interface was performed. Fig. 8(b) and (c) illustrate the cross-section of the interface with the red square shaded area indicating the analyzed portion and the magnified cross-section view of the stoichiometric bilayer LPCVD-SiN_x/PEALD-Al_2O_3 interface, respectively. Figs. 8(d) and (e), which reveal N- deficient and O-rich regions on the surface of the AlGaN barrier in the LPCVD-SiN_x-passivated HEMTs, respectively, demonstrate the presence of a sharp interface (1.8 nm) and narrow oxygen-contaminated region (1.7 nm), respectively, thereby indicating the AlGaN surface was effectively protected in critical processes such as ohmic annealing. From Fig. 8(f), which shows the high-resolution micrograph of LPCVD-SiN_x/AlGaN interface marked by the red square in Fig. 8(b), we note that the formation of a continuous crystalline layer effectively passivates the dangling bonds on the Ga(Al)-terminated AlGaN surface, and thus lowers the interface traps in LPCVD-grown bilayer passivated AlGaN/GaN HEMTs [39].

IV. CONCLUSION

LPCVD-grown bilayer SiN_x-based pre-passivation and PECVD-grown SiN_x-based post-passivation of PEALD-grown Al_2O_3 gate dielectric was investigated to generate a robust and

high-reliability interface ($SiN_x/Al_2O_3/SiN_x$-SiN_x) for effective suppression of current collapse and reduction of leakage current in AlGaN/GaN HEMTs. Both the observed low static-on resistance (0.23-Ω) and dynamic R_{ON}/static R_{ON} validated the suppression of current collapse in the developed HEMTs. In addition, a very low drain leakage current observed even at very high drain voltages together with a high HEMT breakdown voltage indicated the effectiveness of the proposed multilayer SiN_x-based passivation technique. Moreover, a very long operation lifetime expectancy as revealed by the accelerated three-temperature life test and effectively suppressed interface traps as indicated by TEM-EDX mapping demonstrated that the LPCVD-based bilayer passivation prior-to-Al_2O_3 gate dielectric can be used to develop ultralong-lifetime AlGaN/GaN HEMTs for high-power applications.

REFERENCES

[1] Y. Z. Chiou, S. J. Chang, Y. K. Su, C. K. Wang, T. K. Lin, and B. R. Huang, "Photo-CVD SiO2 layers on AlGaN and AlGaN–GaN HEMT" *IEEE Trans. Electron Devices*, vol. 50, no. 8, pp. 1748–1752, Aug. 2003.

[2] H. C. Chiu, H. C. Wang, C. W. Yang, F. H. Huang, H. L. Kao, and H. K. Lin, "A novel micromachined AlGaN/GaN power HEMT with air-bridged matrix heat redistribution layer design," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp 163-165, Feb. 2014.

[3] H. Y. Liu, W. C. Hsu, C. S. Lee, B. Y. Chou, Y. B. Liao, and M. H. Chiang, "Investigation of temperature-dependent characteristics of AlGaN/GaN MOS-HEMT by using hydrogen peroxide oxidation technique," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2760–2766, Aug. 2014.

[4] R. Sun, Y. C. Liang, Y. C. Yeo, Y. H. Wang, and C. Zhao, "Realistic trap configuration scheme with fabrication processes in consideration for the simulations of AlGaN/GaN MIS-HEMT devices" *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 4, no. 3, pp. 720–729, Sept. 2017.

[5] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, "A review of GaN on SiC high electron-mobility power transistors and MMICs," *IEEE Trans. Microw. Theory Techn*., vol. 60, no. 6, pp. 261–264, Jun. 2012.

[6] G. Dutta, S. Turuvekere, N. Karumuri, N. Dasgupta, and A. Dasgupta, "Positive shift in threshold voltage for reactive-ion-sputtered Al_2O_3/AlInN/GaN MIS-HEMT," *IEEE Electron Device Lett*., vol. 35, no. 11, pp. 1085–1087, Nov. 2009.

[7] U. K. Mishra, P. Parikh, and Y.-F. Wu, "AlGaN/GaN HEMTs: An overview of device operations and applications," *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002.

[8] A. Mimouni, T. Fernández, J. Rodriguez-Tellez, A. Tazon, H. Baudrand, and M. Boussuis, "Gate leakage current in GaN HEMT's: A degradation modeling approach," *Electr. Electron. Eng*., vol. 2, no. 6, pp. 397–402, Feb. 2012.

[9] M. Faqir, G. Verzellesi, A. Chini, F. Fantini, F. Danesin, G. Meneghesso, E. Zanoni, and C. Dua, "Mechanisms of RF current collapse in AlGaN-GaN high electron mobility transistors," *IEEE Trans. Device Mater. Rel*., vol. 8, no. 2, pp. 240–247, Jun. 2008.

[10] O. Mitrofanov and M. Manfra, "Dynamics of trapped charge in GaN/AlGaN/GaN high electron mobility transistors grown by plasma-assisted molecular beam epitaxy," *Appl. Phys. Lett*., vol. 84, pp. 422–424, Jan. 2004.

[11] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, Mar. 2001.

[12] P. B. Klein and S. C. Binari, "Photoionization spectroscopy of deep defects responsible for current collapse in nitride-based field effect transistors," *J. Phys. Condens. Matter*, vol. 15, no. 44, p. R1641–R1666, Oct. 2003.

[13] P. B. Klein, S. C. Binari, K. Ikossi, A. E. Wickenden, D. D. Koleske, and R. L. Henry, "Current collapse and the role of carbon in AlGaN/GaN high electron mobility transistors grown by metalorganic vapor-phase epitaxy," *Appl. Phys. Lett*., vol. 79, pp. 3527–3529, Sep. 2001.

[14] S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, P. Doewon, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "Trapping effects and microwave power performance in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 48, pp. 465–471, Mar. 2001.

[15] O. I. Saadat, J. W. Chung, E. L. Piner, and T. Palacios, "Gate-first AlGaN/GaN HEMT technology for high-frequency applications," *IEEE Electron Device Lett*., vol. 30, no. 12, pp. 1254–1256, Dec. 2009.

[16] M. Ochiai, M. Akita, Y. Ohno, S. Kishimoto, K. Maezawa, and T. Mizutani, "AlGaN/GaN heterostructure metal-insulator-semiconductor high-electron-mobility transistors with Si_3N_4 gate insulator," *Jpn. J. Appl. Phys*., vol. 42, pp. 2278–2280, Apr. 2003.

[17] R. Lossy, H. Gargouri, M. Arens, and J. Wurfl, "Gallium nitride MIS-HEMT using atomic layer deposited Al_2O_3 as gate dielectric," *J. Vac. Sci. Technol. A*, vol. 31, no. 1, pp. 01A140-1-5, Dec. 2012.

[18] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Hwang, "GaN metal oxide semiconductor high electron mobility transistor with atomic layer deposited Al_2O_3 as gate dielectric," *Appl. Phys. Lett.*, vol. 86, pp. 063501-1-3, Jan. 2005.

[19] C. Mizue, Y. Hori, M. Miczek, and T. Hashizume, "Capacitance-voltage characteristics of Al_2O_3/AlGaN/GaN structures and state density distribution at Al_2O_3/AlGaN interface," *Jpn. J. Appl. Phys*., vol. 50, pp. 021001-1-7, Feb. 2011.

[20] S. Toyoda, T. Shinohara, H. Kumigashira, M. Oshima, and Y. Kato, "Significant increase in conduction band discontinuity due to solid phase epitaxy of Al_2O_3 gate insulator films on GaN semiconductor," *Appl. Phys. Lett.*, vol. 101, pp. 231607-1-4, Dec. 2012.

[21] R. Coffie, D. Buttari, S. Heikman, S. Keller, A. Chini, L. Shen, and U. K. Mishra, "p-capped GaN-AlGaN–GaN high-electron mobility transistors (HEMTs)," *IEEE Electron Device Lett*., vol. 23, no. 10, pp. 588–590, Oct. 2002.

[22] J. S. Lee, J. W. Kim, J. H. Lee, C. S. Kim, J. E. Oh, and M. W. Shin, "Reduction of current collapse in AlGaN/GaN HFETs using AlN interfacial layer," *Electronics Lett*., vol. 39, no. 9, pp. 750–752, May 2003.

[23] Y. F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra, and P. Parikh, "30-W/mm GaNHEMTs by field plate optimization," *IEEE Electron Device Lett*., vol. 25, no. 3, pp. 117–119, Mar. 2004.

[24] M. F. Romero, A. Jiménez, J. Miguel-Sánchez, A. F. Braña, F. González-Posada, R. Cuerdo, F. Calle, and E. Muñoz, "Effects of N_2 plasma pretreatment on the SiN passivation of AlGaN/GaN HEMT," *IEEE Electron Device Lett*., vol. 29, no. 3, pp. 209–211, Mar. 2008.

[25] N. Miura, T. Nanjo, M. Suita, T. Oishi, Y. Abe, T. Ozeki, H. Ishikawa, T. Egawa, and T. Jimbo, "Thermal annealing effects on Ni/Au based Schottky contacts on n-GaN and AlGaN/GaN with insertion of high work function metal," *Solid-State Electron*., vol. 48, pp. 689–695, May 2004.

[26] P. Gamarra, C. Lacam, M. Tordjman, J. Splettstösser, B. Schauwecker, and M. D. Forte-Poisson, "Optimisation of a carbon doped buffer layer for AlGaN/GaN HEMT devices," *J. Cryst. Growth*, vol. 414, pp. 232–236, Oct. 2014.

[27] R. M. Hua, C. Liu, S. Yang, S. H. Liu, Y. Y. Lu, K. Fu, Z. H. Dong, Y. Cai, B. S. Zhang, and K. J. Chen, "650-V GaN-based MIS-HEMTs using LPCVD SiN*x* as passivation and gate dielectric," in *Proc. ISPSD*, May 2015, pp. 241–244.

[28] Z. L. Zhang, G. H. Yu, X. D. Zhang, X. G. Deng, S. M . Li, Y. M. Fan, S. C. Sun, L. Song, S. X. Tan, D. D. Wu, W. Y. Li, W. Huang, K. Fu, Y. Cai, Q. Sun, and B. S. Zhang, "Studies on high-voltage GaN-on-Si MIS-HEMTs using LPCVD Si3N4 as gate dielectric and passivation layer," *IEEE Trans. Electron Devices*, vol. 63, no. 2, pp. 731–738, Feb. 2016.

[29] M. Hua, Y. Lu, S. Liu, C. Liu, C. Liu, K. Fu, Y. Cai, B. Zhang, and K. J. Chen, "Compatibility of AlN/SiN_x passivation with LPCVD-SiN*x* gate dielectric in GaN-based MIS-HEMT," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp 265-268.

[30] J. R. Shealy, T. R. Prunty, E. M. Chumbes, and B. K. Ridley, "Growth and passivation of AlGaN/GaN heterostructures," *J. Cryst. Growth*, vol. 250, no. 1–2, pp. 7–13, Mar. 2003.

[31] S.-W. Moon, J. Lee, D. Seo, S. Jung, H. G. Choi, H. Shim, J. S. Yim, J. Twynam, and S. D. Roh, "High-voltage GaN-on-Si hetero-junction FETs with reduced leakage and current collapse effects using SiN*x* surface passivation layer deposited by low pressure CVD," *Jpn. J. Appl. Phys.*, vol. 53, no. 8S3, p. 08NH02, Aug. 2014.

[32] X. Wang, S. Huang, Y. Zheng, K. Wei, X. Chen, G. Liu, T. Yuan, W. Luo, L. Pang, H. Jiang, J. Li, C. Zhao, H. Zhang, and X. Liu, "Robust SiN*x* /AlGaN interface in GaN HEMTs passivated by thick LPCVD-

grown SiN*x* layer," *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 666–668, Jul. 2015.

[33] T. Huang, A. Malmros, J. Bergsten, S. Gustafsson, O. Axelsson, M. Thorsell, and N. Rorsman, "Suppression of dispersive effects in AlGaN/GaN high electron-mobility transistors using bilayer SiNx grown by low pressure chemical vapor deposition," *IEEE Electron Device Lett*., vol. 36, no. 6, pp. 537–539, Jun. 2015.

[34] T. Huang, J. Bergsten, M. Thorsell, and N. Rorsman, "Small- and large-signal analyses of different low-pressure-chemical-vapor-deposition SiN_x passivations for microwave GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 908–914, Jan. 2018.

[35] T.-H. Hung, P. S. Park, S. Krishnamoorthy, D. N. Nath, and S. Rajan, "Interface charge engineering for enhancement-mode GaN MISHEMTs," *IEEE Electron Device Lett*., vol. 35, no. 3, pp. 312–314, Mar. 2014.

[36] S. J. Cho, C. Wang, and N. Y. Kim, "Effects of double passivation for optimize DC properties in gamma-gate AlGaN/GaN high electron mobility transistor by plasma enhanced chemical vapor deposition," *Thin Solid Films*, vol. 520, no. 13, pp. 4455–4458, Apr. 2012.

[37] S. J. Cho, C. Wang, and N. Y. Kim, "Effects of double passivation for optimize DC properties in gamma-gate AlGaN/GaN high electron mobility transistor by plasma enhanced chemical vapor deposition" *Thin Solid Films*, vol. 520, no. 13, pp. 4455–4458, Feb. 2012.

[38] S. J. Cho, X. Li, I. Guiney, K. Floros, D. Hemakumara, D. J. Wallis, C. Humphreys, and I. G. Thaync, "Impact of stress in ICP-CVD SiN_x passivation films on the leakage current in AlGaN/GaN HEMTs" *Electron*. *Lett*., vol. 54, no. 15, pp. 947–949, Jul. 2018.

[39] X. Y. Qin, H. Dong, J. Y. Kim, and R. Wallace, "A crystalline oxide passivation for Al_2O_3/AlGaN/GaN,"*Appl*. *Phys*. *Lett*., vol. 105, no. 14, p. 141604–1–5, Oct. 2014.