

Pagination 32-bit

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Upper portion of a virtual address is used to to identify a series of paging-structure entries. The last of these entries identifies the physical address of the region to which the linear address translates (called the **page frame**). The lower portion of the linear address (called the **page offset**) identifies the specific address within that region to which the linear address translates.

The first paging structure is located at the physical address in CR3.

With 32-bit paging, each paging structure comprises $1024 = 2^{10}$ entries. For this reason, the translation process uses 10 bits at a time from a 32-bit linear address.

Bits 31:22 identify the first paging-structure entry. (Page directory)

Bits 21:12 identify a second. The latter identifies the page frame. (Page table)

Bits 11:0 of the linear address are the page offset within the 4-KByte page frame ($2^{12} = 4096$)

Si une page est mappe depuis la premiere etape (un seul niveau de referencement), alors la page frame fait $2^{22} = 4\,194\,304\text{ KiB} = 4\text{ MB}$.

A directory is located at the physical address specified in bits 31:12 of CR3.

A PD contains 1024 PDE, a PDE is selected using the PA defined as follows :

Bits 39:32 are all 0

Bits 31:12 are from CR3.

Bits 11:2 are bits 31:22 of the linear address.

Bits 1:0 are 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Address of page directory ¹																		Ignored				P C D	PW T	Ignored			CR3					
Bits 31:22 of address of 4MB page frame						Reserved (must be 0)				Bits 39:32 of address ²				P A T	Ignored	G	1	D	A	P C D	PW T	U / S	R / W	1	PDE: 4MB page							
Address of page table																		Ignored				0	I g n	A	P C D	PW T	U / S	R / W	1	PDE: page table		
Ignored																										0	PDE: not present					
Address of 4KB page frame																		Ignored				G	P A T	D	A	P C D	PW T	U / S	R / W	1	PTE: 4KB page	
Ignored																										0	PTE: not present					

Figure 4-4. Formats of CR3 and Paging-Structure Entries with 32-Bit Paging