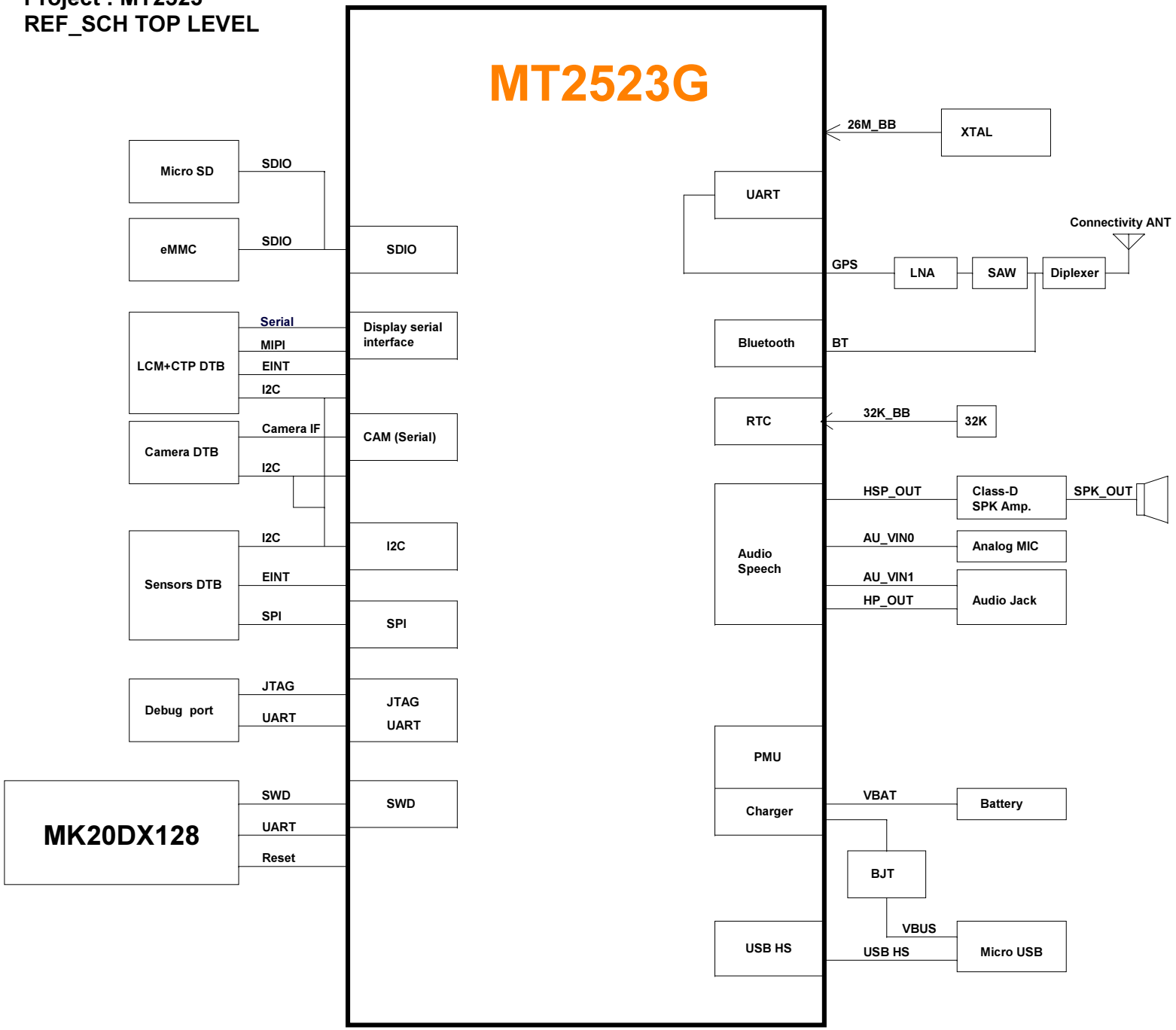
Project : MT2523
REF_SCH TOP LEVEL



MEDIATEK labs

Title: 01_Block Diagram

Size: C | MediaTek HDK MT2523G

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I2C	Function	I2C Spec.	Budgeted Timing	I2C Slave Address (7-bit mode)
I2C0	Rear Camera	400 Kbps	Yes.	Rear camera (GC0310) I2C address: 0X21 (Write:0x42, Read:0x43)
	Touch IC	400 Kbps	Yes.	TP (GT9137) I2C address: 0X24 (Write:0x28, Read:0x29)

		Vout(V)	I_max(mA)
Buck	Vcore	0.7~1.3	200
Digital LDO	Vcore	0.7~1.3	20
Analog LDO	VBT	2.8/1.8	100
	VA28	2.8	150
	VCAMA	2.8	100
	VA18	1.8	2.5
Digital LDO	VSF	1.86/3.0/3.3	100
	VIO28	2.8	150
	VIO18	1.8	200
	VUSB	3.3	80
	VMC	1.8/2.8/3/3.3	230
	VIBR	1.3/1.5/1.8/2/ 2.5/2.8/3/3.3	100
	VDIG18	1.8	5
Driver	ISINK		1X(96mA;48mA/0.25V)

Date/Time	Change list
V1.1 update 04/22	R5011 unmounted, R5010 mounted R2019 change 0 Ohm 0805 to 1K 0603 Update Note 52-18 Remove R5233 and C5228 Add note in Note 11-8 Add D2101 R2103 change to 0.1 ohm Add VCORE/VIO18/VIO28 ext LDO U2005/ U2006/ U2007 with peripheral components Remove JP101 , CN6101 Change C5009 3.6pF / GJM1555C1H3R6WB01D to 2.4pF / GJM1555C1H2R4WB01 Change L5003 6.8nH / LQG15HS6N8H02D to 5.6nH / L / 6.8 / nH / LQG15HS5N6B02D Remove CON301,C301,C302 Remove D301,D302,D303,D304,D305,C303,CON302 Change CON502 AXT510124 to AXE510124 Change to SD Slot to microSD/8P/SMD/TA-M017-012-07-811 Remove ESD4019 , ESD4018 Change Audio Jacker to JACK_CON/6P/ KRCONN J135 4501 06 01G Remove J301,J302 Remove C2017 Add U6606 Sitime 32.768KHz footprint Delete MC_RST net, add R4011 and test point TP6006

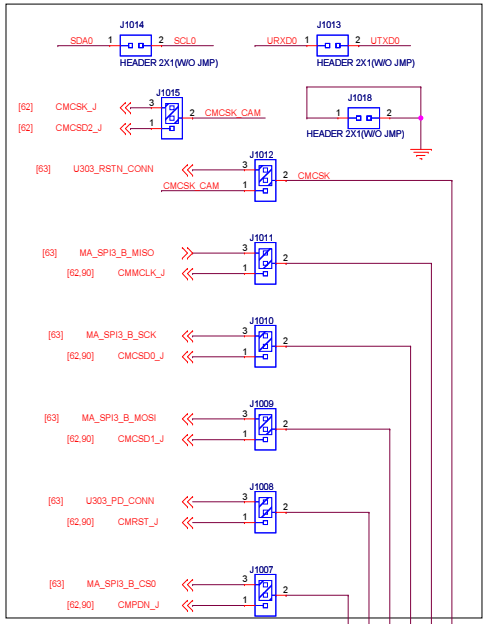
MEDIATEK labs

Title: 05_Change_Notice

Size: C | MediaTek HDK MT2523G

Date: Monday, October 24, 2016 Sheet 5 of 99

Selection of CAM and sensor DTB



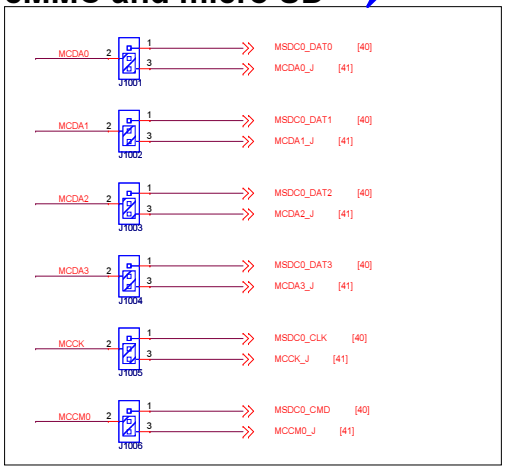
Note: 10-3

Schematic design notice of "10_BB_MT2523G_BB" page.

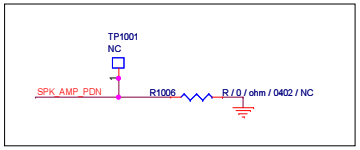
Note 10-1:	Jumper selection for microSD or eMMC; also flexible pin mux feature for user appliance.
Note 10-2:	R1004 should be closed to Larkspur ball out position
Note 10-3:	Jumper selection for Camera or sensor DTB; also flexible pin mux feature for user appliance.
Note 10-4:	Dedicate pins for GPS function are fixed; please don't change this design to other appliance.
Note 10-5:	Optional schematic for external flash

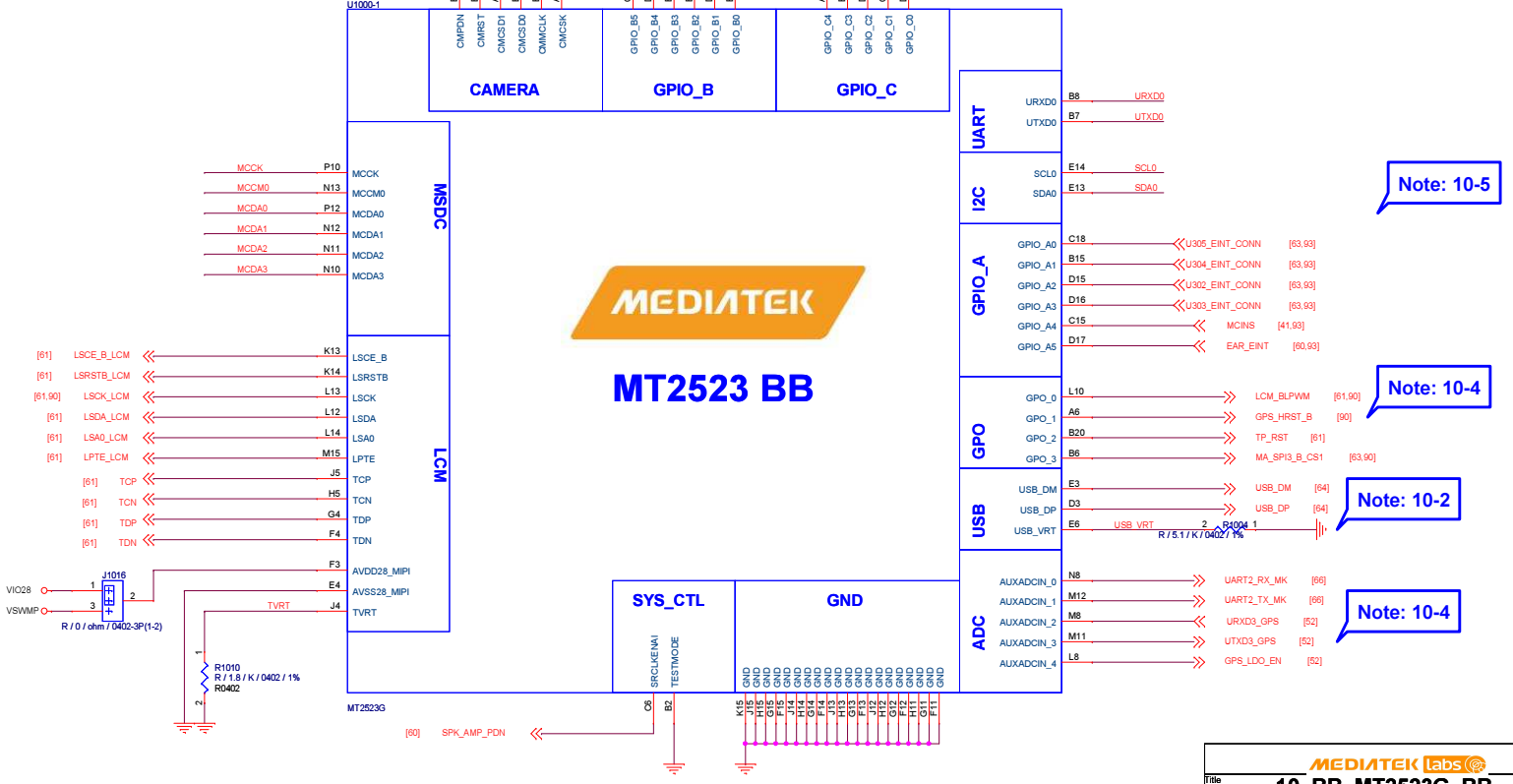
Selection of eMMC and micro SD

Note: 10-1



SYS CTL





Schematic design notice of "11_BB_MT2523G_ABB" page.

Note 11-1:	Those capacitors must be closed Larkspur ball out placement Total capacitor value at VBAT must larger than 28.4uF for DL without battery.
Note 11-2:	Selection of 32.768 KHz crystal mounted: GND: 32.768 KHz crystal is existed VRTC: 32.768 KHz crystal is not existed
Note 11-3:	This jumper could be switched for efuse function workable. Burning eFUSE case is needed: Pin FSOURCE_D connected to VEFUSE No burning eFUSE case: Pin FSOURCE_D is tied to GND .
Note 11-4:	This jumper could be switched for 32.768KHz crystal mounted VA18: 32.768KHz crystal less VIO18: 32.768KHz crystal existed
Note 11-5:	This jumper could be switched for PSRAM power saving VSWXM: Switch off power supply in suspend mode VIO18: Default setting
Note 11-6:	Users are able to adjust IO cluster power source by design; Active eMMC should unmount R1113 and mount J1111.
Note 11-7:	AVSS28_ABB ball L5 and K5 connected first, then connected to C1109 GND side by point directly which without any branch.
Note 11-8:	This test point is used for DCXO calibration C1107/C1108 mounted when 32K co-clock with GNSS function
Note 11-9:	DVDD_VIO_B should be connected to 2.8V power only

VBAT IN

System reset button

Ext. Buck for BT AVDD13

DVDD_IO power source selection

PMU LDO

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MT2523 ABB

Title	11_BB_MT2523_ABB
Size	C
	MediaTek HDK MT2523G
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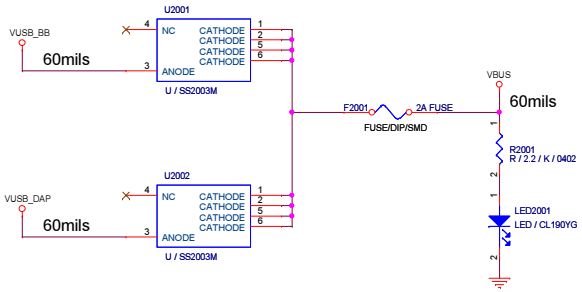
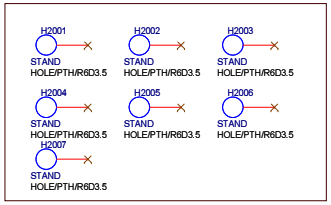
Schematic design notice of "20_POWER_COMMON_LDO" page.

Note 20-1: Users must connect CON6401 for total system power supply

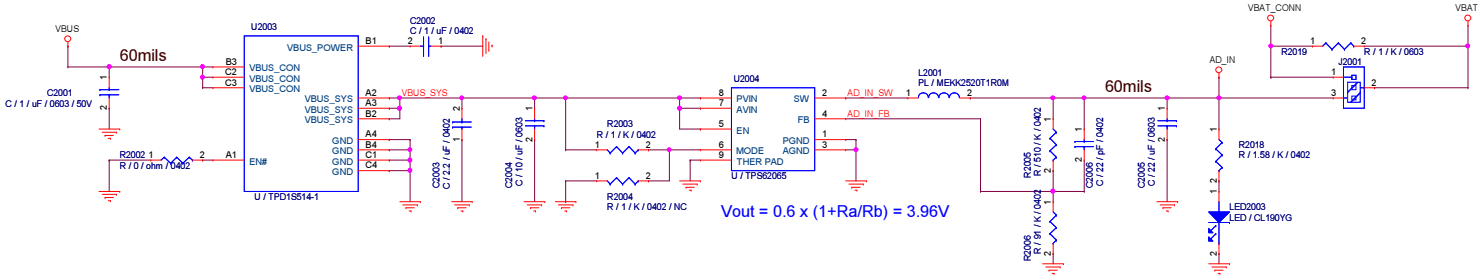
Note 20-2: External LDO are option components
Remove R1118, R1119, C1114 change to 10uF when applying external LDO



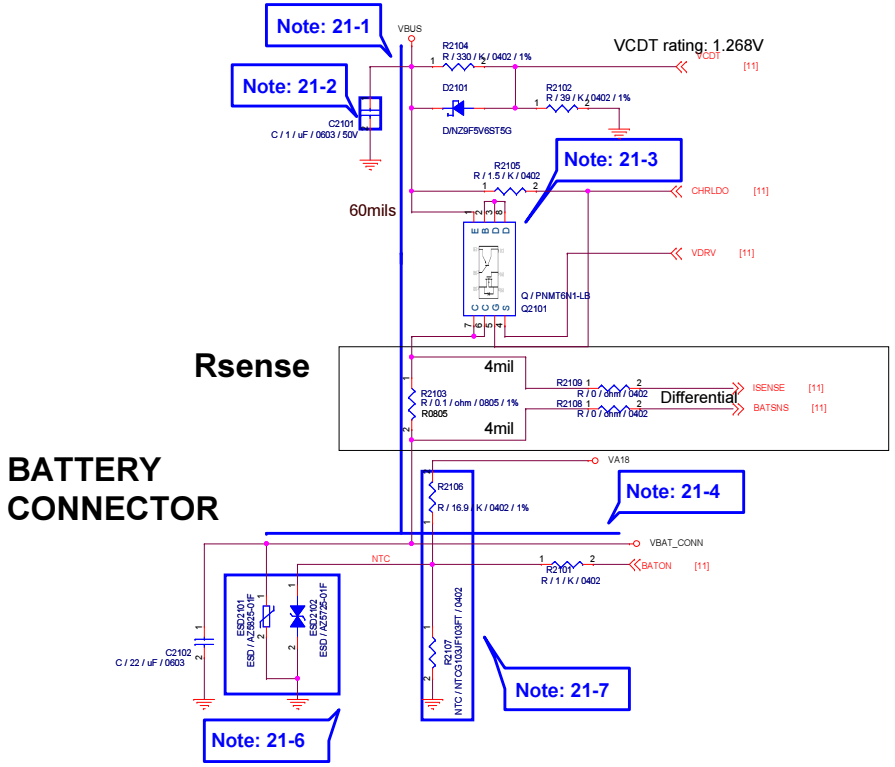
FD and Hole



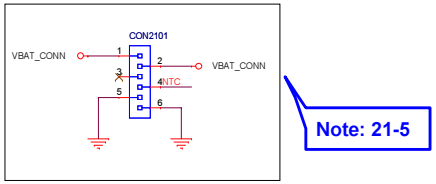
DC 5V supply



Title	20_POWER_COMMON_LDO
Size C	MediaTek HDK MT2523G
Date: Monday, October 24, 2016	Sheet 20 of 99



BATTERY DTB



Schematic design notice of "21_Power_Charging" page.

Note 21-1:	1. Close to Battery Connector. (Rsense (R2103) <10mm) 2. Main path should be 40mil. (VBUS -> U2101's E, -> U2101's C -> R2103 -> VBAT) 3. Star connection from R2103 to BAT Connector
Note 21-2:	Capacitor rating depends on Phone OVP spec.
Note 21-3:	Before you select BJT , please take power dissipation into consideration. Refer to MT6385 design notice.
Note 21-4:	60mils from battery connector to MT2523 chip
Note 21-5:	L style pin header for battery sub board plug in
Note 21-6:	Based on your system level design , if better ESD performance is needed on your system, please refer to ESD performance enhance proposal. Please place ESD2101 closed by R1137.
Note 21-7:	Thermal protection : battery with NTC (1) if battery NTC is 10kohm; R2106=16.9K (+/-1%) (2) if battery NTC is 47kohm; R2106=61.9K (+/-1%)

MEDIATEK labs

Title: 21_POWER_Charging

Size: C | MediaTek HDK MT2523G

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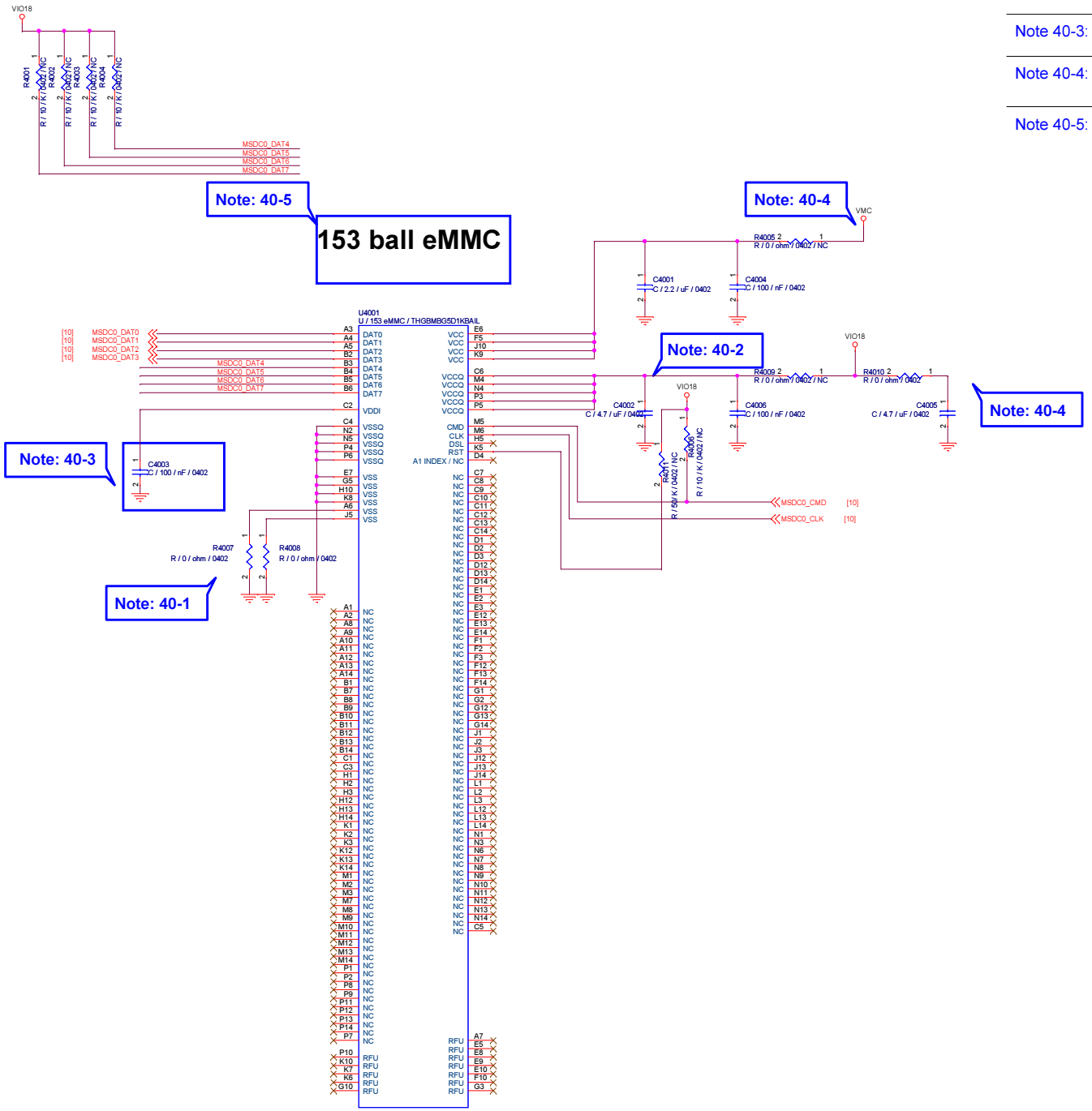
Schematic design notice of "40_MEMORY_eMMC" page.

Note 40-1:	For eMMC 5.0, connect eMMC's A6 & J5 pin to GND. For eMMC 4.5, check eMMC's A6 & J5 is no connection (NC).
Note 40-2:	Please refer eMMC datasheet for the recommendation of VCC/VCCQ/VDDI bypass capacitors values.
Note 40-3:	C4003 need to be placed near by eMMC
Note 40-4:	R4005 and R4009 must be removed when micro SD feature active R4009 and R4010 co-layout for path selection only on one time
Note 40-5:	eMMC is an optional component



MEDIATEK labs			
Title	40_Memory_eMMC		
Size C	MediaTek HDK MT2523G		
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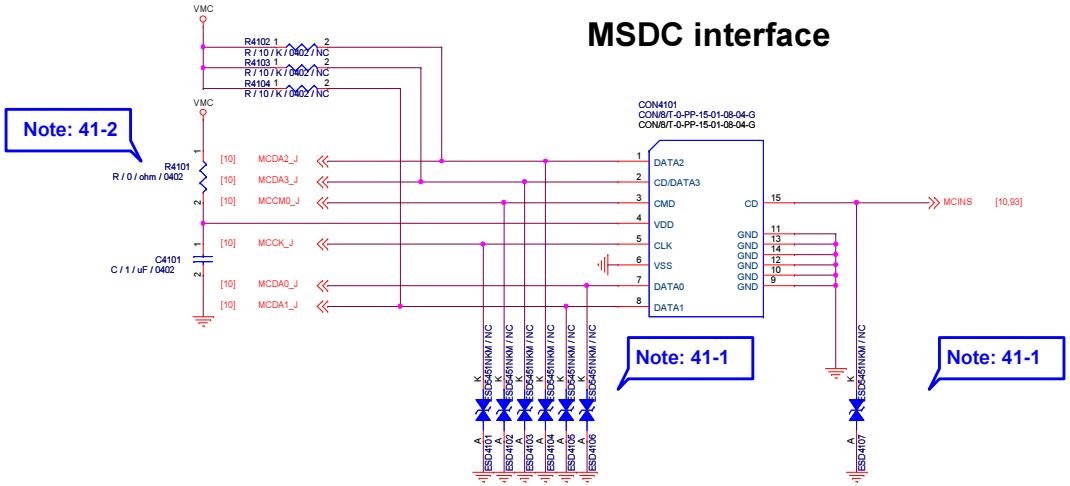
Schematic design notice of "41_MEMORY_SD Card" page.

Note 41-1:	These ESD diodes are optional for better ESD and RF de-sense performance. (The C load of Diodes on trace should be less than 15pF)
Note 41-2:	R4101 must be removed when eMMC feature active



MEDIATEK labs

Title	41_MEMORY_SD Card
Size C	MediaTek HDK MT2523G
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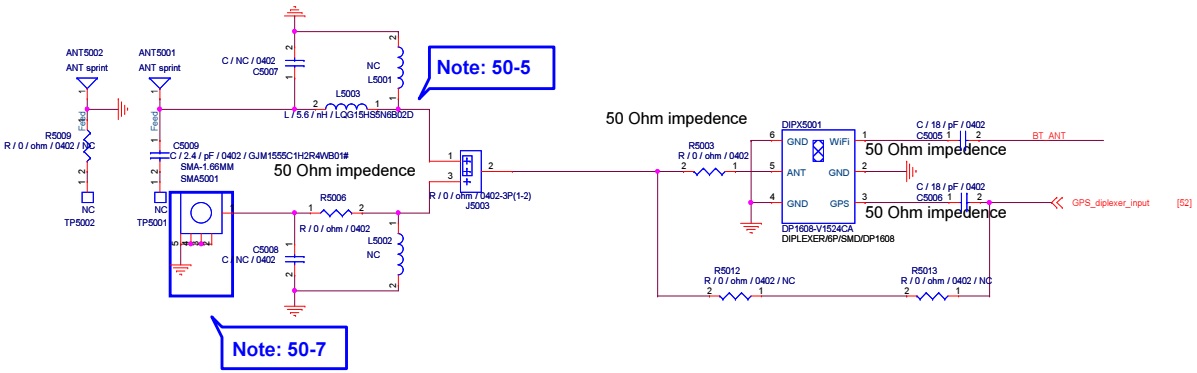
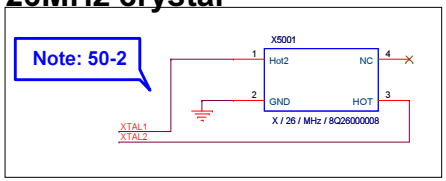
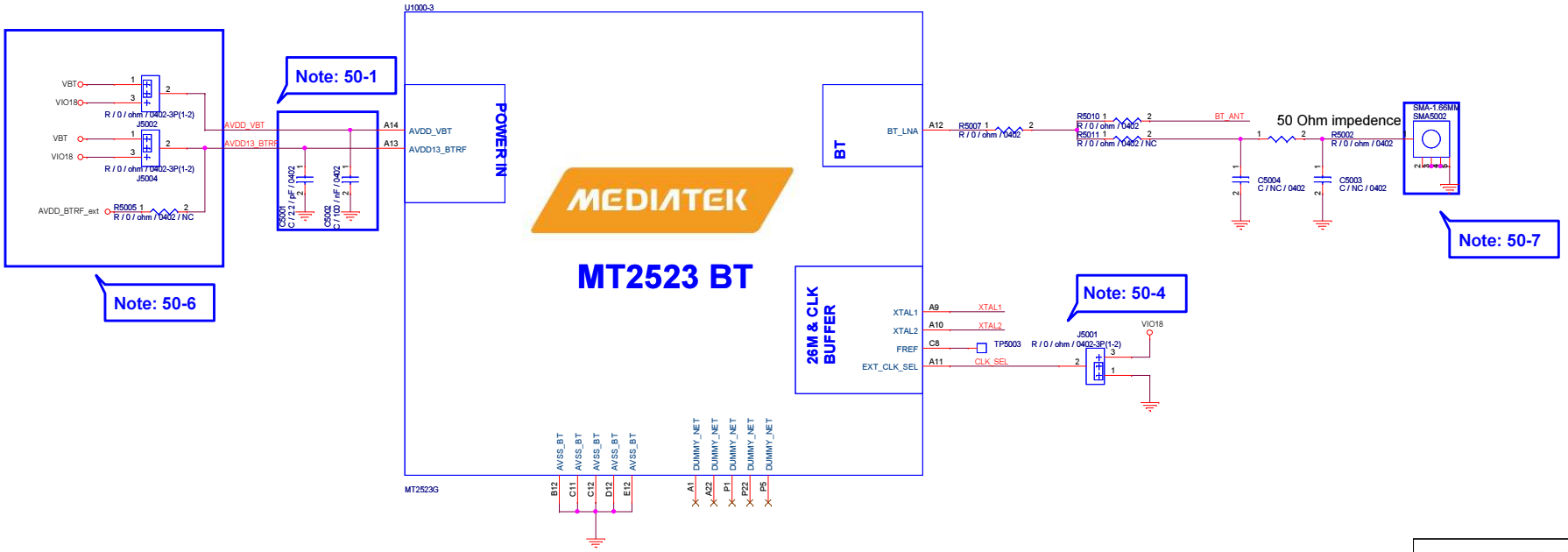


Schematic design notice of "50_CONNECTIVITY_BT_MT2523G" page.	
Note 50-1:	These capacitors should be placed near by ball out position
Note 50-2:	26MHz crystal must be placed near by Larkspur ball out position
Note 50-3:	R5002, C5003 and C5004 are reserved for BT antenna matching tuning J5006 is set for single Bluetooth performance measurement.
Note 50-4:	J5001 should keep low for clock is generated by crystal; Pull high if clock signal is injected from net XTAL1.
Note 50-5:	The impedence of traces about diplexer should be 50 ohm
Note 50-6:	J5002 connected to VBT for dual mode of Bluetooth and BLE modes J5002 connected to VIO18 for BLE mode J5004 connected to VBT for dual mode of Bluetooth and BLE modes J5004 connected to VIO18 for external buck LDO cost reduction J5005 connected to AVDD_BTRF_ext for power saving
Note 50-7:	SMA 5001 SMA5002 are optional components

26MHz crystal





MEDIATEK labs

Title: 50_CONNECTIVITY_BT_MT2523G

Size: C | MediaTek HDK MT2523G

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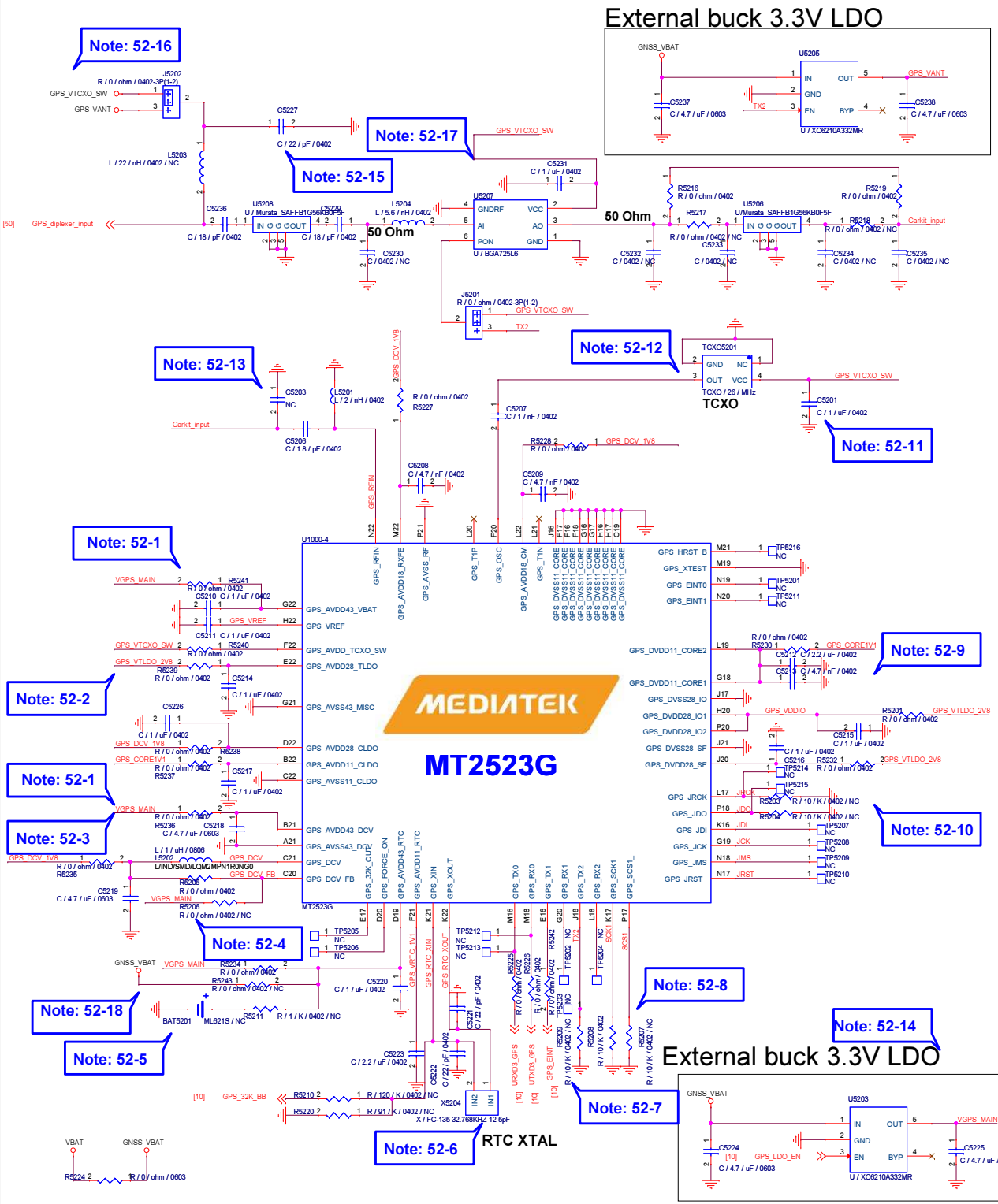

Schematic design notice of "52_CONNECTIVITY_GPS_MT2523G" page.

Note 52-1: Both of pin AVDD43_VBAT and AVDD43_DCV voltage should be keeped between 3.1V to 4.3V (VGPS_MAIN)

Note 52-2: C5214 is close to G1 ball (AVDD28_TLDO)

Note 52-3: AVSS43_DCV should be connected to C5218 GND net first, then connect to reference GND.

Note 52-4: Buck Mode : L5202 = 1uH, R5205 = 0 ohm , R5206 = NC
LDO Mode : L5202 = 0 ohm , R5205 = NC , R5206 = 0 ohm

Note 52-5: Recommend to select 3V coin battery for leakage consideration.
Pin GPS_VRTC_4V3 should be provided between 2.0V to 4.3V.
GNSS_VBAT for pin GPS_VRTC_4V3 should be provided between 2.0V to 4.3V.

Note 52-6: U5204/C5221/C5222 could be removed, R5210 = 0 ohm,
GPS_VRTC_4V3 should be kept (always alive voltage source).
Or change C5220 to 0 ohm and feed 1.1V (always alive voltage source) into GPS_VRTC_1V1.

Note 52-7: VTCXO voltage selection
2.8V TCXO: TLDO 2.8V : R5209 = NC
1.8V TCXO: SMPS 1.8V : R5209 = 10K

Note 52-8: RF clock selection
16.368MHZ TCXO : R5207 = NC , R5208 = NC
26MHZ TCXO : R5207 = NC , R5208 = 10K

Note 52-9: IO Voltage Selection
2.8V IO : R5201= 0 , R5202 = NC (IO voltage is GPS_VTLDO)
1.8V IO : R5201 = NC , R5202 = 0 (IO voltage is GPS_DCV_1V8)

Note 52-10: Host interface selection
UART : R5203 = NC , R5204 = NC (I/F : TX0 , RX0)
SPI : R5203 = NC , R5204 = 10K
I2C : R5203 = 10K , R5204 = 10K

Note 52-11: C5201 is close to U5201 VCC

Note 52-12: In order to keep good GPS clock stability,
TCXO layout please refer to MTK TCXO layout rule.
MT2523 support 16.368MHz&26MHz TCXO, please refer the QVL to select TCXO component

Note 52-13: C5203, C5206 and L5201 are reserved for LNA matching

Note 52-14: Main Input Voltage Requirement and External LDOs Selection
[1] Please choose one voltage source without built-in output high-speed discharge function and confirm the voltage drop-down curve to keep long output voltage drop-down period.
[2] Please choose external LDOs without output high-speed discharge function, such as Torex XC6210/XC6215/XC6221 series to keep long output voltage drop-down period (>1ms from 2.7V to 0.5V).
The voltage drop must can't be lower than 3.1V.

Note 52-15: matching value depends on LNA selected

Note 52-16: GPS_VTCXO_SW Note for external active antenna,
GPS_VTCXO_SW is 1.8V or 2.8V base on TCXO selection.
Please ensure external active antenna is operating at this range.
Otherwise, please using external power supply.

Note 52-17: Please refer the QVL to select LNA component

Note 52-18: GPS HOT re-start feature
No support:
BAT5201=NC, R5211=NC, R5243=NC, R5234=0ohm
X5204=NC, C5222=NC, C5221=NC, R5210=120K, R5220=91K
Support:
BAT5201=NC, R5211=NC, R5243=0ohm, R5234=NC
X5204=NC, C5222=NC, C5221=NC, R5210=120K, R5220=91K
Support and Power optimization
BAT5201=ML621S, R5211=1K, R5243=NC, R5234=0 ohm
X5204=FC-135, C5222=22pF, C5221=22pF, R5210=NC, R5220=NC

Title	52_CONNECTIVITY_GPS_MT3333
Size	C
	MediaTek HDK MT2523G
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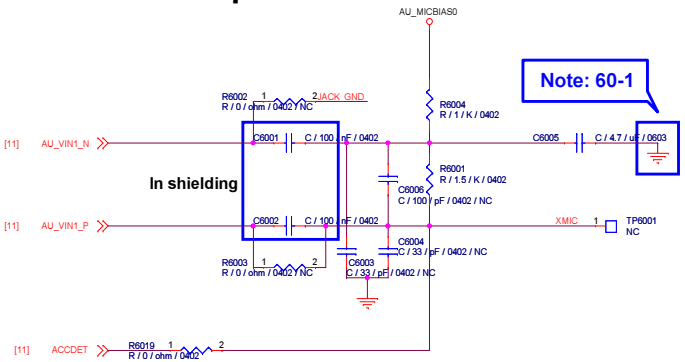
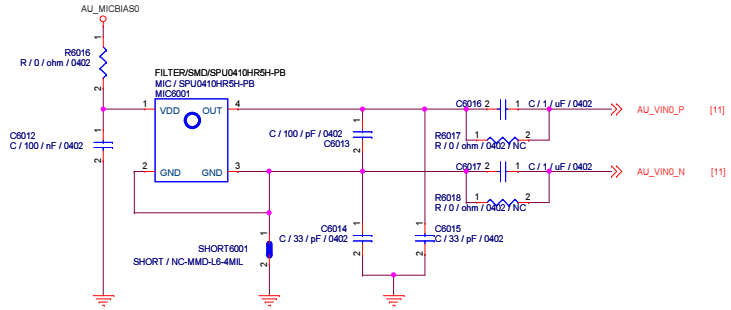
Schematic design notice of "60_PERI_Audio_IO" page.

Note 60-1:	The GND of headset microphone and Headset earphone should be connected together first, then connected to main GND.
Note 60-2:	The gain of class-D amplifier is set to 12dB (4V/V);
Note 60-3:	ESD diodes are for ehnhacement proposal; also could be cost reduction.
Note 60-4:	Speaker is an optional component

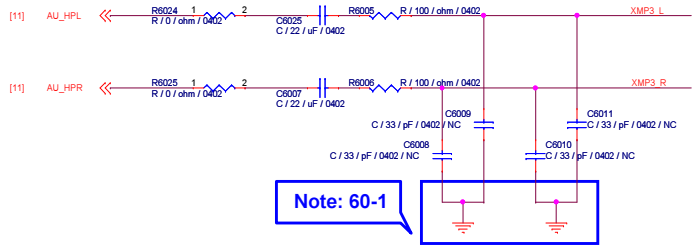
Headset microphone

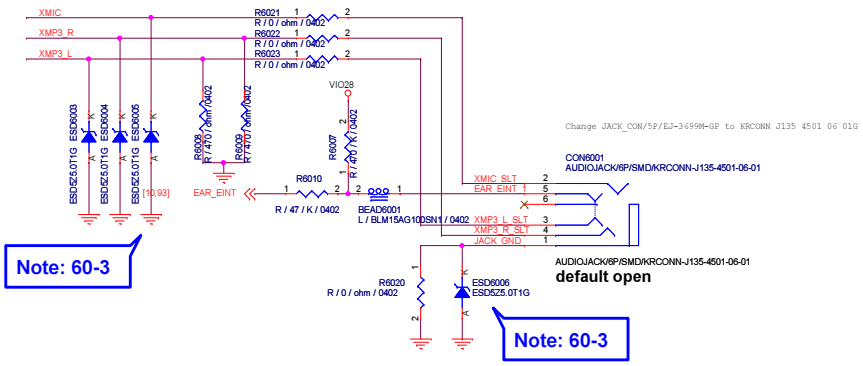


AMIC

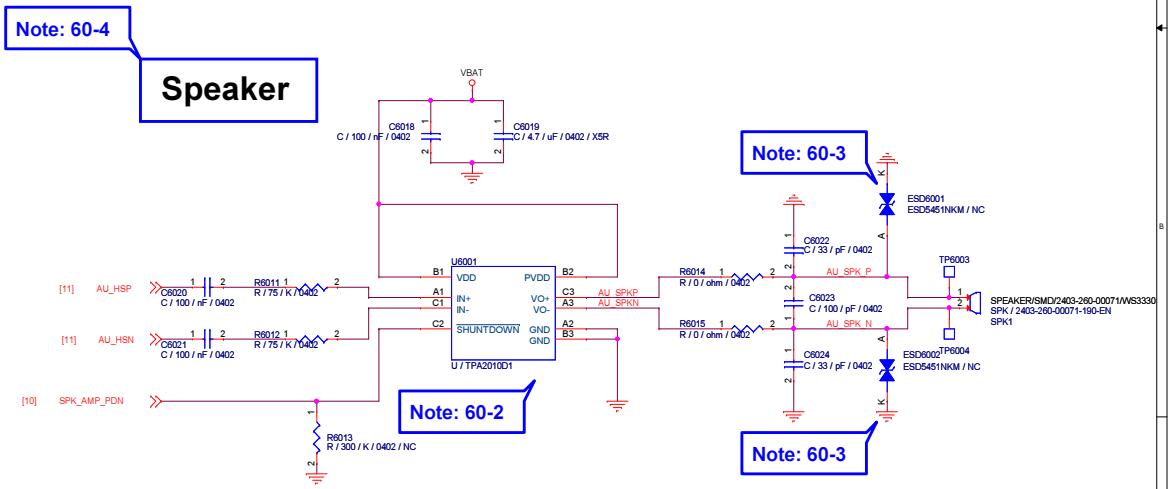


Headset earphone





Speaker



MEDIATEK labs

Title: 60_PERI_Audio_IO

Size: C | MediaTek HDK MT2523G

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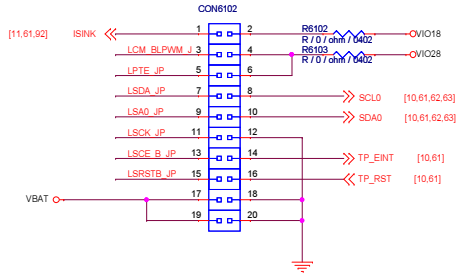
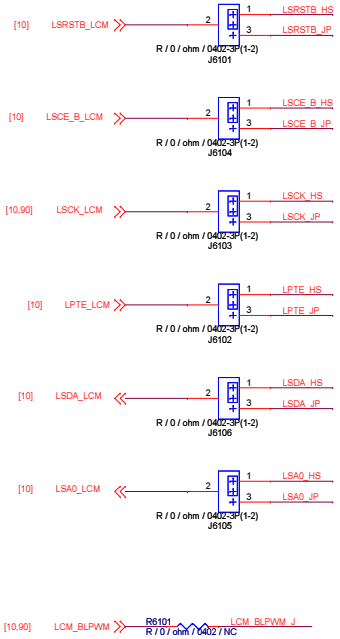
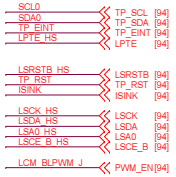
Note 61-1: High speed connector is an optional component







MEDIATEK labs

Title: 61_PERI_LCD_CTP

Size: C | MediaTek HDK MT2523G

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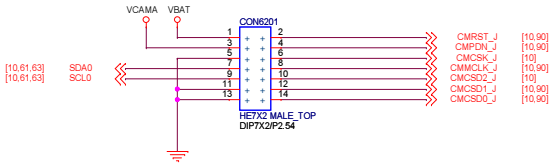

MEDIATEK labs

Title: 62_PERI_CAMERA

Size: C | MediaTek HDK MT2523G

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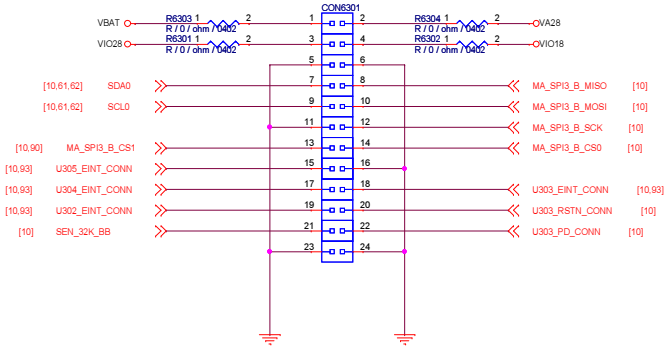


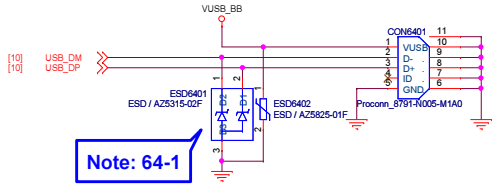
MEDIATEK labs

Title	63_PERI_SENSOR_DTB
Size C	MediaTek HDK MT2523G
Date: Monday, October 24, 2016	Sheet 63 of 99

Schematic design notice of "64_PERI_USB" page.

Note 64-1: This ESD components are optional for better ESD performance.
The C load of these diodes must smaller than 3pf and close to USB jack.

USB



Title	64_PERI_USB
Size	C
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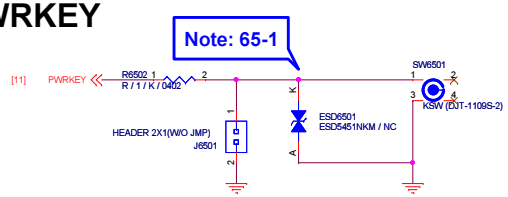
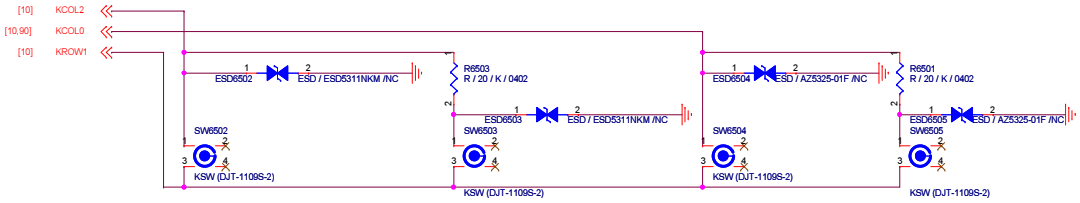
PWRKEY



KEYPAD



Schematic design notice of "65_PERI_KEY" page.

Note 65-1: This ESD diode D6501 must be closed by power button SW6301

Title	65_PERI_Key
Size C	MediaTek HDK MT2523G
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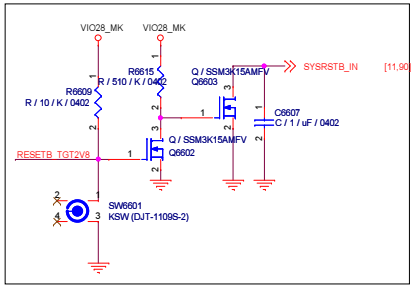
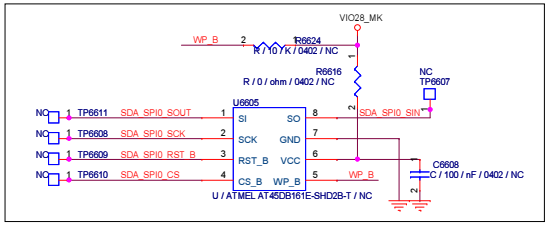
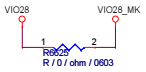
For RESETB LVS



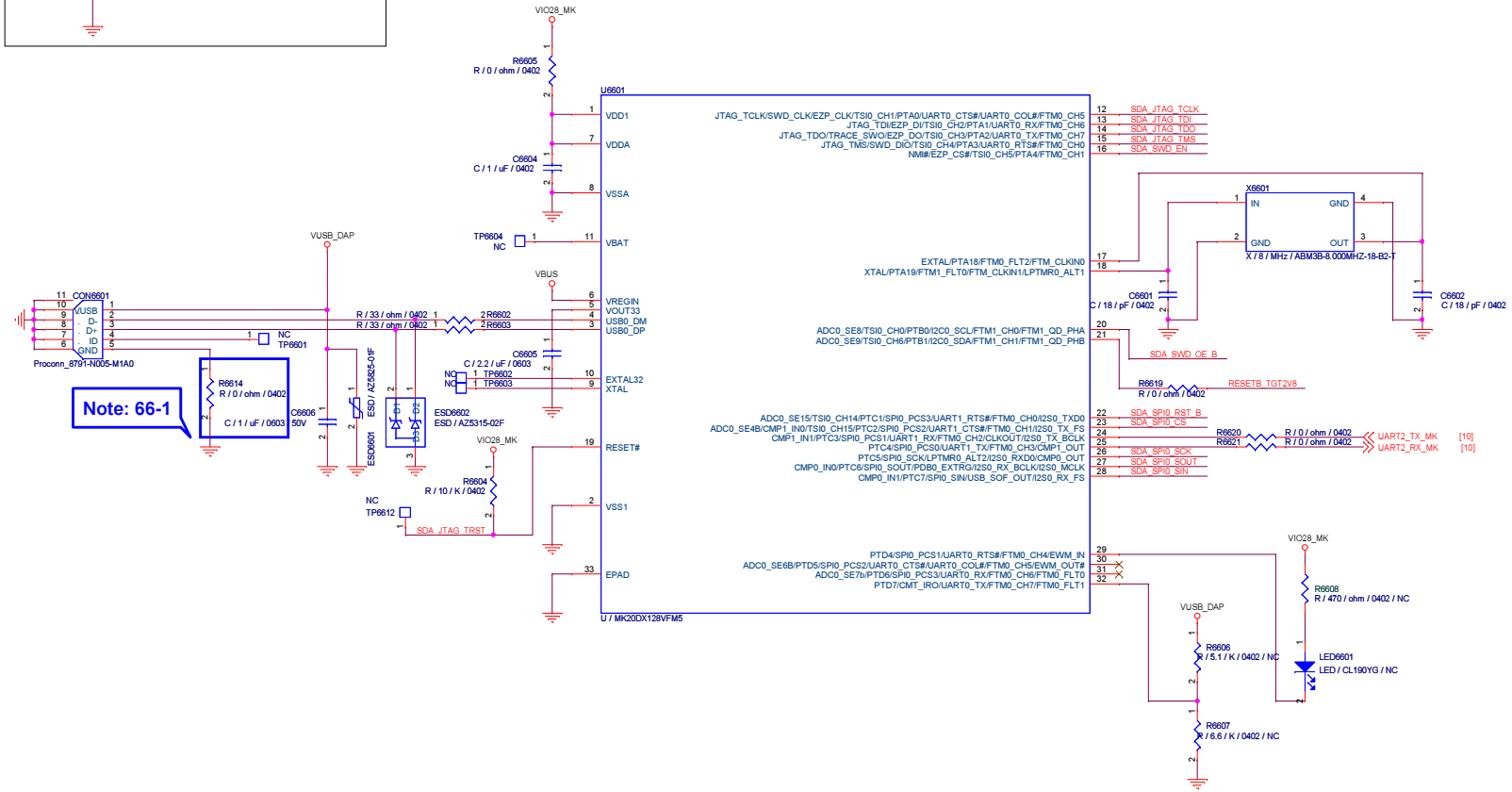
SPI FLASH MEMORY



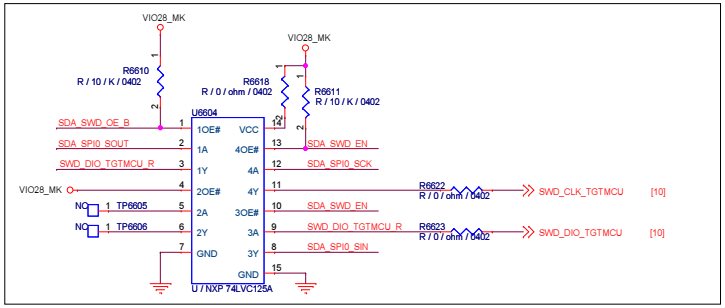


Schematic design notice of "66_PERI_SWD" page.

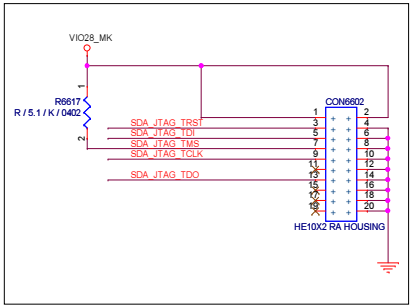
Note 66-1: Replace to bead 330ohm@100MHz 1.5A if power noise impact existed



Buffer for SWD input/output



MK20 JTAG connector



MEDIATEK labs

Title: 66_PERI_SWD

Size: C | MediaTek HDK MT2523G

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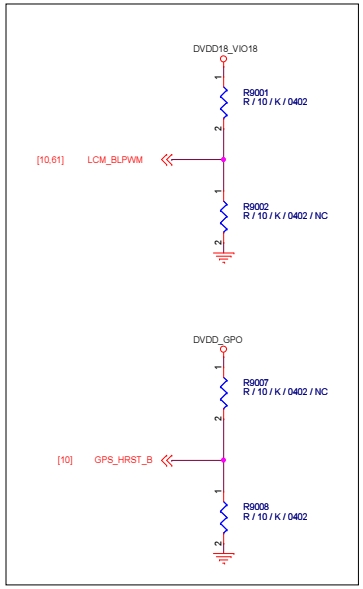
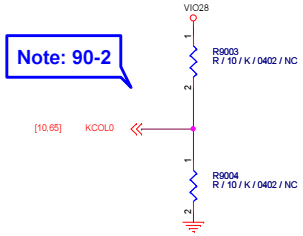
HW trap

MCU JTAG Trapping

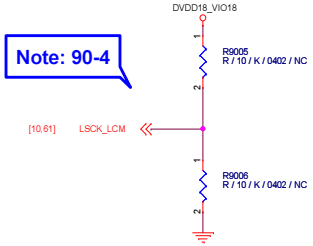
Note: 90-1



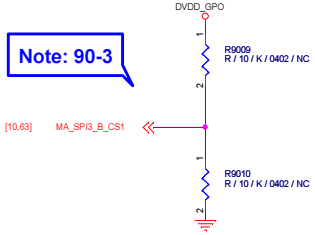
Note: 90-2

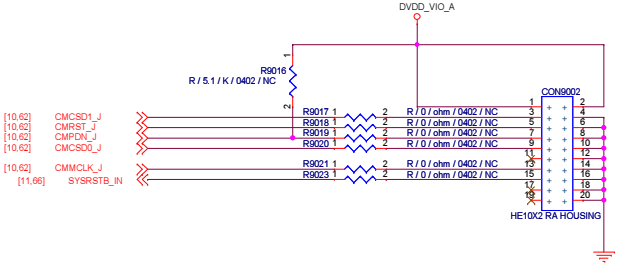


Note: 90-4



Note: 90-3





Schematic design notice of "90_Debug_IO" page.

Note 90-1:	One of JTAG trap pin, selection combination with note 90-2 The sequence is (GPS_HRST_B, LCM_BLPWM) (Low, Low): no JTAG; (Low, High): JTAG at keypad; (High, High): JTAG at CAM
Note 90-2:	Net KCOL0 is the trap pin of USB download. Keep low for image download, keep high for normal boot.
Note 90-3:	This trap pin is used to adjust serial flash voltage. Low: 1.86V, High: 3V
Note 90-4:	This trap pin is used to adjust system into system level test or not. Low: Normal mode, High: Test mode

MEDIATEK labs

Title: 90_DEBUG_IO

Size: C | MediaTek HDK MT2523G

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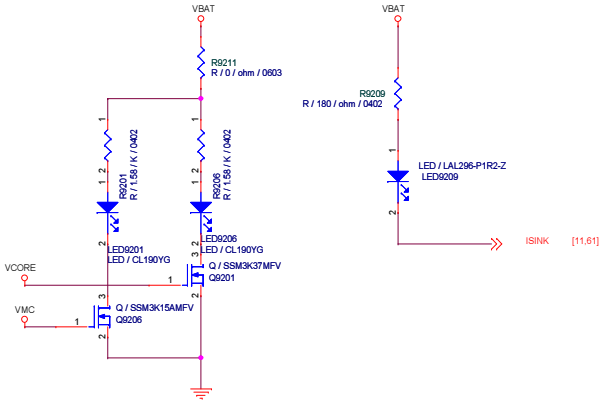
Power Indicator



MEDIATEK labs		
Title	92_POWER INDICATOR	
Size C	MediaTek HDK MT2523G	
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Title

93_Option

Size C

MediaTek HDK MT2523G

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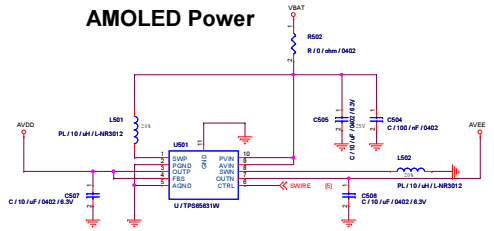
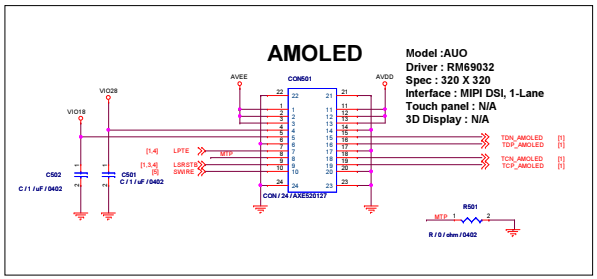
AMOLED Power

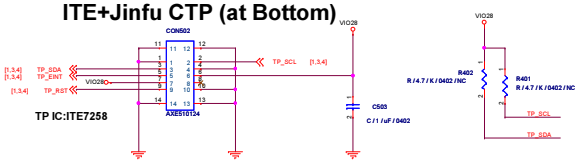


AMOLED



Model :AUO
Driver : RM69032
Spec : 320 X 320
Interface : MIPI DSI, 1-Lane
Touch panel : N/A
3D Display : N/A

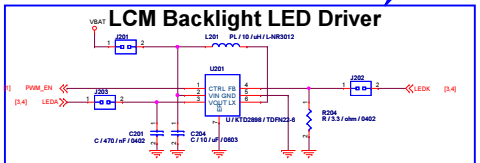
ITE+Jinfu CTP (at Bottom)



TP IC:ITE7258

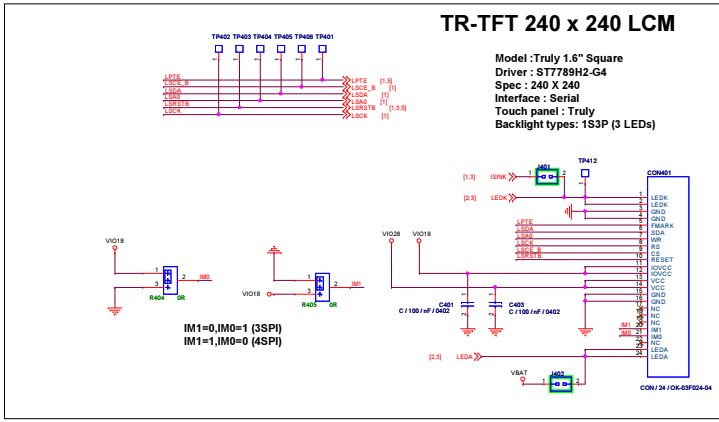
LCM Backlight LED Driver

Note: 2-1



Rset=200/Imax

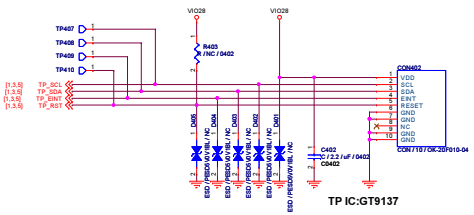
TR-TFT 240 x 240 LCM



Model :Truly 1.6" Square
Driver : ST7789H2-G4
Spec : 240 X 240
Interface : Serial
Touch panel : Truly
Backlight types: 1S3P (3 LEDs)

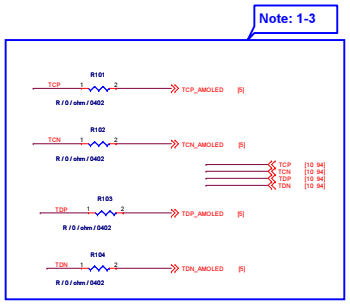
Goodix+Truly CTP (at TOP)

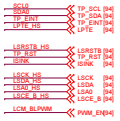
Note: 4-1



TP IC:GT9137

Note: 1-3





Schematic design notice of "01_CONNECTOR" page.

Note 1-1: 1. For MTK Internal development and verification.(EVB:WS3308)
2. CON101,CON102 can support display MIPI and Serial I/F at the same time.

Note 1-2: JP101 only support serial LCM I/F.

Note 1-3: R101,R102,R103,R104 is for selecting TR-TFT LCM or AMOLED.

MEDIATEK

File	94_MIPI_AMOLED_CTP
Size	B
	MTK Confidential
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