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ECEGR 2220

Lab 6

Our microprocessor was built using 5 primary stages. They are the program counter, the register bank, the control system, the ALU, and the memory. In lab 6, our primary goal was to implement the program counter, the control system, and connect all of the components together, including the provided instruction memory. Lab 6 used two files to accomplish this. The first was the ProcElements file which had some MUXs, the control logic, and the program counter. The second was the Processor file itself, which housed all of the primary port mapping for the final project.

The biggest hurdle in the ProcElements file was correctly implementing all of the control logic. To tackle this issue, we systematically went through the control architecture’s outputs, one by one, and deduced the correct outputs for each given opcode and funct the control could receive. After creating the control, the muxes were very simple, and the program counter was also not a problem.

The Processor file is what brought all of our pieces together to build the actual unit. This required a high volume of signals of varying sizes, which functioned as all of the internal connections between our various components. Keeping these signals straight was at first a bit of a struggle, but in the end we wired them all correctly. The final validation of our design was seen in the simulation wave, and we observed that s7 ended storing the value 4, and the memory ended storing the correct pattern. We know these were the correct results because we were able to compare them to the values ending in these locations in QtSpim. That is what the instruction memory was doing, it was looping through values and building a pattern in memory.

Truth Tables

RegSrc:

Input (opcode and funct)	Output
000000 and 000000	1
000000 and 000010	1
Others	0

RegDst:

Input (opcode)	Output
001000	0
001101	0
100011	0
Others	1

Branch:

Input (opcode)	Output
000100	00
000101	01
Others	10

MemtoReg:

Input (opcode)	Output
100011	0
Others	1

ALUOp:

Input (opcode and funct)	Output
000000 and 100000	00000
000000 and 100010	00001
000000 and 100100	00100
000000 and 100101	01000
000000 and 000010	10000
000000 and 000000	10001
001000 and XXXXXX	00010
001101 and XXXXXX	01001
101011 and XXXXXX	00010
100011 and XXXXXX	00010
000100 and XXXXXX	00001
000101 and XXXXXX	00001
Others	ZZZZZ

MemWrite:

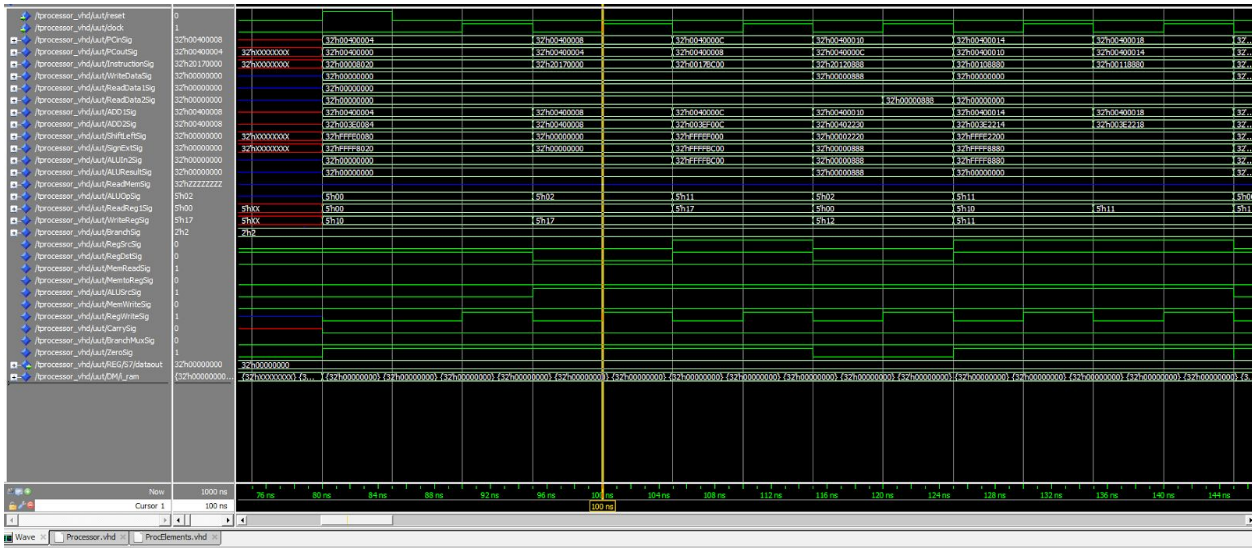
Input (opcode)	Output
101011	1
Others	0

ALUSrc:

Input (opcode AND funct)	Output
001000 and XXXXXX	1
001101 and XXXXXX	1
100011 and XXXXXX	1
101011 and XXXXXX	1
000000 and 000000	1
000000 and 000010	1
Others	0

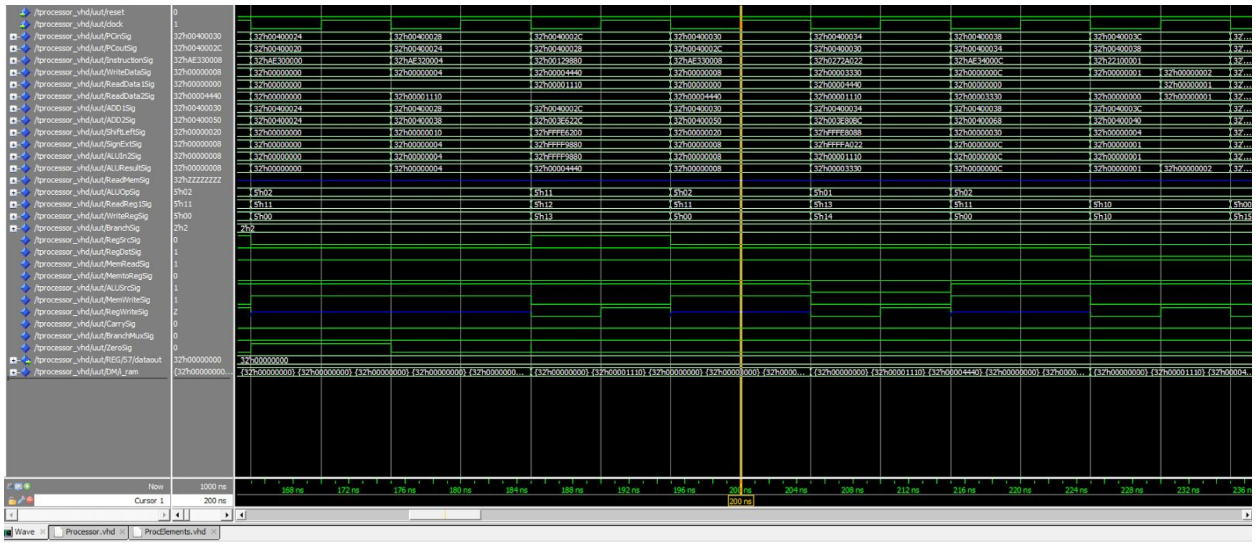
RegWrite:

Input (opcode)	Output
000000	clk
001000	clk
001101	clk
100011	clk
Others	Z



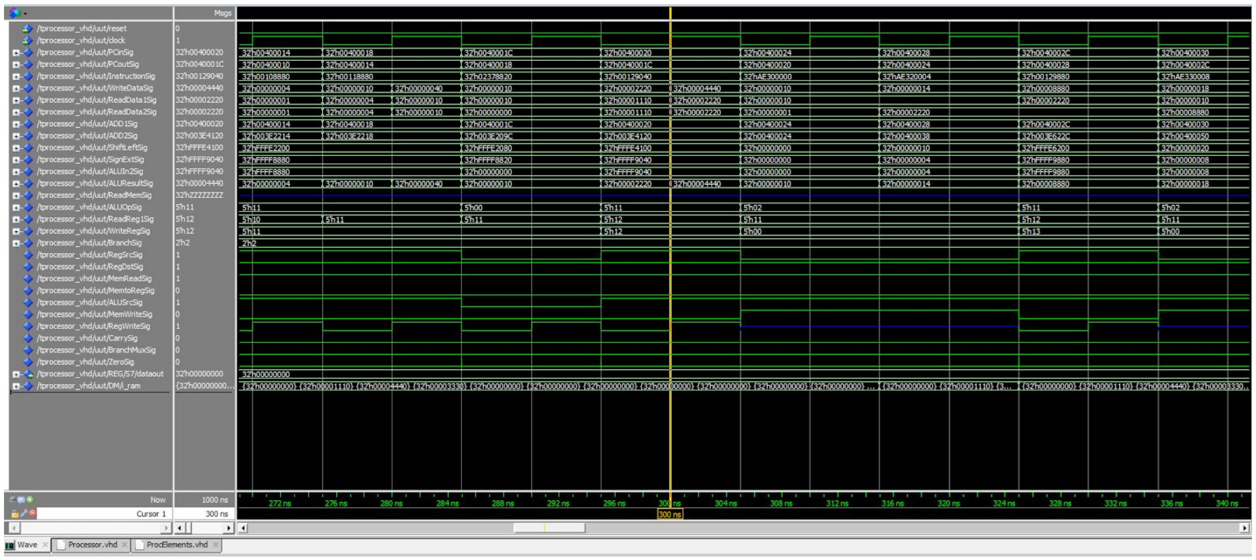
```
/tprocessor_vhd/uut/reset             0
/tprocessor_vhd/uut/clock             1
/tprocessor_vhd/uut/PCinSig           32'h00400008
/tprocessor_vhd/uut/PCoutSig          32'h00400004
/tprocessor_vhd/uut/InstructionSig    32'h20170000
/tprocessor_vhd/uut/WriteDataSig      32'h00000000
/tprocessor_vhd/uut/ReadData1Sig      32'h00000000
/tprocessor_vhd/uut/ReadData2Sig      32'h00000000
/tprocessor_vhd/uut/ADD1Sig           32'h00400008
/tprocessor_vhd/uut/ADD2Sig           32'h00400008
/tprocessor_vhd/uut/ShiftLeftSig      32'h00000000
/tprocessor_vhd/uut/SignExtSig        32'h00000000
/tprocessor_vhd/uut/ALUIn2Sig         32'h00000000
/tprocessor_vhd/uut/ALUResultSig      32'h00000000
/tprocessor_vhd/uut/ReadMemSig        32'hZZZZZZZZ
/tprocessor_vhd/uut/ALUOpSig          5'h02
/tprocessor_vhd/uut/ReadReg1Sig       5'h00
/tprocessor_vhd/uut/WriteRegSig       5'h17
/tprocessor_vhd/uut/BranchSig         2'h2
/tprocessor_vhd/uut/RegSrcSig         0
/tprocessor_vhd/uut/RegDstSig         0
/tprocessor_vhd/uut/MemReadSig        1
/tprocessor_vhd/uut/MemtoRegSig       0
/tprocessor_vhd/uut/ALUSrcSig         1
/tprocessor_vhd/uut/MemWriteSig       0
/tprocessor_vhd/uut/RegWriteSig       1
/tprocessor_vhd/uut/CarrySig          0
/tprocessor_vhd/uut/BranchMuxSig      0
/tprocessor_vhd/uut/ZeroSig           1
/tprocessor_vhd/uut/REG/S7/dataout    32'h00000000
/tprocessor_vhd/uut/DM/i_ram          {32'h00000000...
Now        1000 ns
Cursor 1   100 ns
```

100 ns

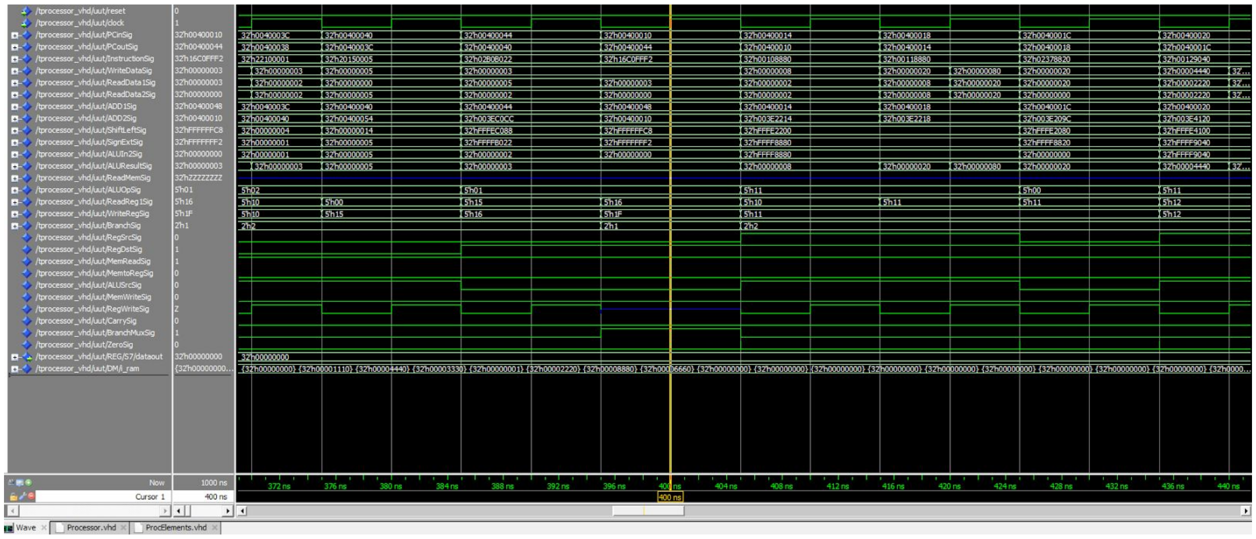


```
/tprocessor_vhd/uut/reset             0
/tprocessor_vhd/uut/clock             1
/tprocessor_vhd/uut/PCinSig           32'h00400030
/tprocessor_vhd/uut/PCoutSig          32'h0040002C
/tprocessor_vhd/uut/InstructionSig    32'hAE330008
/tprocessor_vhd/uut/WriteDataSig      32'h00000008
/tprocessor_vhd/uut/ReadData1Sig      32'h00000000
/tprocessor_vhd/uut/ReadData2Sig      32'h00004440
/tprocessor_vhd/uut/ADD1Sig           32'h00400030
/tprocessor_vhd/uut/ADD2Sig           32'h00400050
/tprocessor_vhd/uut/ShiftLeftSig      32'h00000020
/tprocessor_vhd/uut/SignExtSig        32'h00000008
/tprocessor_vhd/uut/ALUIn2Sig         32'h00000008
/tprocessor_vhd/uut/ALUResultSig      32'h00000008
/tprocessor_vhd/uut/ReadMemSig        32'hZZZZZZZZ
/tprocessor_vhd/uut/ALUOpSig          5'h02
/tprocessor_vhd/uut/ReadReg1Sig       5'h11
/tprocessor_vhd/uut/WriteRegSig       5'h00
/tprocessor_vhd/uut/BranchSig         2'h2
/tprocessor_vhd/uut/RegSrcSig         0
/tprocessor_vhd/uut/RegDstSig         1
/tprocessor_vhd/uut/MemReadSig        1
/tprocessor_vhd/uut/MemtoRegSig       0
/tprocessor_vhd/uut/ALUSrcSig         1
/tprocessor_vhd/uut/MemWriteSig       1
/tprocessor_vhd/uut/RegWriteSig       Z
/tprocessor_vhd/uut/CarrySig          0
/tprocessor_vhd/uut/BranchMuxSig      0
/tprocessor_vhd/uut/ZeroSig           0
/tprocessor_vhd/uut/REG/S7/dataout    32'h00000000
/tprocessor_vhd/uut/DM/i_ram          {32'h00000000...
Now        1000 ns
Cursor 1   200 ns
```

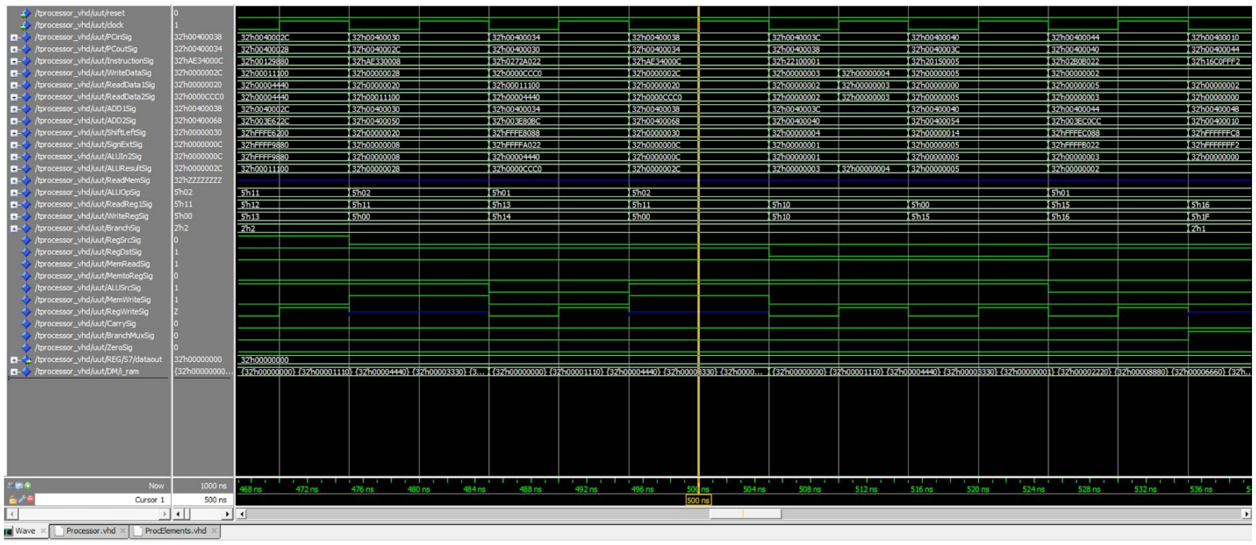
200 ns


```
                                      Msgs
/tprocessor_vhd/uut/reset             0
/tprocessor_vhd/uut/clock             1
/tprocessor_vhd/uut/PCinSig           32'h00400020
/tprocessor_vhd/uut/PCoutSig          32'h0040001C
/tprocessor_vhd/uut/InstructionSig    32'h00129040
/tprocessor_vhd/uut/WriteDataSig      32'h00004440
/tprocessor_vhd/uut/ReadData1Sig      32'h00002220
/tprocessor_vhd/uut/ReadData2Sig      32'h00002220
/tprocessor_vhd/uut/ADD1Sig           32'h00400020
/tprocessor_vhd/uut/ADD2Sig           32'h003E4120
/tprocessor_vhd/uut/ShiftLeftSig      32'hFFFE4100
/tprocessor_vhd/uut/SignExtSig        32'hFFFF9040
/tprocessor_vhd/uut/ALUIn2Sig         32'hFFFF9040
/tprocessor_vhd/uut/ALUResultSig      32'h00004440
/tprocessor_vhd/uut/ReadMemSig        32'hZZZZZZZZ
/tprocessor_vhd/uut/ALUOpSig          5'h11
/tprocessor_vhd/uut/ReadReg1Sig       5'h12
/tprocessor_vhd/uut/WriteRegSig       5'h12
/tprocessor_vhd/uut/BranchSig         2'h2
/tprocessor_vhd/uut/RegSrcSig         1
/tprocessor_vhd/uut/RegDstSig         1
/tprocessor_vhd/uut/MemReadSig        1
/tprocessor_vhd/uut/MemtoRegSig       0
/tprocessor_vhd/uut/ALUSrcSig         1
/tprocessor_vhd/uut/MemWriteSig       0
/tprocessor_vhd/uut/RegWriteSig       1
/tprocessor_vhd/uut/CarrySig          0
/tprocessor_vhd/uut/BranchMuxSig      0
/tprocessor_vhd/uut/ZeroSig           0
/tprocessor_vhd/uut/REG/S7/dataout    32'h00000000
/tprocessor_vhd/uut/DM/i_ram          {32'h00000000...
Now                                   1000 ns
Cursor 1                              300 ns
```

300 ns

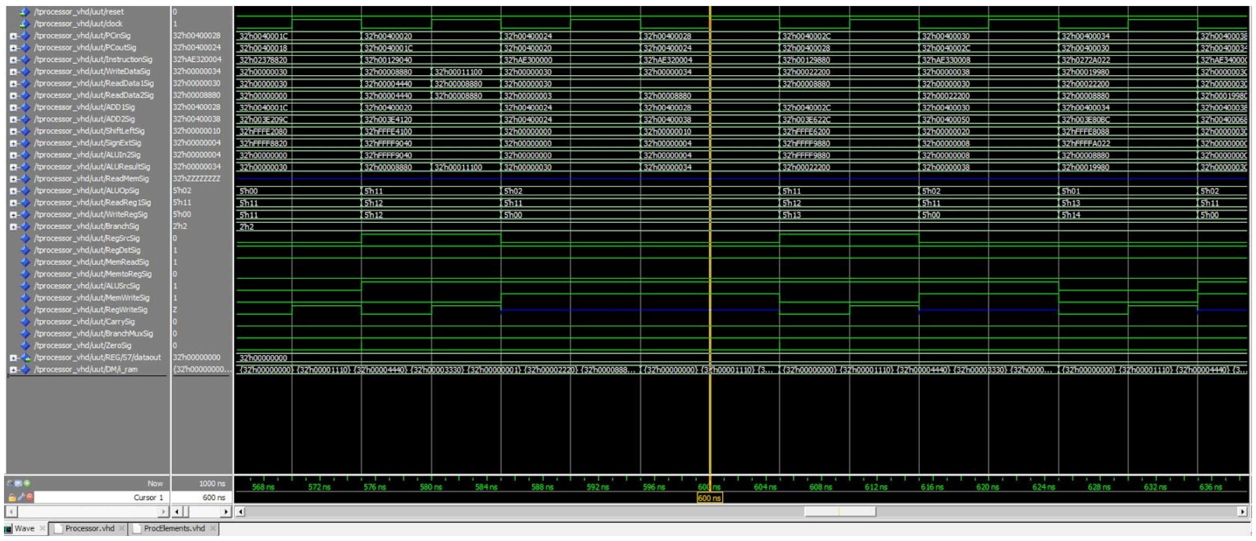

```
/tprocessor_vhd/uut/reset             0
/tprocessor_vhd/uut/clock             1
/tprocessor_vhd/uut/PCinSig           32'h00400010
/tprocessor_vhd/uut/PCoutSig          32'h00400044
/tprocessor_vhd/uut/InstructionSig    32'h16C0FFF2
/tprocessor_vhd/uut/WriteDataSig      32'h00000003
/tprocessor_vhd/uut/ReadData1Sig      32'h00000003
/tprocessor_vhd/uut/ReadData2Sig      32'h00000000
/tprocessor_vhd/uut/ADD1Sig           32'h00400048
/tprocessor_vhd/uut/ADD2Sig           32'h00400010
/tprocessor_vhd/uut/ShiftLeftSig      32'hFFFFFFC8
/tprocessor_vhd/uut/SignExtSig        32'hFFFFFFF2
/tprocessor_vhd/uut/ALUIn2Sig         32'h00000000
/tprocessor_vhd/uut/ALUResultSig      32'h00000003
/tprocessor_vhd/uut/ReadMemSig        32'hZZZZZZZZ
/tprocessor_vhd/uut/ALUOpSig          5'h01
/tprocessor_vhd/uut/ReadReg1Sig       5'h16
/tprocessor_vhd/uut/WriteRegSig       5'h1F
/tprocessor_vhd/uut/BranchSig         2'h1
/tprocessor_vhd/uut/RegSrcSig         0
/tprocessor_vhd/uut/RegDstSig         1
/tprocessor_vhd/uut/MemReadSig        1
/tprocessor_vhd/uut/MemtoRegSig       0
/tprocessor_vhd/uut/ALUSrcSig         0
/tprocessor_vhd/uut/MemWriteSig       0
/tprocessor_vhd/uut/RegWriteSig       Z
/tprocessor_vhd/uut/CarrySig          0
/tprocessor_vhd/uut/BranchMuxSig      1
/tprocessor_vhd/uut/ZeroSig           0
/tprocessor_vhd/uut/REG/S7/dataout    32'h00000000
/tprocessor_vhd/uut/DM/i_ram          {32'h00000000...
Now                                   1000 ns
Cursor 1                              400 ns
```

400 ns



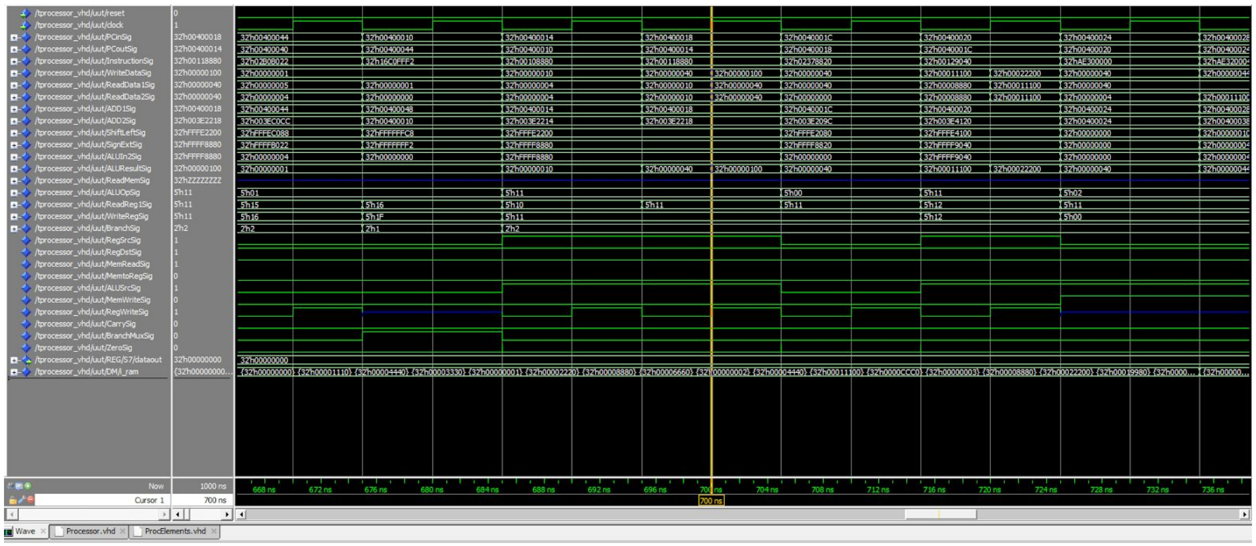
```
/tprocessor_vhd/uut/reset             0
/tprocessor_vhd/uut/clock             1
/tprocessor_vhd/uut/PCinSig           32'h00400038
/tprocessor_vhd/uut/PCoutSig          32'h00400034
/tprocessor_vhd/uut/InstructionSig    32'hAE34000C
/tprocessor_vhd/uut/WriteDataSig      32'h0000002C
/tprocessor_vhd/uut/ReadData1Sig      32'h00000020
/tprocessor_vhd/uut/ReadData2Sig      32'h0000CCC0
/tprocessor_vhd/uut/ADD1Sig           32'h00400038
/tprocessor_vhd/uut/ADD2Sig           32'h00400068
/tprocessor_vhd/uut/ShiftLeftSig      32'h00000030
/tprocessor_vhd/uut/SignExtSig        32'h0000000C
/tprocessor_vhd/uut/ALUIn2Sig         32'h0000000C
/tprocessor_vhd/uut/ALUResultSig      32'h0000002C
/tprocessor_vhd/uut/ReadMemSig        32'hZZZZZZZZ
/tprocessor_vhd/uut/ALUOpSig          5'h02
/tprocessor_vhd/uut/ReadReg1Sig       5'h11
/tprocessor_vhd/uut/WriteRegSig       5'h00
/tprocessor_vhd/uut/BranchSig         2'h2
/tprocessor_vhd/uut/RegSrcSig         0
/tprocessor_vhd/uut/RegDstSig         1
/tprocessor_vhd/uut/MemReadSig        1
/tprocessor_vhd/uut/MemtoRegSig       0
/tprocessor_vhd/uut/ALUSrcSig         1
/tprocessor_vhd/uut/MemWriteSig       1
/tprocessor_vhd/uut/RegWriteSig       Z
/tprocessor_vhd/uut/CarrySig          0
/tprocessor_vhd/uut/BranchMuxSig      0
/tprocessor_vhd/uut/ZeroSig           0
/tprocessor_vhd/uut/REG/S7/dataout    32'h00000000
/tprocessor_vhd/uut/DM/i_ram          {32'h00000000...
Now                                   1000 ns
Cursor 1                              500 ns
```

500 ns



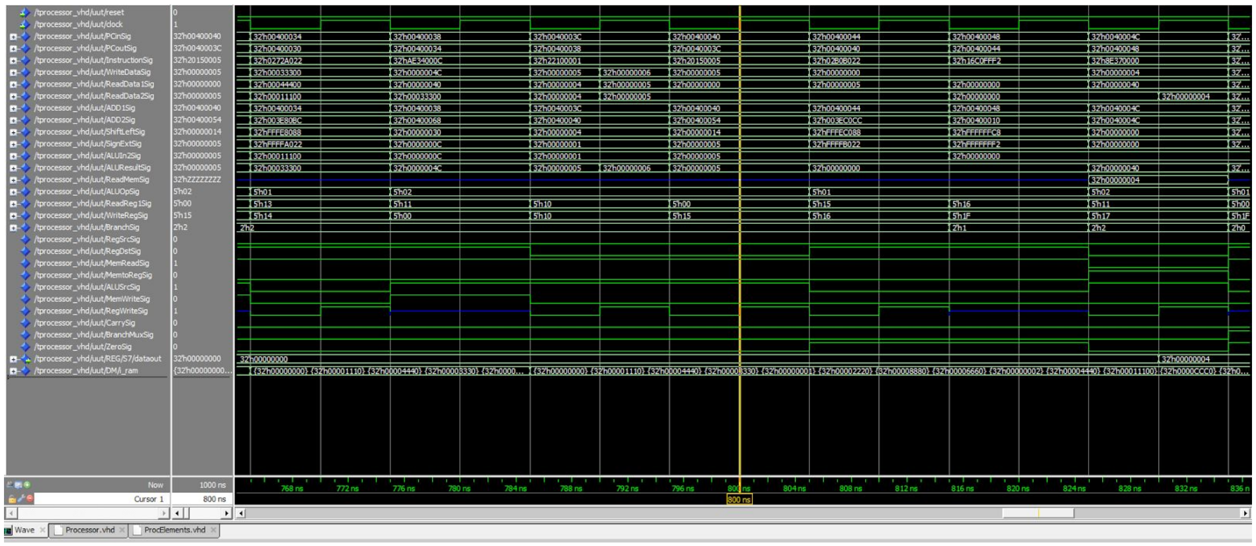
```
/tprocessor_vhd/uut/reset             0
/tprocessor_vhd/uut/clock             1
/tprocessor_vhd/uut/PCinSig           32'h00400028
/tprocessor_vhd/uut/PCoutSig          32'h00400024
/tprocessor_vhd/uut/InstructionSig    32'hAE320004
/tprocessor_vhd/uut/WriteDataSig      32'h00000034
/tprocessor_vhd/uut/ReadData1Sig      32'h00000030
/tprocessor_vhd/uut/ReadData2Sig      32'h00008880
/tprocessor_vhd/uut/ADD1Sig           32'h00400028
/tprocessor_vhd/uut/ADD2Sig           32'h00400038
/tprocessor_vhd/uut/ShiftLeftSig      32'h00000010
/tprocessor_vhd/uut/SignExtSig        32'h00000004
/tprocessor_vhd/uut/ALUIn2Sig         32'h00000004
/tprocessor_vhd/uut/ALUResultSig      32'h00000034
/tprocessor_vhd/uut/ReadMemSig        32'hZZZZZZZZ
/tprocessor_vhd/uut/ALUOpSig          5'h02
/tprocessor_vhd/uut/ReadReg1Sig       5'h11
/tprocessor_vhd/uut/WriteRegSig       5'h00
/tprocessor_vhd/uut/BranchSig         2'h2
/tprocessor_vhd/uut/RegSrcSig         0
/tprocessor_vhd/uut/RegDstSig         1
/tprocessor_vhd/uut/MemReadSig        1
/tprocessor_vhd/uut/MemtoRegSig       0
/tprocessor_vhd/uut/ALUSrcSig         1
/tprocessor_vhd/uut/MemWriteSig       1
/tprocessor_vhd/uut/RegWriteSig       Z
/tprocessor_vhd/uut/CarrySig          0
/tprocessor_vhd/uut/BranchMuxSig      0
/tprocessor_vhd/uut/ZeroSig           0
/tprocessor_vhd/uut/REG/S7/dataout    32'h00000000
/tprocessor_vhd/uut/DM/i_ram          {32'h00000000...
Now                                   1000 ns
Cursor 1                              600 ns
```

600 ns



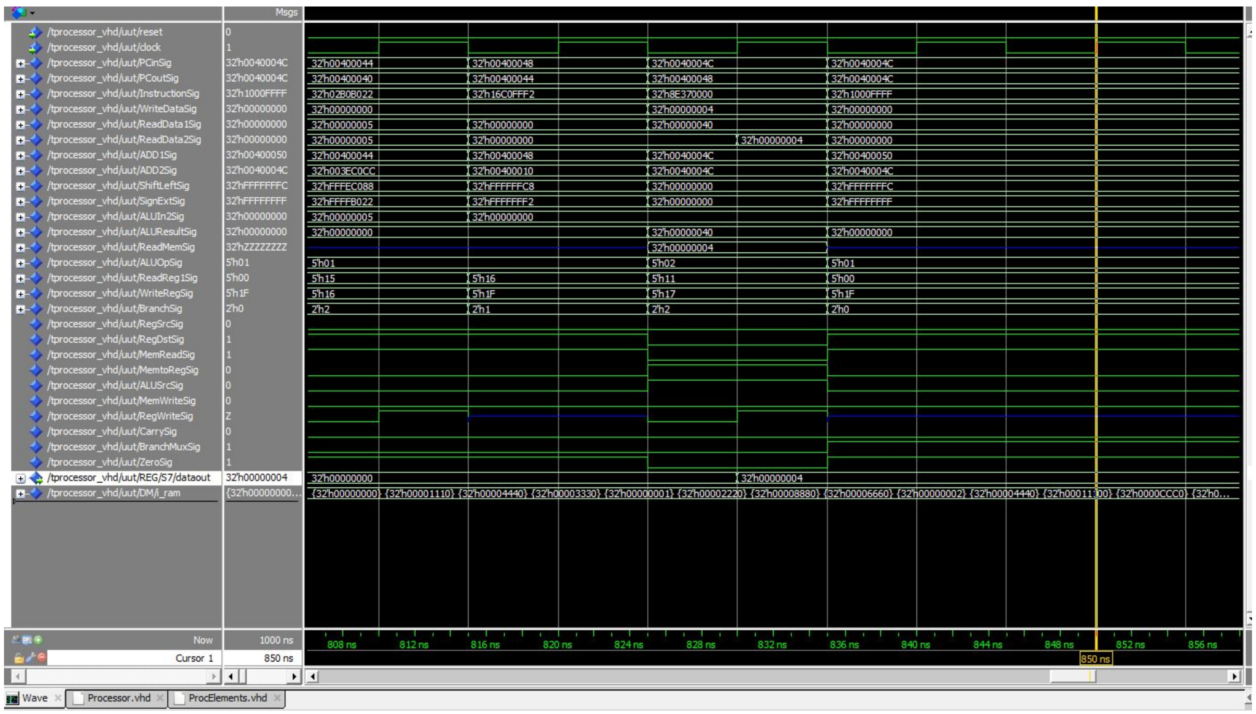
```
/tprocessor_vhd/uut/reset            0
/tprocessor_vhd/uut/clock            1
/tprocessor_vhd/uut/PCinSig          32'h00400018
/tprocessor_vhd/uut/PCoutSig         32'h00400014
/tprocessor_vhd/uut/InstructionSig   32'h00118880
/tprocessor_vhd/uut/WriteDataSig     32'h00000100
/tprocessor_vhd/uut/ReadData1Sig     32'h00000040
/tprocessor_vhd/uut/ReadData2Sig     32'h00000040
/tprocessor_vhd/uut/ADD1Sig          32'h00400018
/tprocessor_vhd/uut/ADD2Sig          32'h003E2218
/tprocessor_vhd/uut/ShiftLeftSig     32'hFFFE2200
/tprocessor_vhd/uut/SignExtSig       32'hFFFF8880
/tprocessor_vhd/uut/ALUIn2Sig        32'hFFFF8880
/tprocessor_vhd/uut/ALUResultSig     32'h00000100
/tprocessor_vhd/uut/ReadMemSig       32'hZZZZZZZZ
/tprocessor_vhd/uut/ALUOpSig         5'h11
/tprocessor_vhd/uut/ReadReg1Sig      5'h11
/tprocessor_vhd/uut/WriteRegSig      5'h11
/tprocessor_vhd/uut/BranchSig        2'h2
/tprocessor_vhd/uut/RegSrcSig        1
/tprocessor_vhd/uut/RegDstSig        1
/tprocessor_vhd/uut/MemReadSig       1
/tprocessor_vhd/uut/MemtoRegSig      0
/tprocessor_vhd/uut/ALUSrcSig        1
/tprocessor_vhd/uut/MemWriteSig      0
/tprocessor_vhd/uut/RegWriteSig      1
/tprocessor_vhd/uut/CarrySig         0
/tprocessor_vhd/uut/BranchMuxSig     0
/tprocessor_vhd/uut/ZeroSig          0
/tprocessor_vhd/uut/REG/S7/dataout   32'h00000000
/tprocessor_vhd/uut/DM/i_ram         {32'h00000000...
Now       1000 ns
Cursor 1  700 ns
Wave | Processor.vhd | ProcElements.vhd
```

700 ns



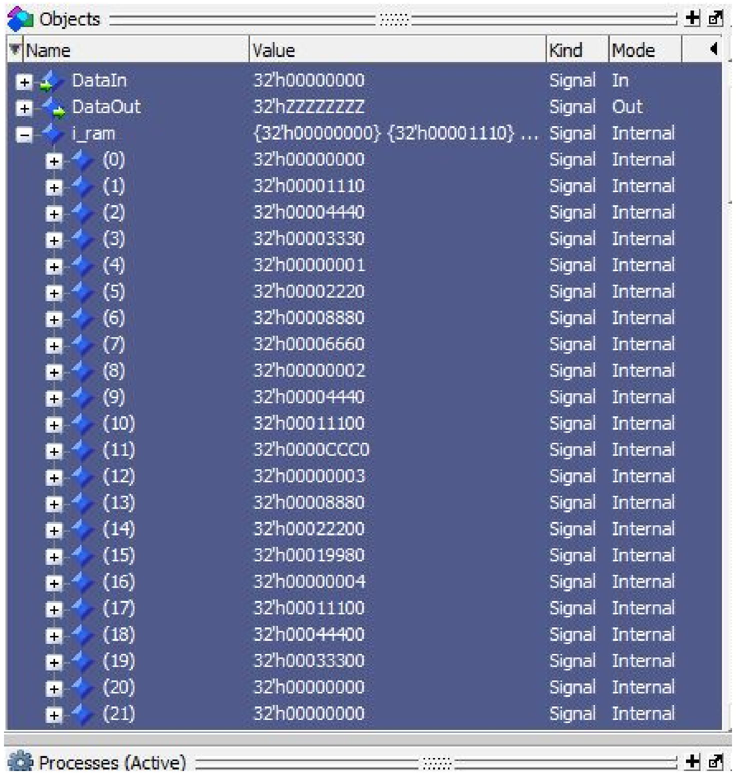
```
/tprocessor_vhd/uut/reset            0
/tprocessor_vhd/uut/clock            1
/tprocessor_vhd/uut/PCinSig          32'h00400040
/tprocessor_vhd/uut/PCoutSig         32'h0040003C
/tprocessor_vhd/uut/InstructionSig   32'h20150005
/tprocessor_vhd/uut/WriteDataSig     32'h00000005
/tprocessor_vhd/uut/ReadData1Sig     32'h00000000
/tprocessor_vhd/uut/ReadData2Sig     32'h00000005
/tprocessor_vhd/uut/ADD1Sig          32'h00400040
/tprocessor_vhd/uut/ADD2Sig          32'h00400054
/tprocessor_vhd/uut/ShiftLeftSig     32'h00000014
/tprocessor_vhd/uut/SignExtSig       32'h00000005
/tprocessor_vhd/uut/ALUIn2Sig        32'h00000005
/tprocessor_vhd/uut/ALUResultSig     32'h00000005
/tprocessor_vhd/uut/ReadMemSig       32'hZZZZZZZZ
/tprocessor_vhd/uut/ALUOpSig         5'h02
/tprocessor_vhd/uut/ReadReg1Sig      5'h00
/tprocessor_vhd/uut/WriteRegSig      5'h15
/tprocessor_vhd/uut/BranchSig        2'h2
/tprocessor_vhd/uut/RegSrcSig        0
/tprocessor_vhd/uut/RegDstSig        0
/tprocessor_vhd/uut/MemReadSig       1
/tprocessor_vhd/uut/MemtoRegSig      0
/tprocessor_vhd/uut/ALUSrcSig        1
/tprocessor_vhd/uut/MemWriteSig      0
/tprocessor_vhd/uut/RegWriteSig      1
/tprocessor_vhd/uut/CarrySig         0
/tprocessor_vhd/uut/BranchMuxSig     0
/tprocessor_vhd/uut/ZeroSig          0
/tprocessor_vhd/uut/REG/S7/dataout   32'h00000000
/tprocessor_vhd/uut/DM/i_ram         {32'h00000000...
Now       1000 ns
Cursor 1  800 ns
Wave | Processor.vhd | ProcElements.vhd
```

800 ns



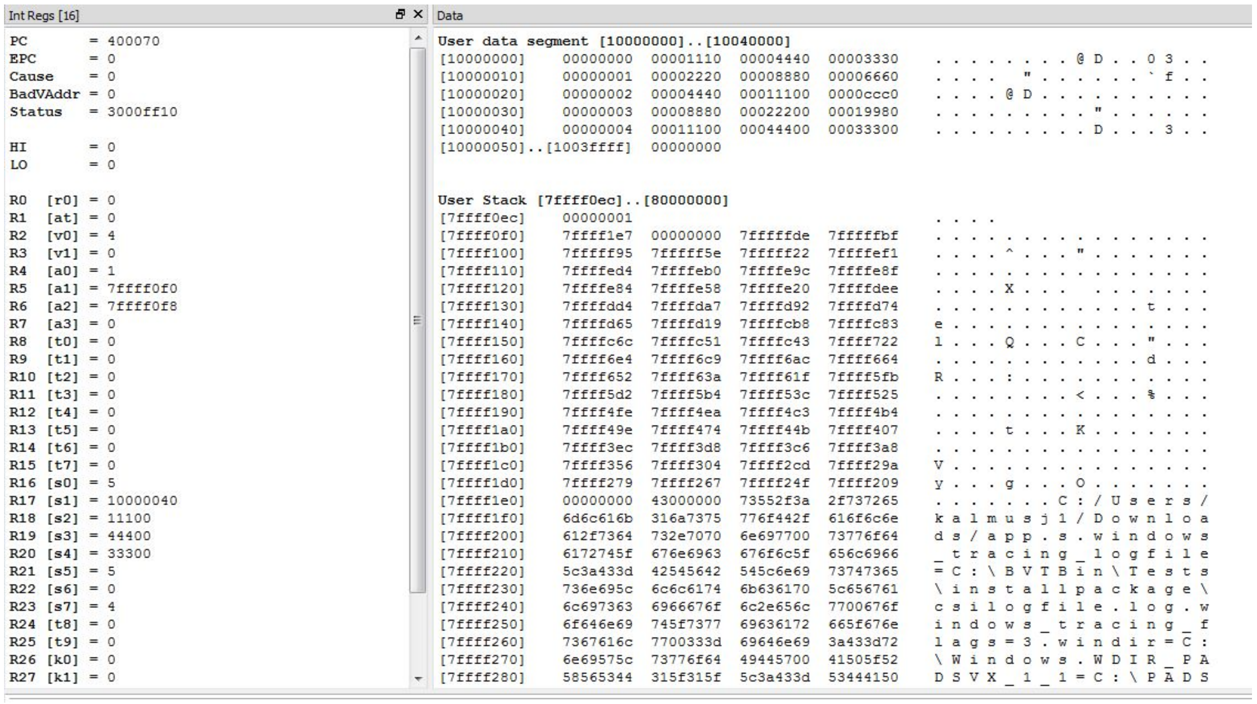
```
/tprocessor_vhd/uut/reset              0
/tprocessor_vhd/uut/clock              1
/tprocessor_vhd/uut/PCinSig            32'h0040004C
/tprocessor_vhd/uut/PCoutSig           32'h0040004C
/tprocessor_vhd/uut/InstructionSig     32'h1000FFFF
/tprocessor_vhd/uut/WriteDataSig       32'h00000000
/tprocessor_vhd/uut/ReadData1Sig       32'h00000000
/tprocessor_vhd/uut/ReadData2Sig       32'h00000000
/tprocessor_vhd/uut/ADD1Sig            32'h00400050
/tprocessor_vhd/uut/ADD2Sig            32'h0040004C
/tprocessor_vhd/uut/ShiftLeftSig       32'hFFFFFFFC
/tprocessor_vhd/uut/SignExtSig         32'hFFFFFFFF
/tprocessor_vhd/uut/ALUIn2Sig          32'h00000000
/tprocessor_vhd/uut/ALUResultSig       32'h00000000
/tprocessor_vhd/uut/ReadMemSig         32'hZZZZZZZZ
/tprocessor_vhd/uut/ALUOpSig           5'h01
/tprocessor_vhd/uut/ReadReg1Sig        5'h00
/tprocessor_vhd/uut/WriteRegSig        5'h1F
/tprocessor_vhd/uut/BranchSig          2'h0
/tprocessor_vhd/uut/RegSrcSig          0
/tprocessor_vhd/uut/RegDstSig          1
/tprocessor_vhd/uut/MemReadSig         1
/tprocessor_vhd/uut/MemtoRegSig        0
/tprocessor_vhd/uut/ALUSrcSig          0
/tprocessor_vhd/uut/MemWriteSig        0
/tprocessor_vhd/uut/RegWriteSig        Z
/tprocessor_vhd/uut/CarrySig           0
/tprocessor_vhd/uut/BranchMuxSig       1
/tprocessor_vhd/uut/ZeroSig            1
/tprocessor_vhd/uut/REG/S7/dataout     32'h00000004
/tprocessor_vhd/uut/DM/i_ram           {32'h00000000...

Now       1000 ns
Cursor 1  850 ns
```

850 ns (Final State) s7 reads 4



Name	Value	Kind	Mode
DataIn	32'h00000000	Signal	In
DataOut	32'hZZZZZZZZ	Signal	Out
i_ram	{32'h00000000} {32'h00001110} ...	Signal	Internal
(0)	32'h00000000	Signal	Internal
(1)	32'h00001110	Signal	Internal
(2)	32'h00004440	Signal	Internal
(3)	32'h00003330	Signal	Internal
(4)	32'h00000001	Signal	Internal
(5)	32'h00002220	Signal	Internal
(6)	32'h00008880	Signal	Internal
(7)	32'h00006660	Signal	Internal
(8)	32'h00000002	Signal	Internal
(9)	32'h00004440	Signal	Internal
(10)	32'h00011100	Signal	Internal
(11)	32'h0000CCC0	Signal	Internal
(12)	32'h00000003	Signal	Internal
(13)	32'h00008880	Signal	Internal
(14)	32'h00022200	Signal	Internal
(15)	32'h00019980	Signal	Internal
(16)	32'h00000004	Signal	Internal
(17)	32'h00011100	Signal	Internal
(18)	32'h00044400	Signal	Internal
(19)	32'h00033300	Signal	Internal
(20)	32'h00000000	Signal	Internal
(21)	32'h00000000	Signal	Internal

850 ns (Final Memory State)



```
Int Regs [16]
PC       = 400070
EPC      = 0
Cause    = 0
BadVAddr = 0
Status   = 3000ff10

HI       = 0
LO       = 0

R0  [r0] = 0
R1  [at] = 0
R2  [v0] = 4
R3  [v1] = 0
R4  [a0] = 1
R5  [a1] = 7ffff0f0
R6  [a2] = 7ffff0f8
R7  [a3] = 0
R8  [t0] = 0
R9  [t1] = 0
R10 [t2] = 0
R11 [t3] = 0
R12 [t4] = 0
R13 [t5] = 0
R14 [t6] = 0
R15 [t7] = 0
R16 [s0] = 5
R17 [s1] = 10000040
R18 [s2] = 11100
R19 [s3] = 44400
R20 [s4] = 33300
R21 [s5] = 5
R22 [s6] = 0
R23 [s7] = 4
R24 [t8] = 0
R25 [t9] = 0
R26 [k0] = 0
R27 [k1] = 0
```

```
Data
User data segment [10000000]..[10040000]
[10000000]    00000000  00001110  00004440  00003330    . . . . . . . . @ D . . 0 3 . .
[10000010]    00000001  00002220  00008880  00006660    . . . .   " . . . . . . ` f . .
[10000020]    00000002  00004440  00011100  0000ccc0    . . . . @ D . . . . . . . . . .
[10000030]    00000003  00008880  00022200  00019980    . . . . . . . . . " . . . . . .
[10000040]    00000004  00011100  00044400  00033300    . . . . . . . . . D . . . 3 . .
[10000050]..[1003ffff]  00000000


User Stack [7ffff0ec]..[80000000]
[7ffff0ec]    00000001                                  . . . .
[7ffff0f0]    7ffff1e7  00000000  7fffffde  7fffffbf    . . . . . . . . . . . . . . . .
[7ffff100]    7fffff95  7fffff5e  7fffff22  7ffffef1    . . . . ^ . . . " . . . . . . .
[7ffff110]    7ffffed4  7ffffeb0  7ffffe9c  7ffffe8f    . . . . . . . . . . . . . . . .
[7ffff120]    7ffffe84  7ffffe58  7ffffe20  7ffffdee    . . . . X . . .   . . . . . . .
[7ffff130]    7ffffdd4  7ffffda7  7ffffd92  7ffffd74    . . . . . . . . . . . . t . . .
[7ffff140]    7ffffd65  7ffffd19  7ffffcb8  7ffffc83    e . . . . . . . . . . . . . . .
[7ffff150]    7ffffc6c  7ffffc51  7ffffc43  7ffff722    l . . . Q . . . C . . . " . . .
[7ffff160]    7ffff6e4  7ffff6c9  7ffff6ac  7ffff664    . . . . . . . . . . . . d . . .
[7ffff170]    7ffff652  7ffff63a  7ffff61f  7ffff5fb    R . . . : . . . . . . . . . . .
[7ffff180]    7ffff5d2  7ffff5b4  7ffff53c  7ffff525    . . . . . . . . < . . . % . . .
[7ffff190]    7ffff4fe  7ffff4ea  7ffff4c3  7ffff4b4    . . . . . . . . . . . . . . . .
[7ffff1a0]    7ffff49e  7ffff474  7ffff44b  7ffff407    . . . . t . . . K . . . . . . .
[7ffff1b0]    7ffff3ec  7ffff3d8  7ffff3c6  7ffff3a8    . . . . . . . . . . . . . . . .
[7ffff1c0]    7ffff356  7ffff304  7ffff2cd  7ffff29a    V . . . . . . . . . . . . . . .
[7ffff1d0]    7ffff279  7ffff267  7ffff24f  7ffff209    y . . . g . . . O . . . . . . .
[7ffff1e0]    00000000  43000000  73552f3a  2f737265    . . . . . . . C : / U s e r s /
[7ffff1f0]    6d6c616b  316a7375  776f442f  616f6c6e    k a l m u s j 1 / D o w n l o a
[7ffff200]    612f7364  732e7070  6e697700  73776f64    d s / a p p . s . w i n d o w s
[7ffff210]    6172745f  676e6963  676f6c5f  656c6966    _ t r a c i n g _ l o g f i l e
[7ffff220]    5c3a433d  42545642  545c6e69  73747365    = C : \ B V T B i n \ T e s t s
[7ffff230]    736e695c  6c6c6174  6b636170  5c656761    \ i n s t a l l p a c k a g e \
[7ffff240]    6c697363  6966676f  6c2e656c  7700676f    c s i l o g f i l e . l o g . w
[7ffff250]    6f646e69  745f7377  69636172  665f676e    i n d o w s _ t r a c i n g _ f
[7ffff260]    7367616c  7700333d  69646e69  3a433d72    l a g s = 3 . w i n d i r = C :
[7ffff270]    6e69575c  73776f64  49445700  41505f52    \ W i n d o w s . W D I R _ P A
[7ffff280]    58565344  315f315f  5c3a433d  53444150    D S V X _ 1 _ 1 = C : \ P A D S
```

QTSpim results match VHDL final state

One way to improve the test program is to incorporate all applicable instructions. The current test program does not have tests for AND, OR, ORI, and SRL. If we incorporated these, the test program will be fully inclusive for all operations possible in our microprocessor.