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Area Efficient Modified Vedic Multiplier

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***Abstract*— This paper describes the design of high speed Vedic multiplier that uses the techniques of Vedic mathematics based on 16 sutras (algorithms) to improve the performance. In this paper the efficiency of Urdhva Tiryagbhyam (vertical and crosswise) Vedic method for multiplication which is different from the process of normal multiplication is presented. Urdhva -Tiryagbhyam is the most efficient algorithm that gives minimum delay for multiplication for all types of numbers irrespective of their size. Vedic multiplier is coded in Verilog HDL and stimulated and synthesized by using XILINX software 12.2 on Spartan 3E kit. Further the design of array multiplier is compared with the proposed multiplier in terms of delay, memory and power consumption.**

Keywords*— *Vedic mathematics, Vedic multiplier, Urdhva-Tiryagbhyam, Array multiplier, Ripple Carry Adder (RCA), Binary to Excess Code Converter (BEC), Half Adder (HA), Full Adder(FA), Carry Select Adder (CSLA).

I. INTRODUCTION

Multiplication is an important fundamental arithmetic operation in Digital Signal Processing (DSP) applications such as Convolution, Fast Fourier Transform (FFT) and also in microprocessors [1, 2].Depending on the time consuming for the multiplication process we can determine the performance of the system that uses multiplier. In order to decrease the consumption of time we require a high speed efficient multiplier.

The requirement for high speed processing system has been increased due to the raising applications in signal processing. Reducing the time delay and power consumption are the essential demands for many applications. Depending on the arrangement of digital components, we have multipliers of different type [1]. As the multiplier decides the performance of the system, it is placed in the critical delay path in most of the DSP algorithms [1]. In this paper a multiplier of different type that uses fundamentals in Vedic mathematics is presented. Vedic Multiplier is one of the fastest and low power consumption multiplier. There are many algorithms in literature that performs multiplication but each of it has its advantages and disadvantages in terms of area, power and delay [1]**.**

In this paper 16bit proposed Vedic multiplier is implemented using verilog HDL language and the Design summary details is compared with the Array multiplier.

The brief is structured as follows. Section II deals with Preliminaries. Vedic Mathematics, Vedic Multiplier and Array multiplier are presented in sections III, IV and V. Section VI presents implementation of Vedic 16x16 multiplier using BEC. Sections VII and VIII deals with results and conclusion.

II. PRELIMINARIES

A. Half Adder: If two inputs A, B are given to the half adder (HA) then the result is two 1-bit outputs i.e., sum and carry.

$$sum = a\ XOR\ b \qquad (1)$$

$$carry = a.b \qquad (2)$$

B. Full Adder: The three inputs A, B, C are given to the full adder (FA) which is the combination of two half adders then the result is two 1-bit outputs i.e., sum and carry.

$$sum = a\ XOR\ b\ XOR\ c \qquad (3)$$

$$carry = a.b + b.c + c.a \qquad (4)$$

C. Ripple Carry Adder: A ripple carry adder (RCA) is a logical circuit in which the carry-out of each full adder is given as the carry input to the next succeeding full adder. It is so called because it gets rippled to the next stage.

a) Area evaluation:

For 4bit RCA 8 XOR gates for the generation of sum and 8 AND gates for carry are required. In each XOR gate 2 INVERTERS, 2 AND, 1 OR gates are needed.

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b) Delay Evaluation for 4bit Ripple Carry Adder:

For the addition of N bits we require N full adders and they are cascaded in parallel. To get the output of each full adder we get a delay of 6 units for sum and 5 units for carry. If we consider a 4 bit ripple carry adder we get total delay of 12 units for sum S3(12) and 11 units for carry Cout(11).

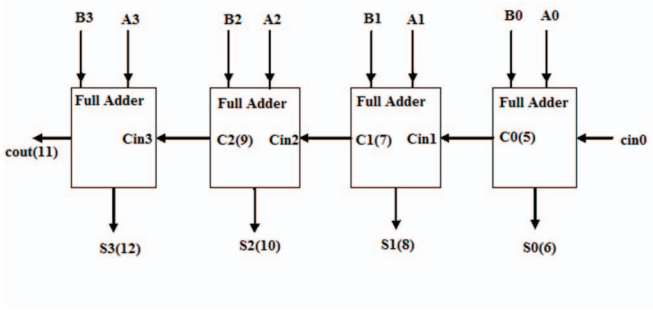

Fig.1. Ripple Carry Adder (RCA) for 4 bit

D. Binary To Excess Converter: The main use of Binary to Excess Converter is to increase the speed of operation and to achieve low area when compared to Ripple Carry Adder (RCA). Normally in the case of Carry Select Adder (CSLA) output sum and carry bits are generated by considering cin=0 and cin=1 and the final sum and carry are selected by using multiplexers where cin is taken as selection line. For BEC adder cin=1 is replaced by Binary to Excess Code Converter in the regular CSLA structure to achieve low area. The main advantage of using BEC adder is, it uses less number of logic gates than the N-bit Ripple Carry Adder which in turn reduces the power consumption and time delay. The following diagram shows the addition of 4bits a(0), a(1), a(2), a(3) using BEC [11,12]. BEC can be used for any number of bits.

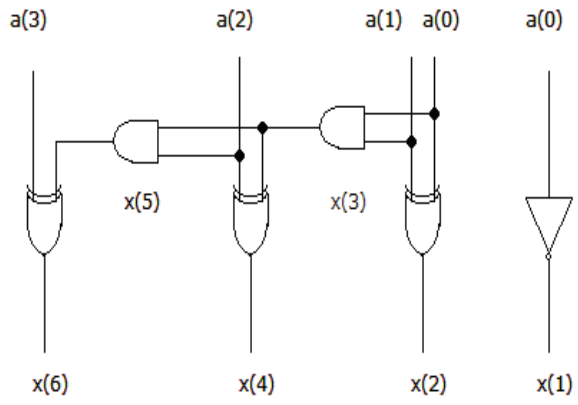

Fig.2.Binary to Excess Code Converter

III. VEDIC MATHEMATICS

The word Vedic is derived from Sanskrit word Veda which means to know without limit. The word Veda covers all Veda-sakhas known to humanity. There are four Vedas: The Rigveda, The Yajurveda, The Samaveda, The Atharvaveda.

Swami Bharati Krishna Tirtha (1884-1960), former Jagadguru Sankaracharya of Puri culled a set of 16 Sutras (aphorisms) and 13 Sub - Sutras (corollaries) from the Atharva Veda [1,9]. He developed methods and techniques for amplifying the principles contained in the aphorisms and their corollaries, and called it Vedic Mathematics.

Nikhilam Navatashcaramam Dashatah sutra and Urdhva–Tiryagbhyam sutra are two sutras used for multiplication. Urdhva–Tiryagbhyam sutra which is applicable to all cases of multiplication and also for the division of large number by another large number. In this paper the multiplication process using Urdhva-Tiryagbhyam sutra is explained [2]. The two sutras used for multiplication process and their meanings are listed below.

TABLE 1. VEDIC SUTRAS WITH MEANINGS

No	Sutras	Corollary	Meaning
1	Nikhilam Navatashcaramam Dashatah	Sisyate sesasamjnah	All from 9 and the last from 10
2	Urdhva-tiryagbhyam	Adyamadyenantyamantyena	Vertically and Crosswise

IV. VEDIC MULTIPLIER

Vedic multiplier is designed by using the concept of Vedic mathematics which uses one of the 16 sutras in it, called Urdhva-Tiryagbhyam (vertically and crosswise multiplication) sutra [2, 10]. By using this multiplier multiplication for all types of numbers irrespective of their size is performed. In this paper the process of 4x4 Vedic multiplier is explained and further implemented to 16bit.

The multiplication process for the two 2bits is shown below by using AND gates and HALF ADDER. Here the multiplicand is a1a0 and the multiplier is b1b0. The Partial products are a0b0, a1b0, a0b1, a1b1. By using the Vedic multiplication process we get the output of 4bits as q0, q1, q2, q3.

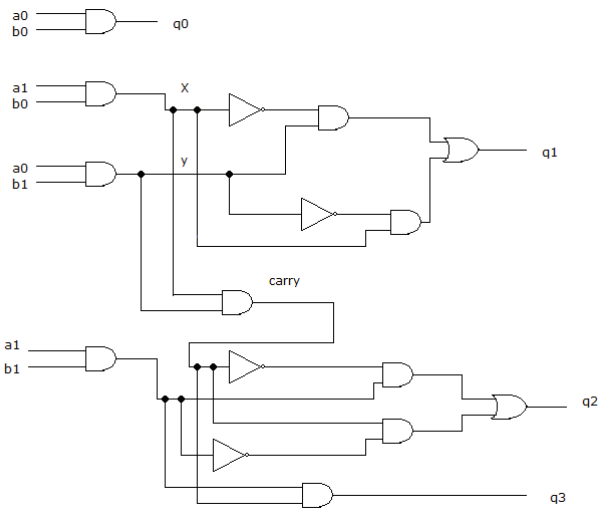

Fig. 3.Block Diagram Representation of 2x2 Vedic multipler

A. Methodology for 4x4 Vedic multiplier:

The dot representation for 4x4 Vedic multiplier is shown below [3,4]. Here the first row represents the multiplicand bits (a3a2a1a0) and the 2nd row represents the multiplier bits (b3b2b1b0). In this Vedic multiplication process addition of bits takes place which are of equal weights. In the 1st case 0 weights are added i.e., only a0b0. In 2nd case weights equal to one are added by using half adder i.e., a0b1 +a1b0. In the 3rd case Partial products of weight equal to 3 are added by using full adder i.e., a0b2+a2b0+a1b1. If any carry is generated during addition process, it will be added to the next step of addition. The maximum weight for 4 bit multiplication is 6.The same procedure is followed until we get the output as 8 bits including carry[5,7].

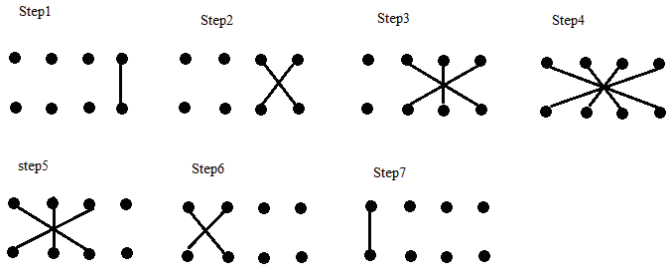

Fig. 4.Dot representation of 4x4 Vedic multiplier

The above mentioned procedure can be used for bits of any size. But the bits of same weights should be added in a single step. By using the same methodology mentioned above this work has been extended up to 16bits.

V. ARRAY MULTIPLIER

The traditional method for multiplication is done by using Array multiplier. Array multiplier is popular due to its familiar structure as it is based on add and shift algorithm [2]. In Array multiplication operation, number of partial products to be added is the main parameter that determines the performance of the multiplier. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit. These products are added systematically by shifting operation .There will be a shift in partial products after the multiplication of one bit of multiplier with multiplicand.

After the multiplication process of all the multiplicand bits with all the multiplier bits, the final step is to add all the partial products to get the result. For this firstly group the partial products in order of two rows each and the products which fall under same group are added by using conventional half and full adders and their respective carries are passed on to next stages. The result from the first step is then added to the next row of partial products. The same procedure is followed until final output is obtained. Representation of 8*8 array multiplier [8] is shown in Figure 4

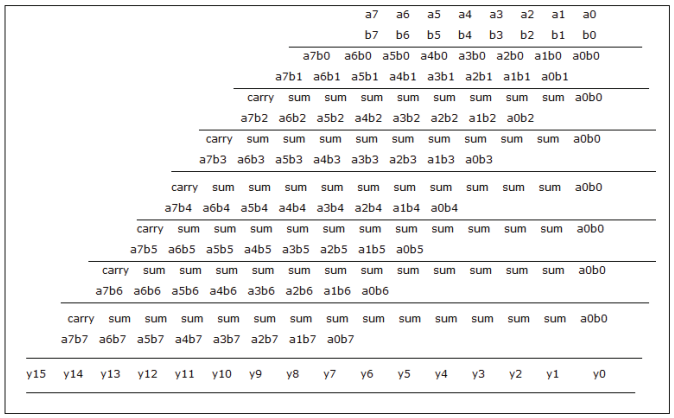

Fig. 5.Array multiplier for 8bit

Here the multiplication process of multiplicand (8bits) with multiplier (8bits) using Array multiplier is shown. The output as 16bits in which 15 bits are sum bits and one carry bit is obtained.

VI. IMPLEMENTATION OF VEDIC 16x16 MULTIPLIER USING BEC:

The design of 4x4 Vedic multiplier is used as a basic building block diagram for design of 8x8 Vedic multiplier. Further design of 16x16 is implemented by using 8x8 Vedic multiplier as basic building block. The aim of using BEC is to reduce the usage of gates compared to normal Vedic multiplier which in turn reduces the power consumption.

The structure of proposed Vedic multiplier is shown in figure 6. It has 4 groups of same size i.e each group consists of 8*8 Vedic multiplier whose inputs are partitioned according to Urdhva-tiryagbhyam sutra. Outputs from Vedic multiplier are given as inputs to BEC adders of different sizes.

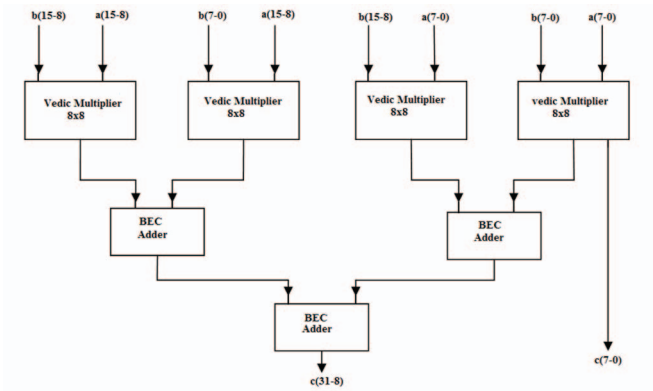

Fig. 6.Block diagram of 16x16 Vedic multiplier using BEC

VII. RESULTS

Here Verilog HDL code for 16x16 bit Vedic multiplier is synthesized using XILINX ISE Design Suite 12.2 and is implemented on FPGA device xc3s500-5fg320 of Spartan 3E family.

The Input output waveforms which are generated by using XILINX software and device utilization summary are shown

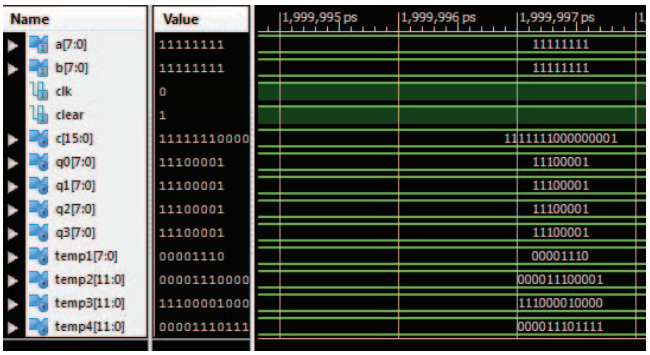

Fig. 7. Simulation results for 8x8 Vedic multiplier using BEC

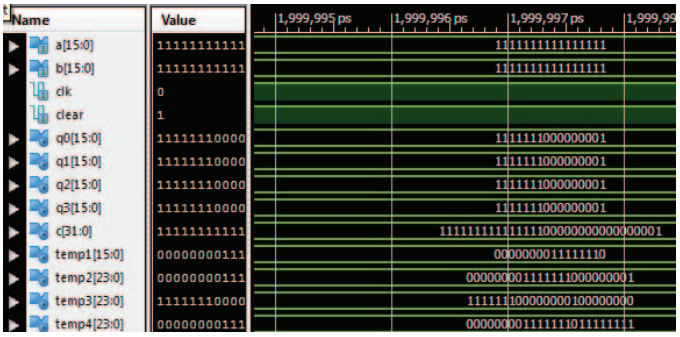

Fig.8. Simulation results for 16x16 Vedic multiplier using BEC

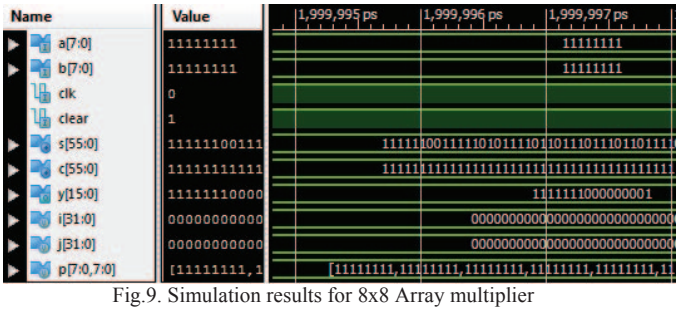

Fig.9. Simulation results for 8x8 Array multiplier

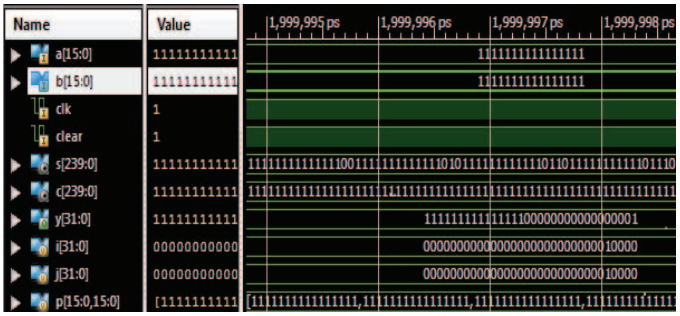

Fig.10. Simulation results for 16x16 Array multiplier

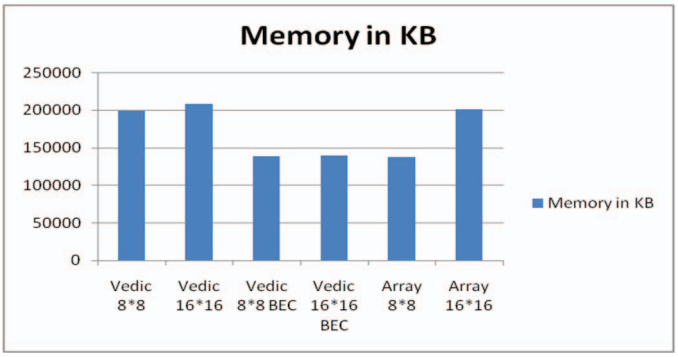

Fig.11. Results for memory utilization

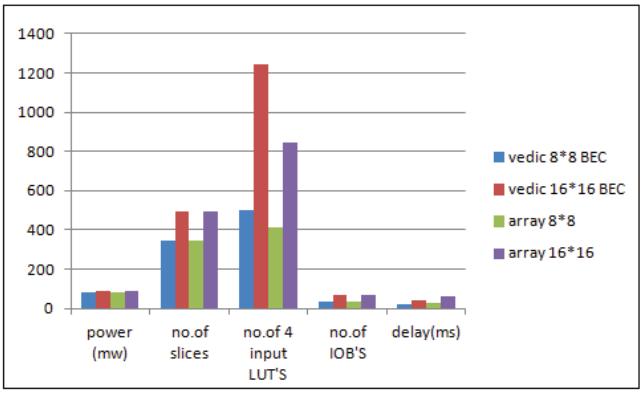

Fig.12. Results for logic utilization

A. Logic Utilization Summary:

The below table2 shows the comparison of Vedic multiplier using BEC and Array multiplier for both 8bit and 16bit.

TABLE 2. Comparison between Array and Vedic multipliers

Logic utilization	Vedic 8x8 BEC	Vedic 16x16 BEC	Array 8x8	Array 16x16
Power in mw	83.79	86.91	83.79	86.22
No.of slice Registers	347/9312	493/9312	347/9312	493/9312
No.of4 input LUTS	497/9312	1243/9312	411/9312	844/9312
No. of IOBs	34/232	66/232	34/232	66/232
Delay in ns	23.18	38.82	24.88	61.49
Memory in KB	138728	139624	136956	200524

VIII. CONCLUSION

From the above results it is clear that for 8bit, memory utilized for Vedic multiplier using BEC (138728KB) is less when compared to Vedic multiplier (198568KB). Similarly in the case of 16bit, memory utilized for Vedic multiplier using BEC (139624KB) is less when compared to normal Vedic multiplier (208268KB).

By comparing the values of both Array and Vedic multiplier it is clear that the delay for Vedic multiplier is much less when compared with Array multiplier. As we increase number of bits delay can be reduced by using Vedic multiplier than Array multiplier.

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