**Final Project Proposal: Optimized High Speed and Low Power Booth Multiplier**

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Multiplication is a critical and unavoidable operation in every system. With a efficient multiplier, one system may deliver data to the next computation stage in a timely manner. Moreover, area is also a concern in modern designs such that the multiplier should be compact. Therefore, in this project, we are proposing to develop a new multiplier solution that aims to extend the of a targeting at delay and area complexity.

In particular, we will examine closely how to extend to work of a booth multiplier combined with a wallace multiplier. A radix-4 multiplier can reduces the computation delay by half with an acceptable hardware cost. …<Wallace multiplier> By extracting the advantages of both multiplier and conducting some local optimization, we may find a more optimal multiplier solution.

To begin the research, we have found several related work on this particular subject. *Studies of Various High Speed Multipliers* presents a modified booth multiplier that reduces the partial product by half. *A High Speed Wallace Tree Multiplier Using Modified Booth Algorithm for Fast Arithmetic Circuits* shows a Wallace Tree Multiplier where the partial product is computed using booth multiplier, and this architecture change results in significant reduction in delay. *Implementation of Pipelined Booth Encoded Wallace Tree Multiplier Architecture* demonstrates a wallace tree multiplier solution that has a four-stage-pipeline. With pipelining, the multiplier has a high throughput after the first four cycles. We will then further extend our research of multipliers based on these previous works.

As an initial outline to approach the solution, we will start with the theoretical derivation of the optimization we proposed. Then we will compare the the result with the classical multipliers as an evaluation of our solution. Lastly, we will implement the design in Verilog to prove the feasibility of our design.