Optimization for High Speed Multiplier

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*Abstract*—Multiplication is a critical and unavoidable operation in most of the real-world systems. However, multipliers usually have problems in high latency, low throughput, and high power consumption. Therefore, we are motivated to propose a new multiplier solution by using pipelined structure, modified Booth encoding, fast sign-extension method, reduced area reduction architecture, and a better final stage adder. We did comparison experiments to illustrate our design’s functionality and effectiveness. Through theoretical analysis and performance estimation, we show that our design has lower latency, higher throughput, and lower power consumption.

*Index Terms*—Booth encoding, high-speed multiplier, pipeline, reduced area reduction.

# INTRODUCTION

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ultiplication is of considerable significance in systems with computation demands. However, multipliers usually take many cycles to generate outputs, thus may not be able to deliver data to the next computation stage in a timely manner. In addition, long latency combinational logic leads to relatively low throughput. Latency issue apart, area complexity is also a concern in modern designs such that the multiplier should be compact, otherwise may induce potentially more power dissipation and higher financial cost. This situation inspires us to optimize the multiplier targeting at lower delay, higher throughput, and relatively lower area complexity. A pipelined high-speed multiplier is thus proposed in this paper.

Booth multiplier [1], is based on an algorithm designed for fast multiplication. It first re-encodes adjacent bits in one of the multiplicand, aimed at reducing the number of partial products. Then all the partial products will be simply calculated and sign-extended in order to achieve multiplication of two’s complement numbers. Finally, weighted summation will be applied to those partial products to generate the result. Therefore, there are several issues for us to address: (1) how to trade-off between performance benefit and overhead of different radix of Booth algorithm; (2) how to achieve efficient sign extension; (3) how to achieve higher performance in partial product summation; and (4) how to reduce the area complexity of the hardware design.

To address the above issues, a number of algorithms and methodologies have been proposed in the literature. Particularly, S. Abraham *et al*. [2] proposes a modified Booth multiplier that halves the number of partial products. S. Dubey *et al*. [3] shows a Wallace Tree multiplier where the partial

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products are computed by Booth multiplier, and this architecture innovation results in significant reduction in delay. R. D. Kshirsagar *et al*. [4] demonstrates a Wallace-tree-based high throughput multiplier by using a four-stage pipeline.

Inspired by the above work, we propose a high-speed multiplier to achieve lower latency, higher throughput, and lower power consumption. Specifically, we adopt radix-4 modified Booth Encoding to halve the number of partial products a multiplier must add together. Then, we adopt reduced area reduction architecture with full adders and half adders to reduce those partial products to two lines, in order to cut down the use of half adders while keeping the reduction efficiency. Additionally, the final two lines of bits are added by an optimized LING adder, to achieve higher speed compared to several other widely used adders. To improve the throughput of our proposed multiplier, we partition our design into a three-stage pipeline based on its latency analysis. We evaluate the throughput of our design by comparing with the non-pipelined counterpart. We also validate the performance superiority by comparing the latency of our optimized multiplier with other structures, including carry look-ahead adder (CLA) and variable-length carry select adder (CSLA).

# Modified Radix-4 Booth Encoding

When doing multiplication of two N-bit binary two’s complement numbers, there will be N partial products (PP) as well as a lot of sign extension bits. In order to add N lines of partial products, N addition operations are needed, with relatively great computation latency and power dissipation. Booth encoding, thus offers a solution to reduce the total number of addition required in the above process. Specifically, as we used in this design, radix-4 Booth Encoding consider three consecutive bits from the least significant bit (LSB) to most significant bit (MSB), with a “0” appended to the LSB. We use {} to represent all bits of the encoded number, and represents the additional “0” in the LSB. Booth algorithm represents three consecutive bits {} with a certain value from set {-2, -1, 0, 1, 2}. The principal in generating Booth Code (BC) is basically giving different weights to {}, as shown below:

(1)

Thus, we have the following BCs for radix 4, as illustrated in Table I. For example, a 16-bit binary 1001101101011101 will be encoded as:

(2)

where represents Booth Encoding operation, and represent -1 and -2 respectively. After Booth Encoding, a two’s complement binary is transformed into two’s complement Booth digits, which have half of the digits as compared to the original number. We denote the multiplicand as A, and multiplier, to which Booth Encoding should be applied, as B. Through this way, the partial products can be generated by multiplexing among pre-calculated 0, -2A, -A, A, and 2A. Detailed methods to implement the pre-calculation will be covered in later sections. Note that the number of partial products for N×N bit multiply is reduced to N/2 accordingly.

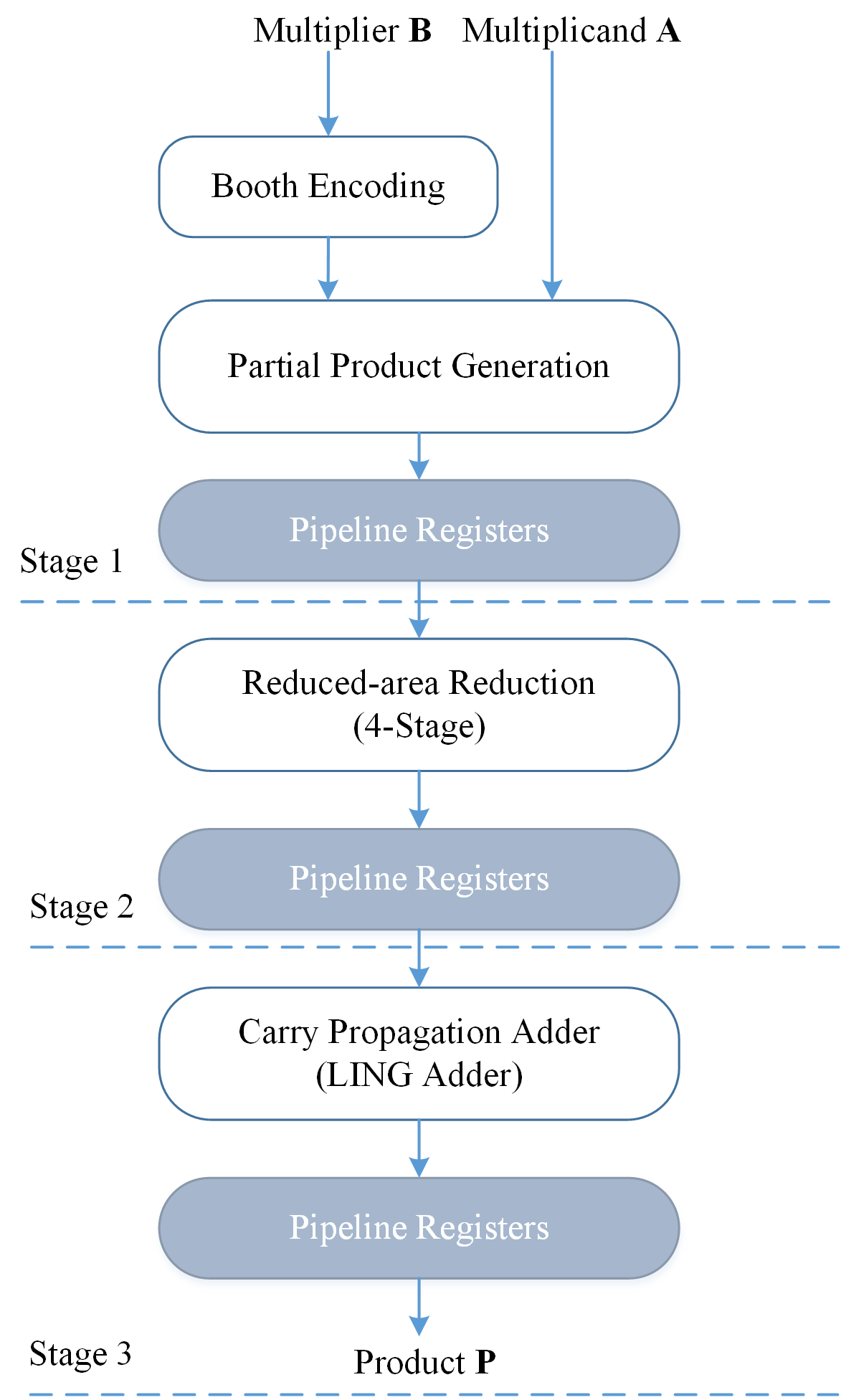


Fig. 1. Framework of our proposed 3-stage pipeline multiplier.

# Reduced-area Reduction

Reduced-area Reduction is the partial product reduction method used in Reduced-area Multiplier []. This method only allows the use of half adder when reducing the rightmost column containing exactly two bits or when it is necessary to meet with height limits specified by Dadda series at each stage, which reduces the number of half adder used in each reduction stage and the interconnect overhead as well.

# LING Adder

# Theoretical Analysis

The complete design of our proposed three-stage multiplier is shown as Fig. 1. There are mainly three stages in its architecture: (1)Booth encoding and partial product generation; (2)reduced-area reduction; and (3)carry propagation adder. Each of them will be further illustrated in the following sections.

## Booth Encoding and Partial Product Generation

As aforementioned, Booth Encoding operation converts every three consecutive digits to 3-bit sign/magnitude Booth Codes. In our implementation, the gate count for each converting is 12. Therefore, assuming the multiplier A and multiplicand B are both N-bit, with N being an even number, total gate count for Radix-4 Booth Encoding will be:

(3)

If we consider each logic gate cost one gate delay, the total gate delay for Radix-4 Booth Encoding operation is constant as follows:

(4)

Partial product generation for Radix-4 Booth Encoding requires the calculation of +A, -A, +2A, and -2A. Given that the left shift operation and the two’s complement operation extend the number of bit of the partial product and also require sign-extension, we adopted a fast sign-extension method proposed in []. This method assumes all the partial products negative, and pre-calculates the sign-extended bits. Additionally, this method delays to add 1 when doing two’s complement operation, to accelerate and simplify the process of partial product generation. In our implementation, the partial products are selected from {0, +A, -A, +2A, -2A} by N/2 N-bit wide 5:1 MUX. In addition, we have to generate the sign correction bits if the negative partial product assumption is wrong for a specific partial product, which cost approximately 8N gates. Note that the pre-calculation of sign-extension bits are hard-coded without any hardware cost. Therefore, the estimated total gate count for the partial product generation module in our design is:

(5)

The estimated gate delay of PP Gen module is also constant:

(6)

TABLE I

Booth codes for radix 4

|  |  |
| --- | --- |
|  | Booth Code |
| 000 | 0 |
| 001 | +1 |
| 010 | +1 |
| 011 | +2 |
| 100 | -2 |
| 101 | -1 |
| 110 | -1 |
| 111 | 0 |

## Partial Product Reduction

Reduced-area Reduction scheme reduces the height of the partial product matrix at the same speed of Dadda Reduction method. Specifically, in our case, 8 16-bit wide partial products with additional sign-related bits takes 4 reduction stages. Note the full adder we implemented costs 4 gate delay. thus the total gate delay of the reduction process is constant:

(7)

As mentioned in [], the hardware requirements for the original RA multipliers are full adders and half adders, where S is the number of reduction stages. Since we adopted Booth Encoding and different implementation and the total gate count is determined by the specific reduction scheme, we counted the total number of half adder and full adder we used in our case, and we used 103 full adders and 20 half adders. Given that the full adder we adopted costs 7 gates and half adder costs 2 gates. Thus the total gate count for reduction scheme is:

(8)

## Carry Propagation Adder

According to the result of final stage partial product reduction, we have to use an adder to achieve 28-bit addition. In order to accelerate the final addition process, we adopted an optimized version of carry look-ahead adder, called LING adder[].

## Pipelined Structure

In order to make a trade-off between additional hardware overhead and throughput, we divided the multiplier into three stages according to the timing report generated by Xilinx Vivado Design Suite 2018.2. The first stage consists of Booth Encoding module and Partial Product Generation module; the second stage consists of Reduced-area reduction module; and the third stage consists of the carry propagation adder. Given this pipeline strategy, the whole multiplier can be divided into three parts with relatively independent functionalities and similar latency, which can increase the maximum frequency it can work at.

# Experimental Results

To validate the functionality and demonstrate the effectiveness of our optimized multiplier, we conduct the first comparison experiment between pipelined version of our proposed design and its non-pipelined counterparts, to show the actual throughput improvement. And we also conduct a comparison experiment among LING adder, Carry Look-ahead Adder, and Carry Select Adder (CSLA) with variable-length block, to validate the superiority in delay of our proposed design. Each of those comparison designs will be detailed below.

In order to construct a 28-bit CLA, we first constructed a 16-bit CLA with 4-bit wide look-ahead logic block and then constructed 3 4-bit CLAs with the same block size.

As for 28-bit CSLA, we adopted variable-length blocks to reduce its delay. Specifically, we set the block width as 5, 7, 6, 5, and 5 from most significant bit to least significant bit. Note that we adopted ripple carry adders within each block.

As for 28-bit LING adder,

## Functionality Validation

We designed all hardware by using hardware description language Chisel3 [], and generated the corresponding Verilog codes by using the compiler it offers. Then we ran the post-implementation functional simulation in Xilinx Vivado. We input randomly generated numbers in the range of [-32768, 32767] to our proposed multiplier, and it successfully passed 65,535 random test cases and several corner test cases, which validated the correct functionality of all our designs.

## Power, Area, and Delay Simulation

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