JIAQI GU

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EDUCATION

The University of Texas at Austin	Ph.D., Electrical and Computer Engineering Integrated Circuits and System Track. Overall GPA 4.00/4.00	May 2023 (expected)
Fudan University, Shanghai, China	B.E., Microelectronic Science and Engineering (Eminent Engineer Program). Overall GPA: 3.91/4.00 (Rank: top 2/71)	Jul 2018

EXPERIENCE

Graduate Research Assistant, The University of Texas at Austin　　　　　　　　　　Jan 2019 – Present

- Designed novel frequency-domain photonic neuromorphic computing architecture for area-efficient optical neural network; achieved 3-4x area reduction by using block-circulant matrices and structured pruning compared with previous ONN architectures
- Developed differentiable quantization-aware training scheme in the unitary manifold to enable robust optical neural networks with low-precision voltage controls; achieved better accuracy and robustness with limited control resolution and device-level variations
- Proposed efficient ONN on-chip learning algorithm for optical neural networks with stochastic zeroth-order optimization algorithms; achieved 3-4x higher learning efficiency, 10x better scalability, and better robustness to thermal variations than previous methods
- Worked on photonic chip tapeout for novel ONN architectures with AMF PDKs using Synopsys optodesigner and Lumerical toolkits.
- Collaborated on the full-stack schematic design, layout, validation, tape-out, and measurement of photonic neural chips using PyTorch, Lumerical toolkits, and Synopsys optodesigner
- Collaborated on developing GPU-accelerated concurrent VLSI detailed placement with CUDA; implemented and optimized global swap and parallel auction algorithm for batched-based independent-set-matching; achieved >10x speedup than sequential implementations without quality degradation
- Collaborated on high-performance VLSI analytical global placement acceleration with CUDA on GPUs; optimized wirelength and density computation operators with CUDA; developed parallel RUDY/RISA congestion map for routability optimization; achieved 40x speedup in global placement
- Developed multi-electrostatics-based robust VLSI placement framework *DREAMPlace 3.0* with PyTorch/C++/CUDA; proposed multi-electrostatic system for optimization under fence region constraints; developed divergence-aware optimizer for robust nonlinear global placement; achieved >13% HPWL improvement and >11% top5 overflow reduction compared with ISPD2015 contest winners
- Proposed efficient ONN on-chip learning framework with power-aware mixed-training strategy and two-level algorithmic sparsity; achieved much better training stability, ~10x training efficiency improvement, and ~10x power reduction than prior methods

Graduate Research Assistant, The University of Texas at Austin　　　　　　　　　　Sep 2018 – Jan 2019

- Projected RISC-V Rocket Core on Zynq FPGA with Chisel3 and achieved communication between them
- Customized FIRRTL transformation and built infrastructure for fault injection and system state snapshot

Research Assistant, Fudan University, Shanghai, China　　　　　　　　　　Aug 2017 – Jul 2018

- Modified infant brain atlas offered by UNC and created complete tissue probability maps
- Developed two-stage reconstruction framework for infant thin-section MR image reconstruction by using GANs and CNN; research is developing brand new method to improve reconstruction performance by fusing multi-planar MR images, and improving PSNR, SSIM, and NMI by 26.2%, 93.4%, and 25.3% respectively compared to bicubic interpolation
- Collaborated on super-resolution reconstruction of ultra-sonic imaging using U-Net and GANs; improved the full width at half maximum (FWHM) of point targets by 3.23%

PUBLICATIONS

Conference Proceedings

[C1] **Jiaqi Gu**, Chenghao Feng, Zheng Zhao, Zhoufeng Ying, Ray T. Chen and David Z. Pan, "Efficient On-Chip Learning for Optical Neural Networks Through Power-Aware Sparse Zeroth-Order Optimization", *Association for the Advancement of Artificial Intelligence (AAAI)*, Virtual Conference, Feb. 02-09, 2021. (Accepted)

[C2] Shubham Rai, Walter Lau Neto, Yukio Miyasaka, Xinpei Zhang, Mingfei Yu, Qingyang Yi Masahiro Fujita, Guilherme B. Manske, Matheus F. Pontes, Leomar S. da Rosa Junior, Marilton S. de Aguiar, Paulo F. Butzen, Po-Chun Chien, Yu-Shan Huang, Hoa-Ren Wang, Jie-Hong R. Jiang, **Jiaqi Gu**, Zheng Zhao, Zixuan Jiang, David Z. Pan, et al., "Logic Synthesis Meets Machine Learning: Trading Exactness for Generalization", *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Virtual Conference, Feb. 01-05, 2021. (Accepted)

[C3] **Jiaqi Gu**, Chenghao Feng, Zheng Zhao, Zhoufeng Ying, Mingjie Liu, Ray T. Chen and David Z. Pan, "SqueezeLight: Towards Scalable Optical Neural Networks with Multi-Operand Ring Resonators", *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Virtual Conference, Feb. 01-05, 2021. (Accepted)

[C4] **Jiaqi Gu**, Zheng Zhao, Chenghao Feng, Zhoufeng Ying, Ray T. Chen and David Z. Pan, "O2NN: Optical Neural Networks with Differential Detection-Enabled Optical Operands", *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Virtual Conference, Feb. 01-05, 2021. (Accepted)

[C5] Chenghao Feng, **Jiaqi Gu**, Zhoufeng Ying, Zheng Zhao, David Z. Pan and Ray T. Chen, "Scalable fast-Fourier-transform-based (FFT-based) integrated optical neural network for compact and energy-efficient deep learning", *SPIE Photonics West*, Mar. 06-11, 2021. (Accepted)

[C6] Chenghao Feng, Zhoufeng Ying, Zheng Zhao, **Jiaqi Gu**, David Z. Pan and Ray T. Chen, "Wavelength-division-multiplexing-based electronic-photonic integrated circuits for high-performance data processing and transportation", *SPIE Photonics West*, Mar. 06-11, 2021. (Accepted)

[C7] **Jiaqi Gu**, Zheng Zhao, Chenghao Feng, Wuxi Li, Ray T. Chen and David Z. Pan, "DREAMPlace 3.0: Multi-Electrostatics Based Robustness VLSI Placement with Region Constraints", *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 02-05, 2020.

[C8] Zixuan Jiang, Keren Zhu, Mingjie Liu, **Jiaqi Gu** and David Z. Pan, "An Efficient Training Framework for Reversible Neural Architectures", *European Conference on Computer Vision (ECCV)*, Aug. 23-28, 2020.

[C9] **Jiaqi Gu**, Zheng Zhao, Chenghao Feng, Wuxi Li, Ray T. Chen and David Z. Pan, "FLOPS: Efficient On-Chip Learning for Optical Neural Networks Through Stochastic Zeroth-Order Optimization", *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, Jul. 19-23, 2020. (**Best Paper Award Finalist**)

[C10] Mario Miscuglio, Zibo Hu, Shurui Li, **Jiaqi Gu**, Aydin Babakhani, Puneet Gupta, Chee-Wei Wong, David Pan, Seth Bank, Hamed Dalir and Volker J. Sorger, "Million-channel parallelism Fourier-optic convolutional filter and neural network processor", *CLEO*, San Jose, CA, May 10-15, 2020.

[C11] Chenghao Feng, Zhoufeng Ying, Zheng Zhao, **Jiaqi Gu**, David Z. Pan and Ray T. Chen, "Integrated WDM-based Optical Comparator for High-speed Computing", *CLEO*, San Jose, CA, May 10-15, 2020.

[C12] Chenghao Feng, Zheng Zhao, Zhoufeng Ying, **Jiaqi Gu**, David Z. Pan and Ray T. Chen, "Compact design of On-chip Elman Optical Recurrent Neural Network", *CLEO*, San Jose, CA, May 10-15, 2020.

[C13] **Jiaqi Gu**, Zheng Zhao, Chenghao Feng, Ray T. Chen and David Z. Pan, "ROQ: A Noise-Aware Quantization Scheme Towards Robust Optical Neural Networks with Low-bit Controls", *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France, Mar. 09-13, 2020.

[C14] Mingjie Liu, Keren Zhu, **Jiaqi Gu**, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, "Towards Decrypting the Art of Analog Layout: Placement Quality Prediction via Transfer Learning", *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France, Mar. 09-13, 2020.

[C15] Chenghao Feng, Zhoufeng Ying, Zheng Zhao, **Jiaqi Gu**, David Z. Pan and Ray T. Chen, "Wavelength-division-multiplexing based electronic photonic network for high speed computing", *SPIE Photonics West*, San Francisco, CA, United States, Feb. 01-06, 2020.

[C16] **Jiaqi Gu**, Zheng Zhao, Chenghao Feng, Mingjie Liu, Ray T. Chen and David Z. Pan, "Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture", *ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC)*, Beijing, China, Jan. 13-16, 2020. (**Best Paper Award**)

[C17] Zheng Zhao, **Jiaqi Gu**, Zhoufeng Ying, Chenghao Feng, Ray T. Chen and David Z. Pan, "Design Technology for Scalable and Robust Photonic Integrated Circuits", *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019. (invited paper)

[C18] **Jiaqi Gu**, Ruoyao Wang, Jian Wang, Jinmei Lai and Qinghua Duan, "Remote Embedded Simulation System for SW/HW Co-design Based On Dynamic Partial Reconfiguration", *IEEE International Conference on ASIC (ASICON)*, Guizhou, China, Oct. 25-28, 2017.

Journal Articles
[J1] Zhoufeng Ying, Chenghao Feng, Zheng Zhao, **Jiaqi Gu**, Richard Soref, David Z. Pan and Ray T. Chen, "Sequential logic and pipelining in chip-based electronic-photonic digital computing", *IEEE Photonics Journal*, Oct., 2020.

[J2] **Jiaqi Gu**, Zheng Zhao, Chenghao Feng, Zhoufeng Ying, Mingjie Liu, Ray T. Chen and David Z. Pan, "Towards Hardware-Efficient Optical Neural Networks: Beyond FFT Architecture via Joint Learnability", *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Sept., 2020.

[J3] Chenghao Feng, Zhoufeng Ying, Zheng Zhao, **Jiaqi Gu**, David Z. Pan and Ray T. Chen, "Wavelength-division-multiplexing (WDM)-based integrated electronic–photonic switching network (EPSN) for high-speed data processing and transportation", *Nanophotonics*, Aug., 2020.

[J4] Yibo Lin, Zixuan Jiang, **Jiaqi Gu**, Wuxi Li, Shounak Dhar, Haoxing Ren, Brucek Khailany and David Z. Pan, "DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement", *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Jun., 2020.

[J5] Zhoufeng Ying, Chenghao Feng, Zheng Zhao, Shounak Dhar, Hamed Dalir, **Jiaqi Gu**, Yue Cheng, Richard Soref, David Pan, and Ray Chen, "Electronic-photonic Arithmetic Logic Unit for High-speed Computing", *Nature Communications*, Apr., 2020.

[J6] Yibo Lin, Wuxi Li, **Jiaqi Gu**, Mark Ren, Brucek Khailany and David Z. Pan, "ABCDPlace: Accelerated Batch-based Concurrent Detailed Placement on Multi-threaded CPUs and GPUs", *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Feb., 2020.

[J7] Ruoyao Wang, Zhenghan Fang, **Jiaqi Gu**, Yi Guo, Shicong Zhou, Yuanyuan Wang, Cai Chang and Jinhua Yu, "High-resolution Image Reconstruction for Portable Ultrasound Imaging Devices", *EURASIP Journal on Advances in Signal Processing*, Dec., 2019.
[J8] **Jiaqi Gu**, Zeju Li, Yuanyuan Wang, Haowei Yang, Zhongwei Qiao and Jinhua Yu, "Deep Generative Adversarial Networks for Thin-section Infant MR Image Reconstruction", *IEEE Access*, May, 2019.

RELATED GRADUATE COURSES/CERTIFICATE

- Computer Architecture (EE 382N 1)
- High Speed Computer Arithmetic (EE 382N 14)
- Computer Architecture: Parallelism/Locality (EE 382N 20)
- Parallel Algorithm Scientific Computing (CS 395T)
- Reinforcement Learning: Theory & Practice (CS 394R)
- VLSI I (EE 382M.7)
- VLSI Physical Design Automation (EE 382M)
- Cross-layer Machine Learning Algorithm/Hardware Co-design (EE 382V)
- VLSI CAD and Optimization (EE 382M 26) (on-going)
- Combinatorial Optimization (EE 381V) (on-going)
- Certificate of NVIDIA workshop on Fundamentals of Accelerated Computing with CUDA Python, NVIDIA DLI, 2019

HONORS

• **Best Poster Award**, NSF Workshop on Machine Learning Hardware	2020
• **1st Place**, ACM/SIGDA Student Research Competition	2020
• 7th Place, 2020 IWLS Contest on Machine Learning + Logic Synthesis	2020
• DAC Young Fellow, 57th IEEE/ACM Design Automation Conference (DAC)	2020
• Best Paper Award Candidate (1 out of 6), 57th IEEE/ACM Design Automation Conference (DAC)	2020
• **Best Paper Award**, 25th ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC)	2020
• 4th Place, 2019 DAC System Design Contest on Low Power Object Detection	2019
• First Prize Scholarship, Fudan University	2017 – 2018
• Top 5, 2018 HUAWEI & FUTURELAB AI Contest (CV Group)	2018
• Top 11%, 2017 IEEEXtreme Global Programming Competition (out of 3,350 teams worldwide)	2017
• 2nd & 3rd Prize, National Mathematical Contest in Modeling	2016, 2017

ADDITIONAL INFORMATION

Computer Skills: Python (PyTorch/Tensorflow), C/C++, CUDA, Matlab, Verilog
Software: Cadence Virtuoso, Synopsys Design Compiler, Hspice, Xilinx Vivado Design Suite**,** Synopsys Optodesigner