YIBO LIN

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PhD ⋄ Department of Eletrical & Computer Engineering

RESEARCH INTERESTS

Modeling and optimization in VLSI CAD and emerging technology, machine learning applications, and hardware security

EDUCATION

University of Texas at Austin, TX, USA *Aug. 2013 – May 2018*
Ph.D. student, Department of Electrical and Computer Engineering
Advisor: David Z. Pan
Dissertation: "Bridging Design and Manufacturing Gap through Machine Learning and Machine-Generated Layout"
(GPA 3.96/4.0)

Shanghai Jiao Tong University, Shanghai, P.R.China *Sep. 2009 – Jun. 2013*
B.S., Department of Microelectronics
(GPA 91.17/100)
(Rank top 1/60)

EXPERIENCE

University of Texas at Austin, Texas, U.S. *Jun. 2018 – Jun. 2019*
Postdoc
ECE Department

Toshiba Memory Corporation, Yokohama, Japan *May 2017 – Aug. 2017*
Internship
Memory lithography group

IMEC, Leuven, Belgium *Sep. 2016 – Nov. 2016*
Internship
Design technology co-optimization for emerging lithography options

Chinese University of Hong Kong, China *Jun. 2016 – Aug. 2016*
Summer Intern
Quantum computing

Cadence Design System, TX, USA *May 2015 – Aug. 2015*
Summer Intern
Routability driven detailed placement

Oracle Inc., TX, USA *May 2014 – Aug. 2014*
Summer Intern
Incremental timing driven detailed placement

TEACHING EXPERIENCE

Guest Lecture	EE382M: VLSI Physical Design Automation	Fall 2017
Graduate Teaching Assistant	EE382M: VLSI I	Fall 2014

PUBLICATIONS

Book Chapters

[B1] **Yibo Lin** and David Z. Pan, "Machine Learning in Physical Verification, Mask Synthesis, and Physical Design", Machine Learning in VLSI Computer-Aided Design, Springer, 2018, edited by Abe Elfedel, Duane Boning and Xin Li. (**Invited Book Chapter**)(to be published)

Journal Papers

[J11] Wuxi Li, **Yibo Lin**, Meng Li, Shounak Dhar and David Z. Pan, "UTPlaceF 2.0: A High-Performance Clock-Aware FPGA Placement Engine", ACM Transactions on Design Automation of Electronic Systems (TODAES), 2017. (accepted)

[J10] **Yibo Lin**, Bei Yu, Meng Li and David Z. Pan, "Layout Synthesis for Topological Quantum Circuits with 1D and 2D Architectures", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct 6, 2017.

[J9] Xiaoqing Xu, **Yibo Lin**, Meng Li, Tetsuaki Matsunawa, Shigeki Nojima, Chikaaki Kodama, Toshiya Kotani and David Z. Pan, "Sub-Resolution Assist Feature Generation with Supervised Data Learning", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Aug 31, 2017.

[J8] **Yibo Lin**, Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu, Zhuo Li, Charles J Alpert and David Z. Pan, "MrDP: Multiple-row detailed placement of heterogeneous-sized cells for advanced nodes", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Aug 31, 2017.

[J7] **Yibo Lin**, Bei Yu, Yi Zou, Zhuo Li, Charles J Alpert and David Z. Pan, "Stitch aware detailed placement for multiple e-beam lithography", Integration, the VLSI Journal, Jun, 2017. (**Best Paper Award**)

[J6] **Yibo Lin**, Xiaoqing Xu, Bei Yu, Ross Baldick and David Z. Pan, "Triple/quadruple patterning layout decomposition via linear programming and iterative rounding", Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3), May 18, 2017.

[J5] Xiaoqing Xu, **Yibo Lin**, Meng Li, Jiaojiao Ou, B. Cline and D. Z. Pan, "Redundant local-Loop insertion for unidirectional routing", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jan 11, 2017.

[J4] **Yibo Lin**, Bei Yu, Biying Xu and David Z. Pan, "Triple patterning aware detailed placement toward zero cross-row middle-of-line conflict", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jan 05, 2017.

[J3] Bei Yu, Xiaoqing Xu, Subhendu Roy, **Yibo Lin**, Jiaojiao Ou and David Z. Pan, "Design for manufacturability and reliability in extreme-scaling VLSI", Science China Information Sciences, 2016. (**Invited paper**)

[J2] **Yibo Lin**, Bei Yu and David Z. Pan, "High performance dummy fill insertion with coupling and uniformity constraints", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Dec, 2016.

[J1] Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, **Yibo Lin**, Zhuo Li, Charles Alpert and David Z. Pan, "Methodology for standard cell compliance and detailed placement for triple patterning lithography", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), May, 2015.

Conference Papers

[C15] **Yibo Lin**, Yuki Watanabe, Taiki Kimura, Tetsuaki Matsunawa, Shigeki Nojima, Meng Li and David Z. Pan, "Data Efficient Lithography Modeling with Residual Neural Networks and Transfer Learning", ACM International Symposium on Physical Design (ISPD), Monterey, CA, Mar 25-28, 2018.

[C14] Meng Li, Bei Yu, **Yibo Lin**, Xiaoqing Xu, Wuxi Li and David Z. Pan, "A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Jeju, Korea, Jan 22-25, 2018.

[C13] **Yibo Lin**, Peter Debacker, Darko Trivkovic, Ryoung-han Kim, Praveen Raghavan and David Z. Pan, "Patterning Aware Design Optimization of Selective Etching in N5 and Beyond", IEEE International Conference on Computer Design (ICCD), Boston, MA, Nov 5-8, 2017.

[C12] **Yibo Lin**, Xiaoqing Xu, Jiaojiao Ou and David Z Pan, "Machine learning for mask/wafer hotspot detection and mask synthesis", Photomask Technology, Oct 16, 2017. (**Invited paper**)

[C11] Wei Ye, **Yibo Lin**, Xiaoqing Xu, Wuxi Li, Yiwei Fu, Yongsheng Sun, Canhui Zhan and David Z. Pan, "Placement Mitigation Techniques for Power Grid Electromigration", IEEE International Symposium on Low Power Electronics and Design (ISLPED), Taipei, Jul 24-26, 2017.

[C10] Xiaoqing Xu, **Yibo Lin**, Vinicius Livramento and David Z. Pan, "Concurrent Pin Access Optimization for Unidirectional Routing", ACM/IEEE Design Automation Conference (DAC), Austin, TX, Jun 18-22, 2017.

[C9] Jiaojiao Ou, Bei Yu, Xiaoqing Xu, Joydeep Mitra, **Yibo Lin** and David Z. Pan, "DSAR: DSA aware routing with simultaneous DSA guiding pattern and double patterning assignment", ACM International Symposium on Physical Design (ISPD), Portland, OR, Mar 19-22, 2017.

[C8] **Yibo Lin**, Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu, Zhuo Li, Charles J Alpert and David Z. Pan, "MrDP: Multiple-row detailed placement of heterogeneous-sized cells for advanced nodes", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, Nov 7-10, 2016.

[C7] Yudong Tao, Changhao Yan, **Yibo Lin**, Sheng-Guo Wang, David Z. Pan and Xuan Zeng, "A novel unified dummy fill insertion framework with SQP-based optimization method", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, Nov 7-10, 2016.

[C6] **Yibo Lin**, Bei Yu and David Z. Pan, "Detailed placement in advanced technology nodes: a survey", IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Hangzhou, China, Oct 25-28, 2016. (**Invited paper**)

[C5] **Yibo Lin**, Xiaoqing Xu, Bei Yu, Ross Baldick and David Z. Pan, "Triple/quadruple patterning layout decomposition via novel linear programming and iterative rounding", Proceedings of SPIE, San Jose, CA, Feb 21-25, 2016. (**Best Student Paper Award**)

[C4] **Yibo Lin**, Bei Yu, Yi Zou, Zhuo Li, Charles J Alpert and David Z. Pan, "Stitch aware detailed placement for multiple e-beam lithography", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Macau, China, Jan 25-28, 2016.

[C3] **Yibo Lin**, Bei Yu, Biying Xu and David Z. Pan, "Triple patterning aware detailed placement toward zero cross-row middle-of-line conflict", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, Nov 2-6, 2015.

[C2] **Yibo Lin**, Bei Yu and David Z. Pan, "High performance dummy fill insertion with coupling and uniformity constraints", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 7-11, 2015.

[C1] David Z. Pan, Lars Liebmann, Bei Yu, Xiaoqing Xu and **Yibo Lin**, "Pushing multiple patterning in sub-10nm: are we ready?", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 7-11, 2015. (**Invited Paper**)

RELATED COURSES

- EE382M: VLSI I — *Prof. Michael Orshansky*
- EE382N: Computer Architecture — *Prof. Aater Suleman*
- EE382V: Optimization Issues in VLSI CAD — *Prof. David Pan*
- EE382M: VLSI II — *Prof. Jacob Abraham*
- EE380L: Engineer Programming Languages — *Prof. Craig Chase*
- EE382V: Nanometer Scale IC Design — *Prof. Michael Orshansky*
- EE382V: VLSI Physical Design Automation — *Prof. David Pan*
- EE381V: Advanced Algorithms — *Prof. Evdokia Nikolova*
- EE382V: Advanced Programming Tools — *Prof. Aziz Adnan*
- EE380N: Optimization in Engineering Systems — *Prof. Ross Baldick*
- CS383C: Numerical Analysis: Linear Algebra — *Prof. Robert van de Geijn*

SKILLS

Programming Languages
C/C++, Python, Verilog

Web Development
HTML5, JavaScript/jQuery

EDA Tools
Cadence Virtuoso, Synopsys Design Compiler, Synopsys IC Compiler

AWARDS AND HONORS

Inaugural Best Paper Award	Integration, the VLSI Journal	2018
Graduate Continuing Fellowship	University of Texas at Austin	2017
Franco Cerrina Memorial Best Student Paper Award	SPIE	2016
A. Richard Newton Young Student Fellow	DAC	2014
National Scholarship	Shanghai Jiao Tong University	2012
Samsung Scholarship	Shanghai Jiao Tong University	2011
The Second Prize Scholarship	Shanghai Jiao Tong University	2010