YIBO LIN

University of Texas at Austin, Austin, TX 78712 ◇ University of Texas at Austin
yibolin@utexas.edu ◇ www.cerc.utexas.edu/~yibolin
PhD student ◇ Department of Eletrical & Computer Engineering

RESEARCH INTERESTS

Nanometer IC design for manufacturability, modeling and optimization in VLSI CAD

EDUCATION

University of Texas at Austin, TX, USA *Aug. 2013 – Present*
Ph.D. student, Department of Electrical and Computer Engineering
Advisor: David Z. Pan
(GPA 3.96/4.0)

Shanghai Jiao Tong University, Shanghai, P.R.China *Sep. 2009 – Jun. 2013*
B.S., Department of Microelectronics
(GPA 91.17/100)
(Rank top 1/60)

EXPERIENCE

IMEC, Leuven, Belgium *Sep. 2016 – Nov. 2016*
Internship
Design technology co-optimization for emerging lithography options

Chinese University of Hong Kong, China *Jun. 2016 – Aug. 2016*
Summer Intern
Quantum computing

Cadence Design System, TX, USA *May 2015 – Aug. 2015*
Summer Intern
Routability driven detailed placement

Oracle Inc., TX, USA *May 2014 – Aug. 2014*
Summer Intern
Incremental timing driven detailed placement

ECE Department, University of Texas at Austin, TX, USA *Jan. 2014 – Present*
Graduate Research Assistant
Multiple patterning lithography layout decomposition
Stitch aware detailed placement
Triple-patterning aware detailed placement
Dummy fill insertion
Detailed-routing-driven placement

PUBLICATIONS

Journal Papers

[J3] **Yibo Lin**, Bei Yu and David Z. Pan, "High Performance Dummy Fill Insertion with Coupling and Uniformity Constraints", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2016. (submitted)

[J2] Bei Yu, Xiaoqing Xu, Subhendu Roy, **Yibo Lin**, Jiaojiao Ou, and David Z. Pan, "Design for Manufacturability and Reliability in Extreme-Scaling VLSI", Science China Information Sciences, 2016 (**Invited paper**)

[J1] Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, **Yibo Lin**, Zhuo Li, Charles Alpert, and David Z. Pan, "Methodology for Standard Cell Compliance and Detailed Placement for Triple Patterning Lithography", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol.34, no.5, pp.726-739, 2015.

Conference Papers

[C8] Yudong Tao, Changhao Yan, **Yibo Lin**, Shengguo Wang, David Z. Pan, and Xuan Zeng, "A Novel Unified Dummy Fill Insertion Framework with SQP-Based Optimization Method", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, Nov. 7-10, 2016 (to appear)

[C7] **Yibo Lin**, Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu, Zhuo Li, Charles J. Alpert and David Z. Pan, "MrDP: Multiple-row Detailed Placement of Heterogeneous-sized Cells for Advanced Nodes", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, Nov. 7-10, 2016 (to appear)

[C6] **Yibo Lin**, Bei Yu, and David Z. Pan, "Detailed Placement In Advanced Technology Nodes: A Survey", IEEE International Conference on Solid -State and Integrated Circuit Technology (ICSICT), Hangzhou, China, Oct. 25-28, 2016 (**Invited paper**) (to appear)

[C5] **Yibo Lin**, Xiaoqing Xu, Bei Yu, Ross Baldick, and David Z. Pan, "Triple/Quadruple Patterning Layout Decomposition via Novel Linear Programming and Iterative Rounding", SPIE Advanced Lithography Conference, San Jose, CA, Feb. 21-25, 2016 (**Best Student Paper Award**)

[C4] **Yibo Lin**, Bei Yu, Yi Zou, Zhuo Li, Charles J. Alpert and David Z. Pan, "Stitch Aware Detailed Placement for Multiple E-Beam Lithography", IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC), Macau, Jan. 25-28, 2016.

[C3] **Yibo Lin**, Bei Yu, Biying Xu and David Z. Pan, "Triple Patterning Aware Detailed Placement Toward Zero Cross-Row Middle-of-Line Conflict", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, Nov. 2-6, 2015.

[C2] David Z. Pan, Lars Liebmann, Bei Yu, Xiaoqing Xu and **Yibo Lin**, "Pushing Multiple Patterning in Sub-10nm: Are We Ready?", ACM/IEEE Design Automation Conference (DAC), pp. 197:1-197:6, San Francisco, CA, June 7-11, 2015. (**Invited Paper**)

[C1] **Yibo Lin**, Bei Yu and David Z. Pan, "High Performance Dummy Fill Insertion with Coupling and Uniformity Constraints", ACM/IEEE Design Automation Conference (DAC), pp. 71:1-71:6, San Francisco, CA, June 7-11, 2015.

RELATED COURSES

- EE382M: VLSI I — *Prof. Michael Orshansky*
- EE382N: Computer Architecture — *Prof. Aater Suleman*
- EE382V: Optimization Issues in VLSI CAD — *Prof. David Pan*
- EE382M: VLSI II — *Prof. Jacob Abraham*
- EE380L: Engineer Programming Languages — *Prof. Craig Chase*
- EE382V: Nanometer Scale IC Design — *Prof. Michael Orshansky*
- EE382V: VLSI Physical Design Automation — *Prof. David Pan*
- EE381V: Advanced Algorithms — *Prof. Evdokia Nikolova*
- EE382V: Advanced Programming Tools — *Prof. Aziz Adnan*
- EE380N: Optimization in Engineering Systems — *Prof. Ross Baldick*
- CS383C: Numerical Analysis: Linear Algebra — *Prof. Robert van de Geijn*

SKILLS

Programming Languages
C/C++, Python, Verilog

Web Development
HTML5, JavaScript/jQuery

EDA Tools
Cadence Virtuoso, Synopsys Design Compiler, Synopsys IC Compiler

AWARDS AND HONORS

Franco Cerrina Memorial Best Student Paper Award	SPIE	2016
A. Richard Newton Young Student Fellow	DAC	2014
National Scholarship	Shanghai Jiao Tong University	2012
Samsung Scholarship	Shanghai Jiao Tong University	2011
The Second Prize Scholarship	Shanghai Jiao Tong University	2010