

# Power MOSFET

**TO-220AB**


N-Channel MOSFET

## FEATURES

- Dynamic dV/dt rating
- Logic-level gate drive
- $R_{DS(on)}$  specified at  $V_{GS} = 4\text{ V}$  and  $5\text{ V}$
- $175\text{ }^{\circ}\text{C}$  operating temperature
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS\***  
Available

## Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

## DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

## PRODUCT SUMMARY

$V_{DS}$ (V)	60	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 5.0\text{ V}$	0.20
$Q_g$ (Max.) (nC)	8.4	
$Q_{gs}$ (nC)	3.5	
$Q_{gd}$ (nC)	6.0	
Configuration	Single	

## ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRLZ14PbF
Lead (Pb)-free and halogen-free	IRLZ14PbF-BE3

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	60	V
Gate-source voltage	$V_{GS}$	$\pm 10$	
Continuous drain current	$I_D$	$T_C = 25\text{ }^{\circ}\text{C}$	A
		$T_C = 100\text{ }^{\circ}\text{C}$	
Pulsed drain current <sup>a</sup>	$I_{DM}$	40	
Linear derating factor		0.29	W/ $^{\circ}\text{C}$
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	39.5	mJ
Maximum power dissipation	$P_D$	43	W
Peak diode recovery dV/dt <sup>c</sup>	dV/dt	4.5	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	$^{\circ}\text{C}$
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300 <sup>d</sup>	
Mounting torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

## Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 25\text{ V}$ , starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $L = 0.79\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 10\text{ A}$  (see fig. 12)
- $I_{SD} \leq 10\text{ A}$ ,  $dI/dt \leq 90\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175\text{ }^{\circ}\text{C}$
- 1.6 mm from case

**THERMAL RESISTANCE**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	-	62	°C/W
Case-to-sink, flat, greased surface	$R_{thCS}$	-	0.50	-	
Maximum junction-to-case (drain)	$R_{thJC}$	-	-	3.5	

**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		60	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.070	-	V/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		1.0	-	2.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 10 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C		-	-	250	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 5.0 V	I <sub>D</sub> = 6.0 A <sup>b</sup>	-	-	0.20	Ω
		V <sub>GS</sub> = 4.0 V	I <sub>D</sub> = 5.0 A <sup>b</sup>	-	-	0.28	
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 6.0 A <sup>b</sup>		3.5	-	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	400	-	pF
Output capacitance	C <sub>oss</sub>			-	170	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	42	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 5.0 V	I <sub>D</sub> = 10 A, V <sub>DS</sub> = 48 V see fig. 6 and 13 <sup>b</sup>	-	-	8.4	nC
Gate-source charge	Q <sub>gs</sub>			-	-	3.5	
Gate-drain charge	Q <sub>gd</sub>			-	-	6.0	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 10 A R <sub>g</sub> = 12 Ω, R <sub>D</sub> = 2.8 Ω see fig. 10 <sup>b</sup>		-	9.3	-	ns
Rise time	t <sub>r</sub>			-	110	-	
Turn-off delay time	t <sub>d(off)</sub>			-	17	-	
Fall time	t <sub>f</sub>			-	26	-	
Internal drain inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L <sub>S</sub>			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	10	A
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>			-	-	40	
Body diode voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.6	V
Body diode reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 10 A, dI/dt = 100 A/μs <sup>b</sup>		-	93	130	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	0.34	0.65	μC
Forward turn-on time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

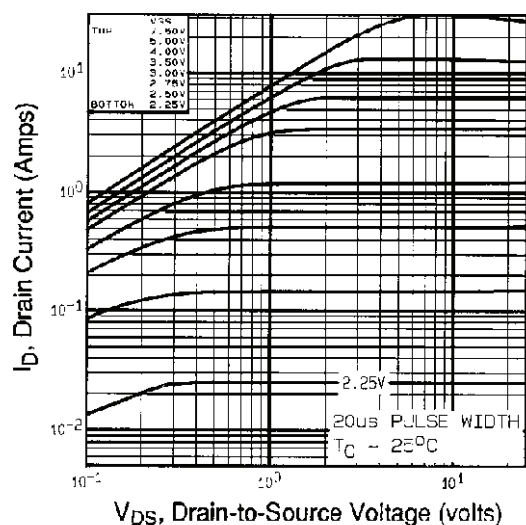


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$

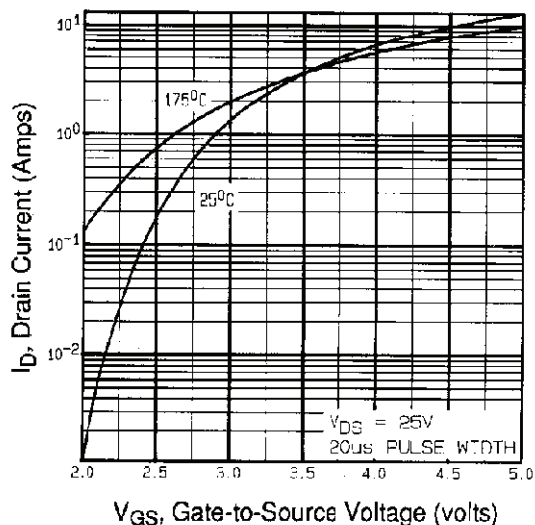


Fig. 3 - Typical Transfer Characteristics

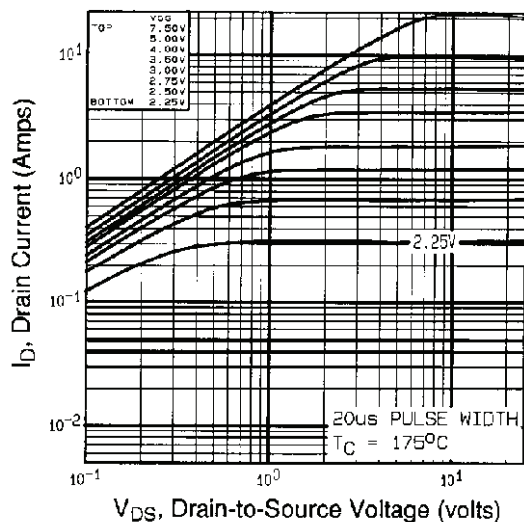


Fig. 2 - Typical Output Characteristics,  $T_C = 175\text{ }^{\circ}\text{C}$

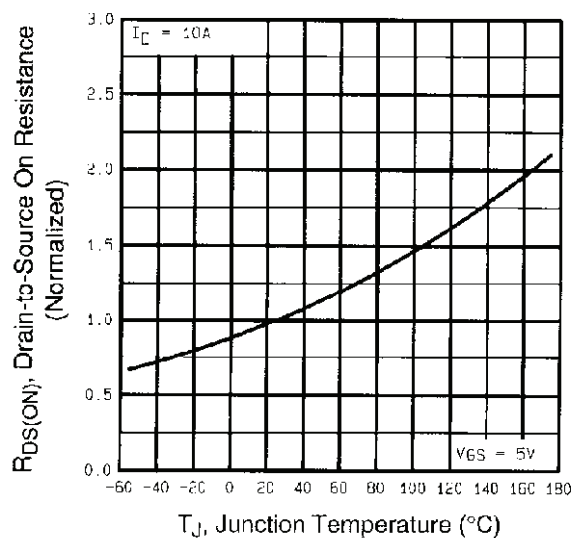
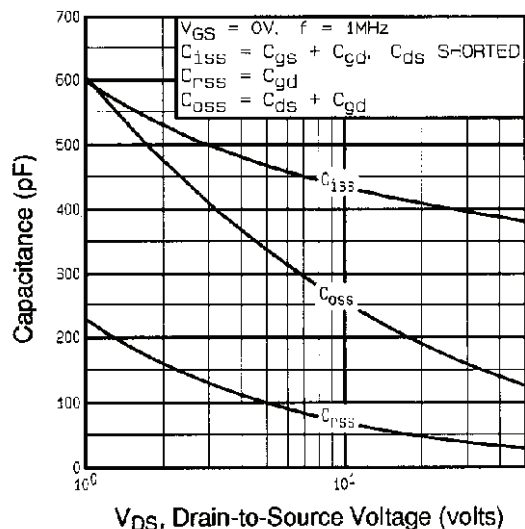
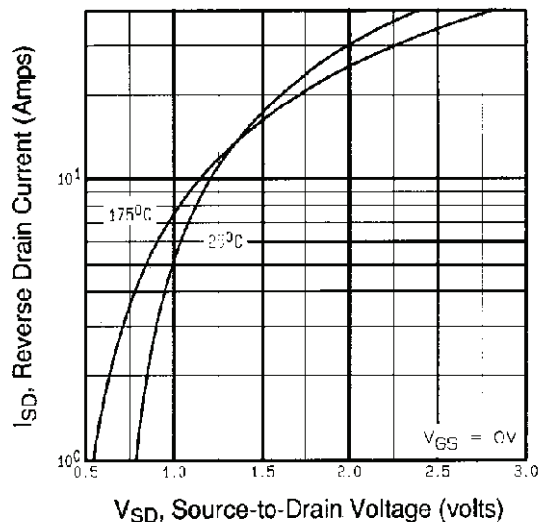
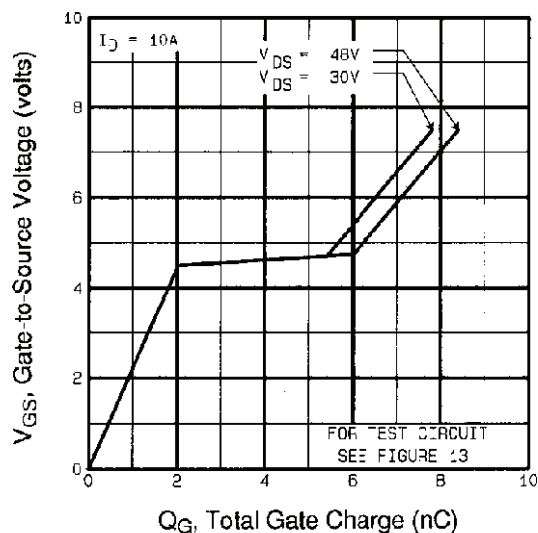
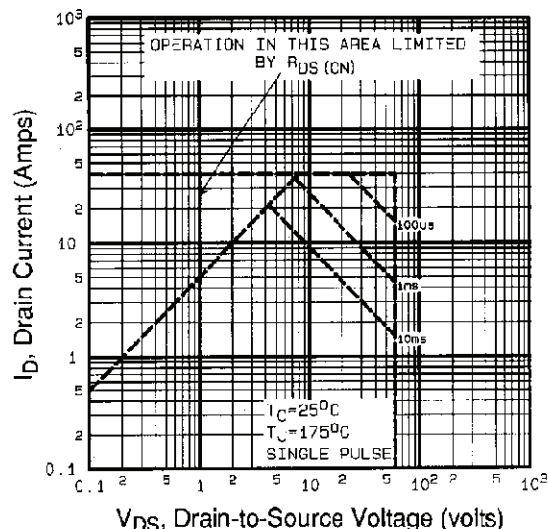
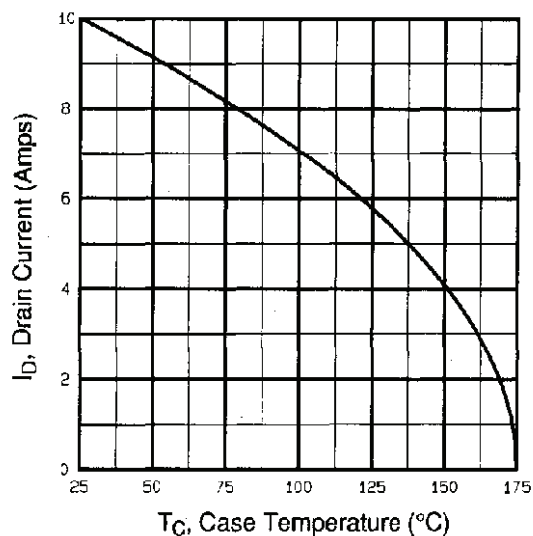
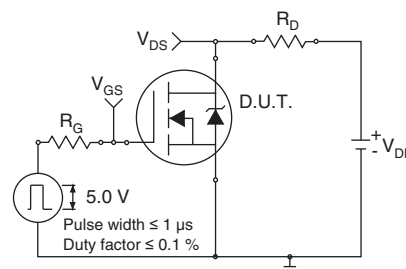
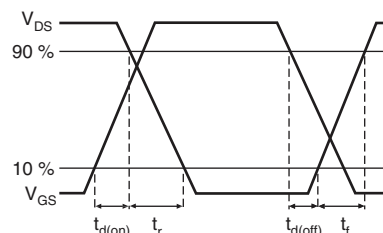
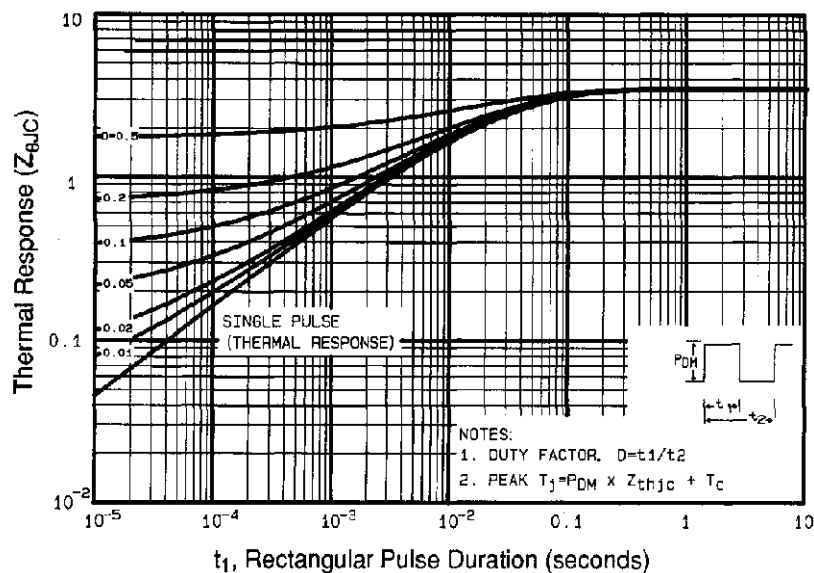
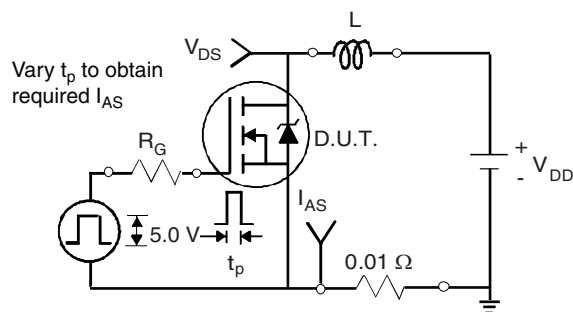
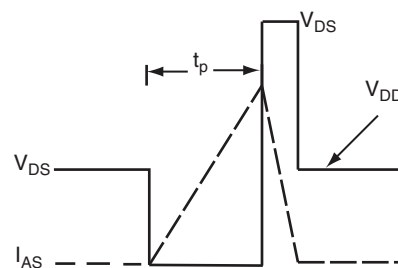
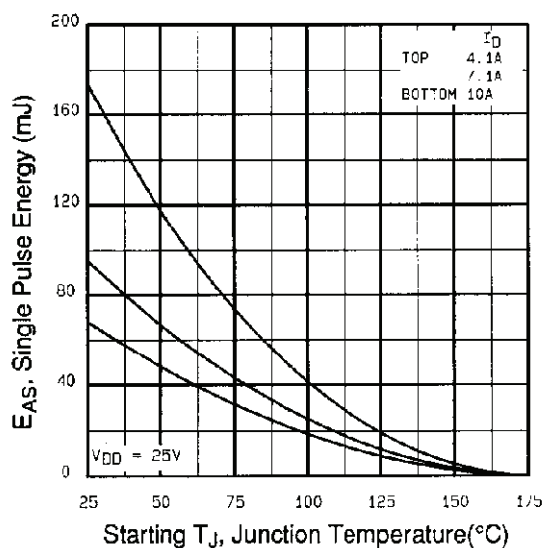
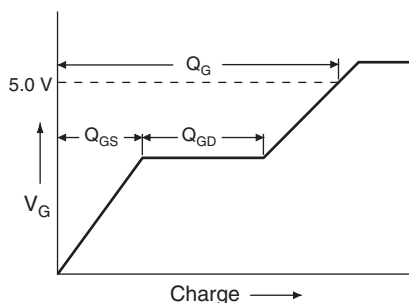
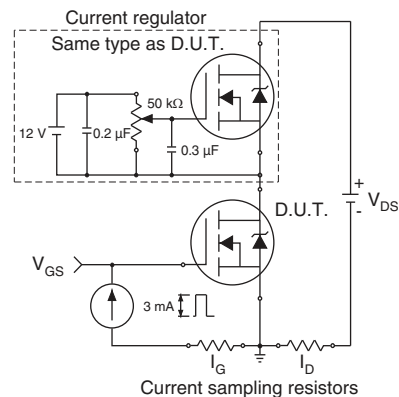
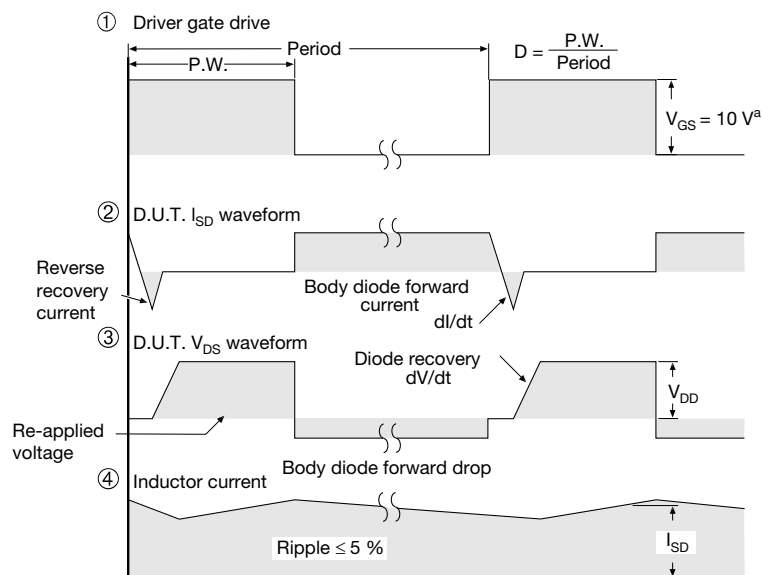
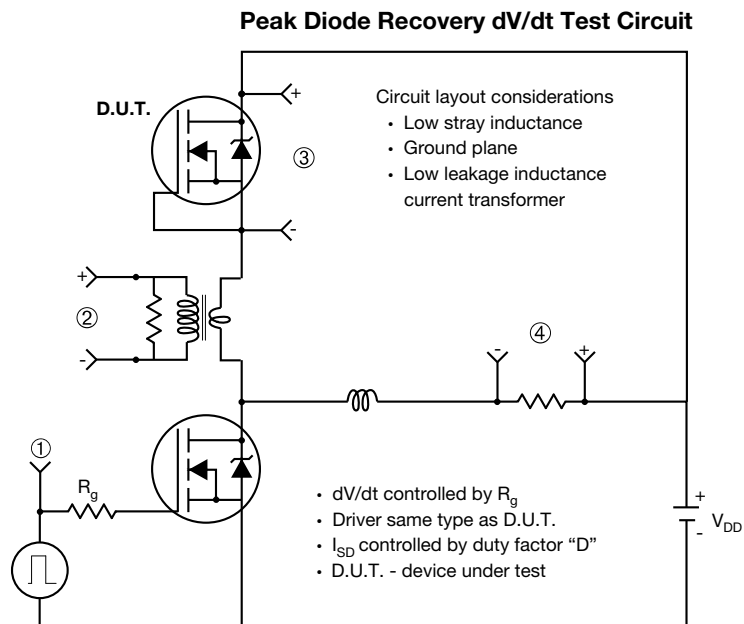


Fig. 4 - Normalized On-Resistance vs. Temperature


**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 8 - Maximum Safe Operating Area**


**Fig. 9 - Maximum Drain Current vs. Case Temperature**

**Fig. 10a - Switching Time Test Circuit**

**Fig. 10b - Switching Time Waveforms**

**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**


**Fig. 12a - Unclamped Inductive Test Circuit**

**Fig. 12b - Unclamped Inductive Waveforms**

**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

**Fig. 13a - Basic Gate Charge Waveform**

**Fig. 13b - Gate Charge Test Circuit**



**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

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