ECE 645
Spring 2013

Homework 5

due Saturday, April 27, 11:59PM

Problem 1

Perform the following tasks for the unsigned Radix-4 shift/add sequential multiplier with right shift, and the upper half of the cumulative partial product kept in the carry-save form (the signed version of this multiplier is shown conceptually in Parhami, 2nd ed., Figures 10.9 and 10.10). Assume that both operands are of the size of k bits.

1. Draw a detailed block diagram, based on D flip-flops, multiplexers (with each data input of the size of 1 bit), Full Adders, Half-Adders, and logic gates, for k=4.
2. Draw a generalized block diagram, based on registers (of arbitrary size), multiplexers (with arbitrary size of data inputs), adders (with arbitrary size of operands), bit-by-word logic operators (e.g., b AND a, where b is a bit, and a is a k-bit word), and logic gates, for arbitrary value of k.
3. Mark the critical path on both block diagrams.
4. Derive the formulas for the following performance metrics of the k x k bit multiplier (assuming k is even):
    a. Minimum clock period, as a function of the delays and timing parameters of basic logic components (e.g., d_{FF}, d_{AND2}, t_{setup}), and the parameter k
    b. Minimum latency
    c. Maximum throughput (in additions per second).
5. Compare all performance metrics of this multiplier with the performance metrics of an equivalent multiplier with Radix-2.

Problem 2

Show all intermediate values obtained during the calculation of the product $p=a \cdot x$, for the multiplier from Problem 1.

Assume: $k = 4$, $a = 13$, $x = 12$.