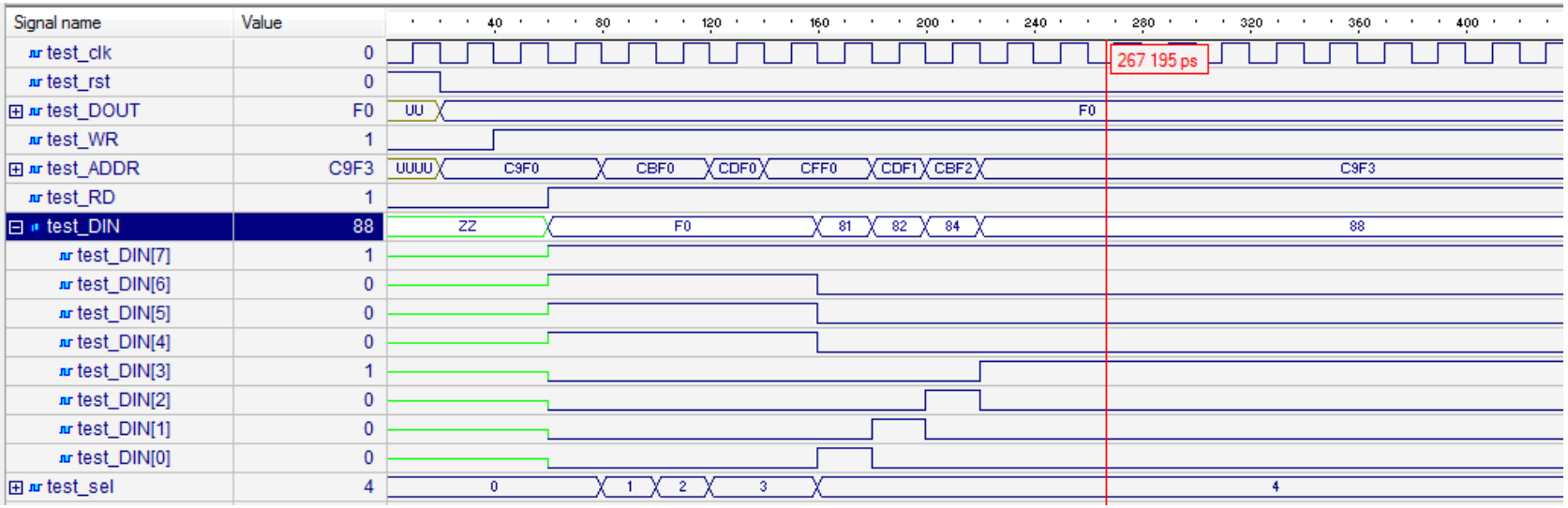

Functional Simulation Log

asim +access +r -advdataflow Homework4_Task6_tb

Warning: Verilog Optimization cannot be used when -advdataflow is in effect. Verilog Optimization disabled.

Simulation has been stopped

ELBREAD: Elaboration process.

ELBREAD: Elaboration time 0.0 [s].

asim: Stack memory: 32MB

asim: Retval memory: 32MB

#

KERNEL: Main thread initiated.

KERNEL: Kernel process initialization phase.

KERNEL: Time resolution set to 1ps.

ELAB2: Elaboration final pass...

ELAB2: Create instances ...

ELAB2: Create instances complete.

ELAB2: Elaboration final pass complete - time: 0.0 [s].

KERNEL: Warning: You are using the Active-HDL Student Edition. The performance of simulation is running at a reduced rate.

KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.

KERNEL: Kernel process initialization done.

Allocation: Simulator allocated 6148 kB (elbread=1023 elab2=5033 kernel=91 sdf=0)

KERNEL: ASDB file was created in location C:\My_Designs\Homework4_Task6\Homework4_Task6\src\wave.asdb

12:18 AM, Saturday, October 13, 2012

Simulation has been initialized

Selected Top-Level: Homework4_Task6_tb (arch_Homework4_Task6_tb)